Improving the Quasi Resonant DC Link in the Voltage Inverter

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ABSTRACT:
One of the fundamental structures of inverters with soft switching is the use of quasi-resonant DC link (QRDCL) circuits, in which element switching occurs in the zero voltage (ZVS) and / or zero current (ZCS) conditions and also the use of pulse width modulation (PWM). One of the indices of distinction and superiority of these converters is losses in the QRDCL circuit, fewer losses, and the increase of converter's frequency. This paper aims to calculate losses of the QRDCL and the design control circuits of the improved QRDCL voltage inverter. In this regard, at first, the benefits of soft switching and general characteristics of various types of topologies used in inverters with soft switching is studied and then, the desired improved inverter with the capability of EDPWM (Enhanced Double PWM) which uses the single-phase soft switching technique (SPSS) is introduced. For proper functioning of the circuit, a particular type of the sinusoidal pulse width modulation (SPWM) is used, which its characteristics are studied and then the desired control circuit inverter is proposed. Finally, the full simulation of the inverter is conducted and the obtained results of analyzing the functionality of the circuit and mathematical equations governing the circuit are compared with the results come from computer simulation.

KEYWORDS: Inverter, Soft switching, QRDCL, PWM, Losses, EDPWM, SPSS.

1. INTRODUCTION

In the hard switching circuits with a PWM capability, considering to the simplicity of a power circuit, there are some limitations; such as high stress of switching elements, high switching losses, high dv/dt and di/dt etc. If the switching elements switch in the ZVS or ZCS, soft switching mode occurs. With using of soft switching methods, the problems of hard switching circuits greatly reduced, so the switching frequency can be increased, which causes the reduction in price, weight and size of filter elements (remove harmonics), the decrease of acoustic noise and the increase of output control speed.

The main characteristic of the DC link inverter is an added resonant circuit with high frequency in main structure of the inverter which only acts when the link voltage is zero and returned to the first statues and in other times the same resonant circuit is completely out of the circuit. The resonant circuit is controlled by some switches and through adjusting the times of its function, the times of zero voltages can be controlled so implementation of PWM is possible.

Soft switching topologies can be classified based on the location of resonant circuit, kind of resonant circuit (i.e. series or parallel) and ZVS or ZCS properties, which are provided by the resonant circuit, as per the Figure (1), [1].

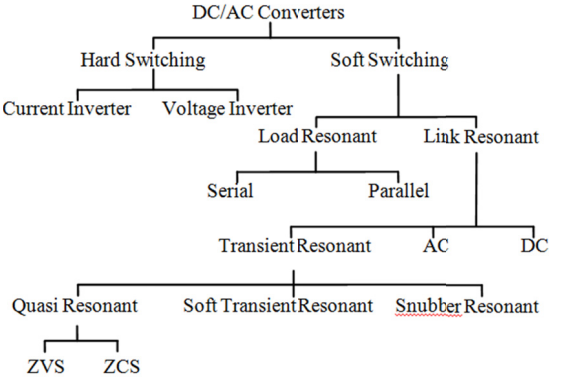

Fig. 1. Soft switching topologies

Each topology presented in Figure (1) has properties, which justify their applications under some circumstances, among these topologies, QRDCL inverters for having some benefits such as the possibility of using of PWM, reduction of di/dt and dv/dt, the independent performance of the resonant

circuit from the load, the acting of the resonant circuit only at times of switching and finally, the decrease of losses related to the resonant elements for the average power (few KW level), are much considered [1]-[5].

The disadvantages of the circuits' topology are: an added auxiliary high power switch in the main circuit, the need to backing the resonant link to the initial state after each switching, the increase some of the auxiliary switches in the resonant circuit and consequently, the relative complexity of the control system [6]-[8].

2. PROPOSED THREE-PHASE VOLTAGE INVERTER WITH QUASI-RESONANT DC LINK

A new type of DC link voltage inverter with the ability for performing quasi-resonant PWM in two areas (Enhanced Double PWM-EDPWM) and also using of the single phase soft switching technique (SPSS) has been proposed [1]. Figure (2) shows the power circuit and the circuit of proposed resonant inverter. The resonant circuit includes four switches SL, SD, SU, S and DL, DD, DU diodes, resonant inductor L, resonant capacitor C1 and Cr (parallel to the main switches for utilizing of SPSS technique).

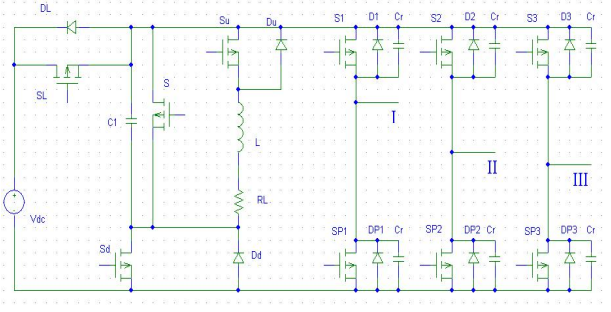

Fig. 2. The proposed quasi-resonant inverter

In this circuit, through increasing the number of auxiliary switches of the resonant circuit and also using of PWM, the resonant circuit return to the initial state without energy, after each time activating this causes the simplicity of the control system of the circuit. Conditions in the proposed circuit are in a way that ZVS mode is provided for the main power switches and in addition, due to the being of the capacitors (distributed) which are paralleled to the main switches, turning off these switches occurs with the least losses. ZVS and ZCS conditions are established for auxiliary switches of the resonant circuit. So, the only major problem of this circuit is additional supplementary guidance losses of the auxiliary switch SL which is located in the mainstream current.

3. MODULATION METHOD

Modulation used in the proposed circuit should have the following conditions:

A - For decreasing the mortalities come from switching off, some parallel capacitors are distributed on the main switches and for avoiding from high discharge current in switches and achieving to the ZVS conditions link voltage should be zero during the turning on the switches.

B - For the proper function of the resonant circuit, the direction of current should be reversed after changing the switches' position, because at the beginning of each period, the direction of current is from the main bridge to the resonant circuit. To achieve this characteristic for each phase pair of power switches, a switch turn on at the beginning of each switching period that the same switch carrying the current not the reverse parallel diode.

For easy control of output voltage, SPWM with minor modifications is used. Using a saw tooth wave instead of a symmetric triangle wave as a carrier and also using feedback for (Mark) current of each phase, for determining how to turn on and off switching of the phase, provide the A and B conditions [9].

Figure (3) shows the first-phase phase control circuit inverter. In this circuit the signal Vf, feedback direction current, Vramp-1 and Vramp-2 two reversed saw tooth waves, and Vref is the sine wave of the first-phase reference.

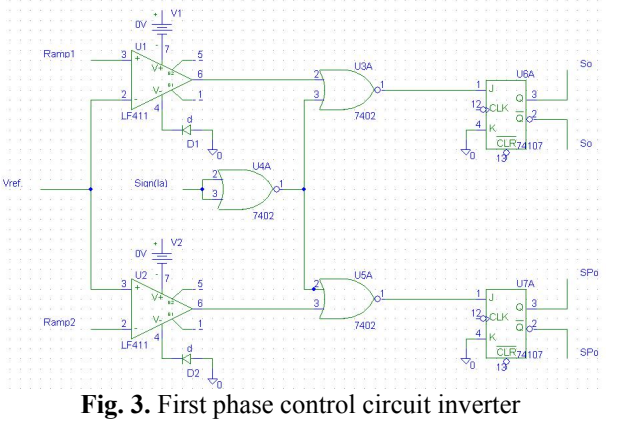

Fig. 3. First phase control circuit inverter

4. INTRODUCTION OF QRDCL

The proposed quasi-resonant circuit Figure(4), has seven function modes (Table (1)) in which link voltage reaches zero and after turning on the power switches and changing the direction of the link current, link voltage back to the initial value. Details and relations related to each of modes of the proposed circuit in reference [1] are fully described. Here for understanding the results of simulation, a summary of the circuit status in each of the modes is described.

For simplicity and better analysis of the proposed circuit from its equivalent circuit, Figure (4) is used.

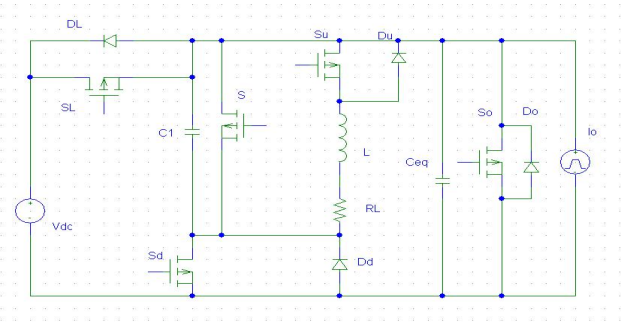

Fig. 4. The proposed equivalent circuit

Cr Capacitors which are distributed on the main switches, modeled with a Ceq capacitor which its value in each switching period is 3Cr.

Do diode is the reversed parallel diodes model of the main switches of the inverter and prevents of negative link voltage.

Io current source is a current which pulled by the inverter's outputs and during a switching period, considering to the largeness of the output filter inductor or the load inductor, can be assumed constant with a good approximation. So switch is equivalent to at least two switches on an inverter phase or all inverter switches.

Mode 0 (t0-t1): SL and SD are on, and the remaining switches and diodes are off. (Time of performance PWM and Tpwm1 can be controlled.) C1 and Ceq Capacitors are charge to size of Vs and link voltage is equivalent to Vs.

Mode I (t1-t2): SU is on when current is zero and inductor current increased to Ip linearly (Control section).

Mode II (t2-t3): SL is off when the voltage is and occurs between inductor and C1 capacitors and Ceq resonant. Thus, the capacitor voltage is zero and inductor current reaches to the maximum.

Mode III (t3-t4): SD is off when the voltage is zero and C1 capacitor, and inductor will continue to be resonant untill C1 capacitor voltage reaches to the negative value -VC1max. When the inductor current is negative, Du diode leads instead of Su switch and inductor current reaches to its negative maximum value (-Ilmax).

Mode IV(t4-t5): S is on when the voltage is zero and inductor current is spinning between Du and S and voltage of the C1 capacitor remains constant in a zero state. (Performance time of PWM and Tpwm2 can be controlled.)

Mode V (t5-t6): S is off when the voltage is zero and resonant between L inductor and C1 and Ceq capacitors cause the link voltage increase to Vs.

Mode VI (t6-t7): Turning on the DL (or SL switch when the voltage is zero) causes the added inductor current discharge in the source and control circuit of link voltage return to the initial state. In this state, DL and Du and Dd diodes are on.

In Figure (5), control circuit is shown and it can see that the structure of control circuit is simple.

The Various modes of the proposed circuit are described in Table (1).

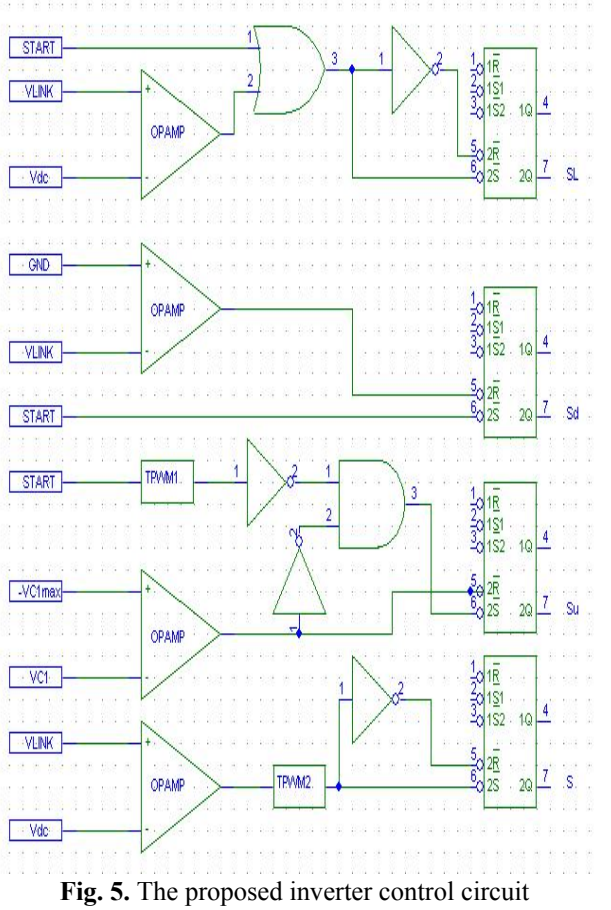

Fig. 5. The proposed inverter control circuit

Table 1. The various modes of the proposed circuit

Modes / Switches	0 t0-t1	1 t1-t2	2 t2-t3	3 t3-t4	4 t4-t5	5 t5-t6	6 t6-t7
S_L	ON	ON	OFF	OFF	OFF	OFF	OFF
D_L	OFF	OFF	OFF	OFF	OFF	OFF	ON
S_D	ON	ON	ON	OFF	OFF	OFF	OFF
D_D	OFF	OFF	OFF	OFF	OFF	ON	ON
S_u	OFF	ON	ON	ON	OFF	OFF	OFF
D_u	OFF	OFF	OFF	ON	ON	ON	ON
S	OFF	OFF	OFF	OFF	ON	OFF	OFF

T0=t1-t2=Tpwm1= Controllable time

T1=t2-t1=(Ip*L)/Vs

T2=t3-t2=1/ω1*Arc Sin(Vs/(Vs+2Zo*Io))

T3=t4-t3=π/ω2

T4=t5-t4=Tpwm2= Controllable time

T5=t6-t5= π/(2*ω1)

T6=t7-t6=(Io*L)/Vs

T(Periodic Cycle) = Σ (Ti) =1/f(Frequency)

5. LOSSES OF QUASI-RESONANT DC LINK

The motivation for the use of the resonant inverter

stems from a desire to eliminate the switching losses in the inverter devices. One of the suitable parameters in selecting quasi resonant DC link is losses, the less losses, the more increase in work frequency. So, this case can be more considered in average and high power.

There are various ways for evaluating the losses in quasi-resonant dc link. One of these ways is obtaining different output power from input power and taking the integral of that in a specified range [10].

Losses in the QRDCL circuit shall be classified into four parts: conduction losses, switching losses, off state losses and resistive losses. Equations for estimating the various losses in the QRDCL inverter are developed.

5.1. Conduction Losses: Include on-state losses and dynamic saturation. On-state losses are a part of the conduction losses which relates to the time the switch is on. Dynamic saturation loss is another part of conduction losses that happens when the switch is on its voltage won't change from full off-state to full joint-state constantly but quickly reaches from full off-state to about saturation voltage, but in the near of saturation voltage goes into saturation with the lower speed. The time it takes to voltage on two double voltage switch reaches from 10% of off-state voltage to 110% of saturation state voltage, named dynamic saturation time, which depends on the switch characteristic and is generally between 1 to 10 μsec.

5.2. Switching Losses: Include two parts: turn-on losses and turn-off losses. Considering that the main switches of the inverter with QRDCL are on when voltage or current is zero, so there are no switching losses when the switches are on, and switching losses can be calculated only when soft switching condition for turning off the switches is not ruled.

5.3. Off State Losses: Off state losses in power electronic circuits, is considered as a very little part of the total losses and is generally ignored. These losses are due to the passing the reverse saturation current in switches and considering to this fact the switches are off and there is the double voltage. These losses can be calculated precisely.

5.4. Resistive Losses: These are due to the passing current from resonant inductor resistance in QRDCL circuit.

6. THE LOSSES IN PROPOSED IMPROVED QRDCL INVERTER [1]

Through adding a switch to the reference resonant circuit [11] can increase the capability of PWM in both up and down edges of link voltage. Furthermore, with distributing link capacitor as distributed capacitors on the main inverter's switches by using the SPSS technique, can off the main carrier switches in inverter even when the link voltage is not zero Figure(2).

For calculating the losses of DC link, considering to the equivalent circuit in Figure(4), (conduction losses, which are due to the turning on diodes and switches and also switching losses, which are due to turning off the switches and resistive losses of the resonant inductor), should be calculated.

Conduction losses of turning on the switches and diodes, obtain through using the different stages of circuit performance and mathematical relations governing them obtain by using following equations in which Zo = (L/C)½, ω1 = (1/(LC)½), ω2 = (1/(LC1)½), Ip = (Vs/Zo)*Cos(ω1*t2)-Io, ILmax = Io+Vs/Zo, C = Ceq+C1, T2=(1/ω1)*Arc(Sin(Vs/(Vs+2*Io*Zo))), f is the switching frequency, VCE (Sat.) is double switch voltage in the mode of being on, Vf is double diode voltage in the mode of being on, PSL(Cond), PSU(Cond), PSd(Cond) and PS(Cond) are respectively conduction losses when the switches SL, SU, Sd and S are on and PDL(Cond), PDU(Cond) and PDd(Cond) are respectively conduction losses when the diodes DL, DU, Dd are on.

$$P_{SL(cond)} = f.V_{CE(sat)}.[\int_{t0}^{t1} I_o.dt + \int_{t1}^{t2} (\tfrac{Vs}{L}(t-t1)+I_o).dt] \quad (1)$$

$$P_{DL(cond)} = f.V_f.[\int_{t6}^{t7} (\tfrac{-Vs}{L}(t-t6)).dt] \quad (2)$$

$$P_{Su\,(cond\,)} = f.V_{CE\,(sat\,)}.[\int_{t6}^{t7} (\tfrac{Vs}{L}(t-t1)).dt + \int_{t2}^{t3} [(I_P+I_o)Cos\omega_1(t-t2)+\tfrac{Vs}{Zo}Sin\omega 1(t-t2)-I_o].dt + \int_{t3}^{t4} [(I_{L\max} Cos\ \omega_2(t-t3).dt\ ] \quad (3)$$

$$P_{Du\,(cond\,)} = f.V_f.[\int_{t4}^{t5} [(I_{L\max}.dt + \int_{t5}^{t6} [(I_{L\max}-I_o)Cos\omega_1(t-t5)+I_o]dt + \int_{t6}^{t7} (\tfrac{-Vs}{L}(t-t6)+I_o)dt \quad (4)$$

$$P_{Sd\,(cond\,)} = f.V_{CE\,(sat\,)}.[\int_{t1}^{t2} (\tfrac{Vs}{L}(t-t1)).dt + \int_{t2}^{t3} [(I_P+I_o)Cos\omega_1(t-t2)+\tfrac{Vs}{Zo}Sin\omega 1(t-t2)-I_o].dt] \quad (5)$$

$$P_{Dd\,(cond\,)} = f.V_f.[\int_{t6}^{t7} (\tfrac{-Vs}{L}(t-t6)+I_O).dt + \int_{t5}^{t6} [(I_{L\max}-I_o)Cos\ \omega_1(t-t5)+I_o].dt] \quad (6)$$

$$P_{S\,(cond\,)} = f.V_{CE\,(sat\,)}.[\int_{t4}^{t5} I_{L\max}.dt\ ] \quad (7)$$

Switching losses for turning off each of the link circuit switches can be calculated from the following equations in which tf is switched off time, and C is the capacity of the switch output capacitor and f is switching frequency, PSL(sw), PSU(sw) , PSd(sw) and PS(sw) are respectively the switching losses, when the SL, SU, Sd and S switches are off.

$$P_{SL(SW)} = \frac{(I_o + \frac{V_S}{L}(t2-t1))^2 .t_f^2 .f}{24C} \quad (8)$$

$$P_{Su(SW)} = \frac{(I_{L\max} .Cos\omega_2 (t4-t3))^2 .t_f^2 .f}{24(C+C_1)} \quad (9)$$

$$P_{Sd(SW)} = \frac{(\frac{V_S}{L} .Sin\omega_1 (t_3 - t_2) + (I_o + I_P).Cos\omega_1 (t3-t2) - I_o)^2}{24C} * t_f^2 .f \quad (10)$$

$$P_{S(SW)} = \frac{I_{L\max}{}^2 .t_f^2 .f}{24(C+C_1)} \quad (11)$$

To calculate the resistive losses of the resonant inductor the following equation is used, in which f is switching frequency and RL is resistance of the resonant inductor:

$$P_{SL(cond)} = f.R_L .[\int_{t1}^{t2} (\frac{V_S}{L}(t-t1))^2 .dt] + \quad (12)$$

$$\int_{t2}^{t3} [(I_P + I_o)Cos\omega_1 (t-t2) + \frac{V_S}{Zo} Sin\omega 1(t-t2) - I_o]^2 .dt +$$

$$\int_{t3}^{t4} [(I_{L\max} Cos\omega_2 (t-t3)]^2 .dt + \int_{t4}^{t5} (I_{L\max})^2 .dt +$$

$$\int_{t5}^{t6} [(I_o - I_{L\max})Cos\omega_1 (t-t4) - I_o]^2 .dt + \int_{t6}^{t7} (\frac{V_S}{L}(t-t5) - I_o)^2 .dt$$

To calculate the total losses of QRDCL circuit, the following equation is used:

$$P_{total} = P_{Cond} + P_{SW} + P_{RL} \quad (13)$$

In which Pcond is total conduction losses and obtain from the summation of relations (1) to (7) and Psw is total switching losses and obtain from the summation of relations (8) to (11).

7. SIMULATION OF QRDCL CIRCUIT

Using the electronic software pspice, the equivalent circuit of the proposed inverter [1] Figure (6), with values of inductor's elements equals to 100μH with resistance equals to 10mΩ, Ceq capacitor equals to 0.01μF,C1 capacitor equals to 0.1μF, voltage of input source 35V and output current 1.5A for frequency 25KHz are analyzed by using MR876 diodes and IRF640 switches.

Figure (7) shows the inductor current wave and Figure (8) shows the link capacitor voltage wave (Ceq) and capacitor voltage wave C1.

Wasted energy in DC link in one period has been shown in Figure (9) it can be used for calculating the losses of DC link.

The loss amount is calculated approximately 2.75W, which confirms the calculated values by mathematical relations.

Table (2) shows the overall results of the simulation.

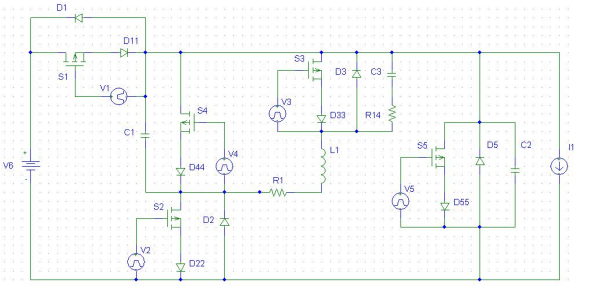

Fig. 6. Simulation of the proposed circuit

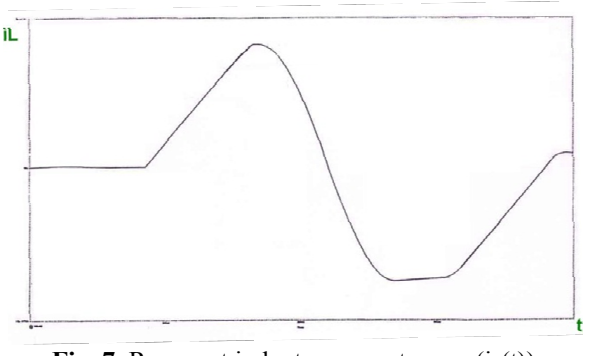

Fig. 7. Resonant inductor current wave ($i_L(t)$)

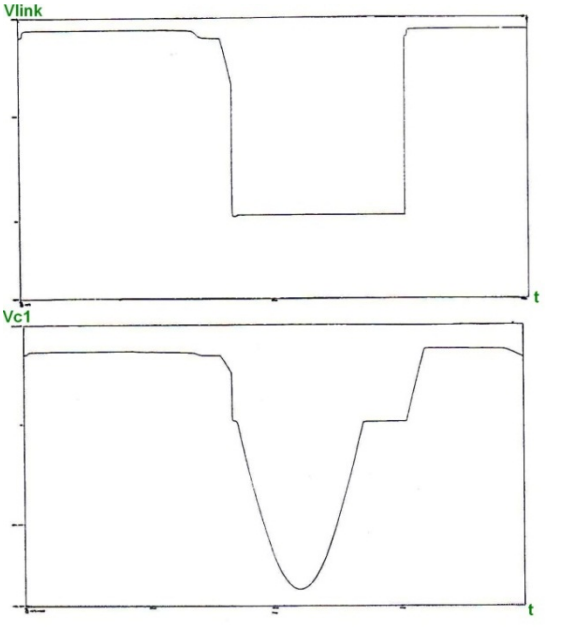

Fig. 8. Link voltage (Vlink(t)) and voltage of C1 capacitor (Vc1(t)) waves

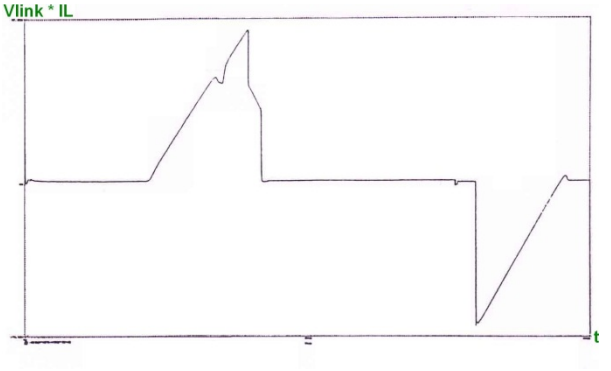

Fig. 9. Wasted energy in the proposed resonant link (Vlink(t) * $I_L(t)$)

Table 2. The results of the simulation of proposed circuit

Parts	Link losses result P (Link)	
L=100µH, RL=10mΩ, Ceq=0.01µF, C1=0.1µF, VDC=35V, Io=1.5A, fs=25KHz, Diode:MR876, Switch : IRF640	Simulation	Mathematical relations
	2.75W	2.78W

Since the changes in the resonant circuit elements, effect on the link voltage is zero and returning it to the initial state (time T) and also effect on peak of the inductor current, have been studied as follows.

By reducing the amount of L, time T will be decreased but peak of the inductor current increases, curve variations during the time T and inductor current for L values from 10µH to 100µH have been shown in Figures (10) and (11).

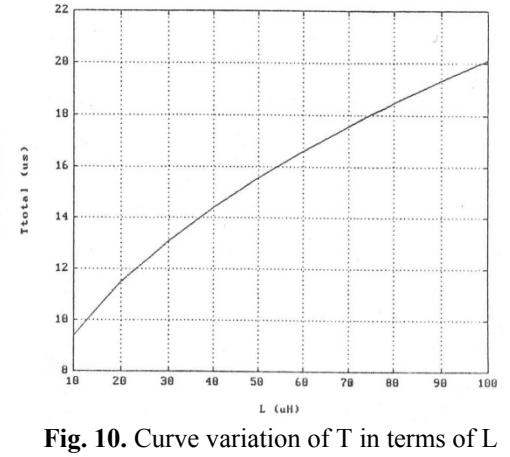

Fig. 10. Curve variation of T in terms of L

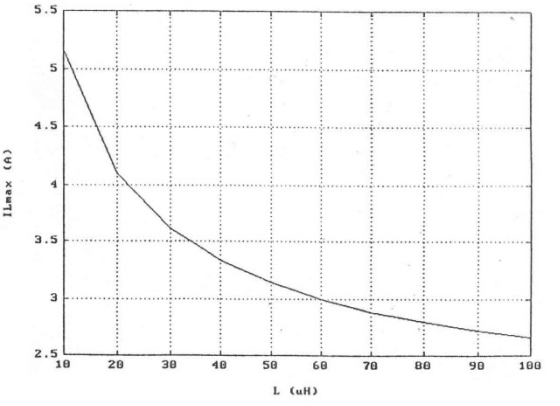

Fig. 11. Curve variation of ILmax in terms of L

Through decreasing output current, peak inductor current increases and the time T reduces. T curve and peak inductor current for values Io from 0.5A to 10A have been shown in Figures (12) and (13).

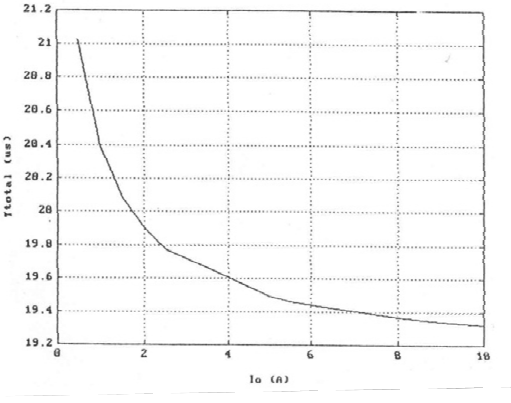

Fig. 12. T curve in terms of Io

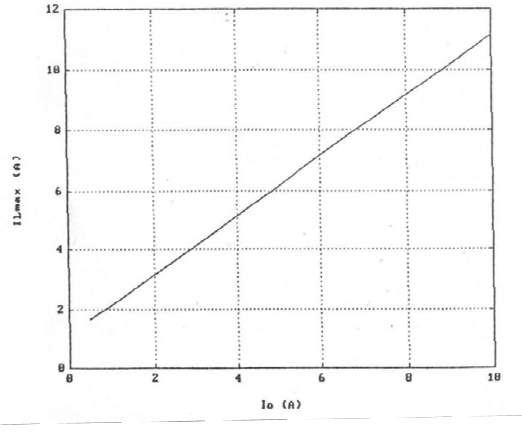

Fig. 13. ILmax curve in terms of Io

T time increase when capacitors C1 and Ceq increase and T curve in terms of changes C1 and Ceq from 0.01µF to 0.1µF have been shown in Figures (14) and (15).

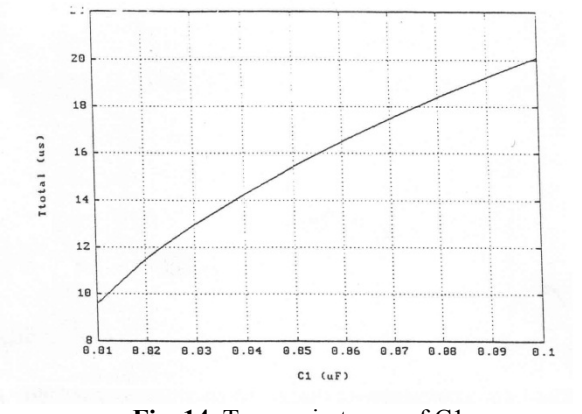

Fig. 14. T curve in terms of C1

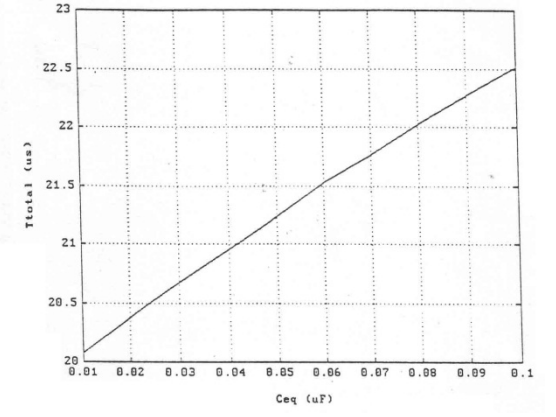

Fig. 15. T curve in terms of Ceq

8. STUDYING OF LOSSES AND SIMULATING A FEW SAMPLE QRDCLI

By using the mathematical relations governing the various functions of circuits [11], [12] and [13] with the proposed circuit and also using of computer simulation, the final results are per the Table (3).

Table 3. Compare between results

Circuit	Switches	PWM capability	P(link) Simulation	P(link) Mathematical relations	SPSS capability
[11]	4	1 range	2.36W	2.40W	Yes
[12]	4	2 range	2.14W	2.16W	No
[13]	3	1 range	2.29W	2.35W	No
Proposed	4	3 range	2.75W	2.78W	Yes

It needs to be mentioned that the inductor values, capacitors, output current, input voltage and work frequency should be as per the work Table (2).

9. CONCLUSION

Studying and simulating the inverter with introduced DC link shows that, this inverter, (in addition to the reduction of losses, which are due to the switch off), provides ZVS and ZCS conditions for turning on switches. In this inverter by using a special SPWM which has been described, quasi-resonant circuit each time link voltage is zero without any precision sensors and by simple control circuit returns to the initial free energy state. In the proposed inverter, because of high switching frequency, output voltage is with little distortion.

To calculate the total losses in QRDCLI should just obtain the conduction losses when the switches are on and the reversed parallel diodes and obtain switching losses when the switches are off and also and the resistive losses or resonant inductor. With that analogy in Table (3) which are the results of computer simulation with software PSPICE for three sample circuits and the circuit and the proposed circuit, can see these results confirm the calculated values obtained from the mathematical equations governing on the various stages of each circuit. Meantime, these results show that losses in QRDCL circuit of different circuits are almost identical and in the small amount and therefore, using of QRDCL in inverters for applications in high frequency (several tens of KHz) are suitable.

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