A Reconfigurable Hybrid Architecture for HomePNA3.1/ Ethernet MAC

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ABSTRACT:
With the growing demands of home networking, the existing networking technologies couldn't satisfy user expectations any more. Today networking technologies is interested that don't need new cable and have the high bandwidth. HomePNA (Home Phoneline Networking Alliance) is a solution. HomePNA3.0 and Ethernet was similar in MAC sublayer; hence, HomePNA3.0/Ethernet reconfigurable implementation was appeared cost-effective. But the difference between HomePNA3.1 and Ethernet increased. In this paper, we propose new reconfigurable hybrid architecture. We implement it in behavioural level using VHDL language. Our implementation was able to have HomePNA3.1 and Ethernet MACs together. Our synthesis shows that our implementation decreases number of logical element by 32%.

KEYWORDS: HomePNA, Ethernet, Home networking, Reconfigurable system design.

1. INTRODUCTION

Today, there are a lot of different technologies to build local networks, with the main one being Ethernet. Ethernet, the most common and a widely-used standard, is a wired local area network technology that ordinarily requires each computer to be equipped with an interface card, a hub or switch and also cable. However, old home cabling isn't simple. On the other hand, except wireless communication, all of networking technologies need a media. As a result, the price is growing for both network equipment and cables. However, is there another way-out, without changing requirements to the network cables?[1]-[3]

HomePNA is a solution. This technology provides the ideal support for concurrent data, voice and video services. Its advanced capabilities such as traffic management and QoS, make the delivery of IPTV, VoIP and real-time gaming applications flawless. HomePNA3.1 technologies adequately provide bandwidth inside the home. [4] However, users accustomed to use Ethernet and have no desire to change their ways, and use HomePNA. This problem can be solved by the reconfigurable device. A reconfigurable system can perform two or more functionalities; and the user can alter the functionality of the system based on the intended application. The principal benefit of the reconfigurable system is the ability to execute larger hardware designs with fewer gates and to realize the flexibility of a hardware-based solution while retaining the execution speed of a more traditional, hardware-based approach.

This paper proposes reconfigurable hybrid architecture for HomePNA3.1/Ethernet MAC that we attained by considering reconfigurability as a key criterion in hardware partitioning. So the main contributions of this research are to add reconfigurability to the parameters considered in hardware partitioning, and to propose a reconfigurable hybrid architecture that is reconfigurable for HomePNA3.1 and Ethernet functions.

Implementation of disjoint subsystems in the final reconfigurable system makes it easy and cheap for traditional Ethernet users to gradually adopt HomePNA in their homes and offices. The rest of this paper is organized as follows. In the next section, we overview related works that have been done on HomePNA and

reconfigurable system design. In section 3, we demonstrate the protocol stack of HomePNA3.1 standard and Ethernet, and we discuss their similarities and dissimilarities. Section 4 introduces our reconfigurable hybrid architecture HomePNA3.1/Ethernet. Experimental results are shown in section 5, and final section presents the conclusions.

2. RELATED WORKS

There are a lot of researches that was done on HomePNA in academia and industry and some prominent network equipment companies, such as 3Com©, manufactured products base on HomePNA standards.

In [3], we produce a HomePNA3.0/Ethernet MAC. Our prototype of HomePNA3.0/Ethernet developed in order to make it possible to explore different solutions at the level of standardization, system architecture and implementation. This prototype is implemented on an FPGA that has a scalable architecture and is easily adaptable because of its modularity. Our first achievement published in [1] and [2].

In our previous research, we design and implement HomePNA3.0. We present a new architecture because of differences between HomePNA3.0 and HomePNA3.1 that was described in next section. Originally, our last implementation couldn't use by HomePNA3.1, due to its maximum clock frequency.

Bisaglia et al. [5] analyze receiver architecture for HomePNA and equalization techniques. They in [6] propose a model for the HomePNA channel and analyze its physical layer. They concentrate on physical layer but by concerning media access control sublayer.

Chung et al. [7] present a mathematical analysis of the saturation throughput of HomePNA2 MAC. Kim et al. [8] make a similar analysis for HomePNA3.0 master-less mode. They defined saturation throughput as the maximum network throughput for a given number of nodes, when every node always has frames ready to be transmitted.

Kangude et al. [9] present an analysis of HomePNA2 MAC protocol and its collision resolution mechanism. They show that the number of slots used for collision resolution (defined by the standard) is not optimal for some scenarios. Then in [10] they suggest that the number of slots increase according to network load to increase network efficiency.

Loh et al. [11] investigate on quality and priority management in HomePNA2 link layer. In [12], Won et al. present a design and performance analysis of HomePNA2 transceiver chip circuit. In [13], Su et al. estimate the performance of home LAN using HomePNA2 station.

Similarly, reconfigurable system design has been interested recently, and there are lots of efforts on reconfigurability methodologies and partitioning methods, and some reconfigurable architecture has been proposed for specific applications using reconfigurable methodologies. For instance, Vosoughi et al. [15] presented reconfigurable hybrid hardware/software architecture for EFM/Ethernet. In [16], Sung et al. present hardware/software co-designed implementation of IEEE802.16 TDMA MAC for subscriber station. Soltani [17] proposes a new algorithm for hardware/software partitioning and evaluates it by applying it on a JPEG2000 encoder.

There are some other researches on reconfigurable system design too, but none of them investigated on Ethernet and HomePNA.

3. PROTOCOL STACK OF HOMEPNA AND ETHERNET

In this section, we describe the protocol stack of HomePNA and Ethernet, and also compare similarities and dissimilarities of them at the end.

These protocols are defined in data link layer and physical layer. The data link layer is described in more detail with Media Access Control (MAC), Logical Link Control (LLC) and Convergence sub layers. MAC is responsible for managing access to media using a media access protocol. MAC acts as an interface between the LLC and physical layer. It provides addressing and media access control mechanisms that make it possible for network nodes communicate within a multi-point network.

The Media Independent Interface (MII) is a standard interface used to connect a MAC to a physical layer chip. The MII may be used to connect either MAC to an external physical layer via a pluggable connector or a MAC chip to a physical layer chip on the same printed circuit board.

3.1. Ethernet

IEEE 802.3 describe Ethernet standard. It is the most widespread LAN technology [4].

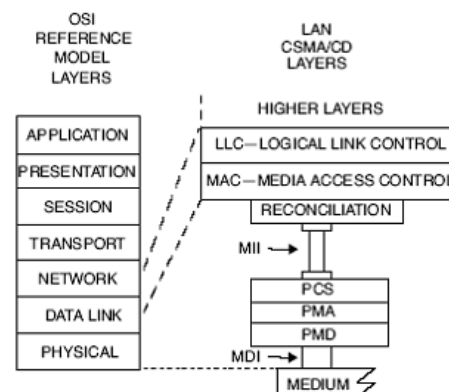Layer model specification of Ethernet was shown in Figure 1.

Fig. 1. protocol stack of Ethernet [18]

Ethernet defines a number of wiring and signaling standards for physical layer of the OSI networking model as well as a common addressing format and media access control at the data link layer. Ethernet use CSMA/CD techniques to control media access, and it doesn't have any priority for nodes to access the media [18].

CSMA/CD terminates transmission as soon as a collision is detected and reduces the probability of a second collision on retry.

All nodes respectively do below functions after collision detection.

- Continue transmission until minimum packet time to ensure all receivers detect the collision.
- Increase retransmissions counter.
- If the maximum number of transmission attempts reached, then node aborts transmission.
- Calculate and wait random back off period based Exponential back off algorithm.
- Retransmit packet.

Ethernet use Binary Exponential back-off algorithm for resolve collision. In Exponential back off algorithm, the retransmission has delayed until an amount of time derived from the slot time and the number of attempts to retransmit. For example, after c collisions, a random number of slot times between and 2^c are chosen. Thus, the number of retransmission attempts increases, delay increases exponentially too [18].

3.2. Protocol stack of HomePNA

In mid-90s the Tut Systems© offered its own technology for transferring data on a phone line that knew as HomePNA1 [19].

The HomePNA phrase refers to the industry group that agrees on specifications for home LAN technology using regular phone wiring. Founders of HomePNA included AMD©, Intel©, Epigram©, Conexant©, among others.

The HomePNA technology is also commonly referred to HPNA, HomePNA, Home Phoneline Networking or Phoneline Networking Transceiver or PNT.

The key advantage of HomePNA technology was its ability to function over unstructured wiring, i.e. any topology or type of wiring. For example, Figure 2 could be the topology of home phone line [19].
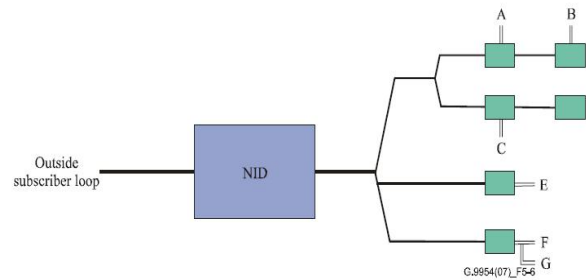

Fig. 2. unstructured wiring of HomePNA

The HomePNA2 specification (with 10Mbps bandwidth) has G.9951 ITU Recommendation [20]. The HomePNA3.0 specification (with 128Mbps bandwidth) has an ITU standard that was known as G.9954 Recommendation [21].

HomePNA3.1 with 320Mbps bandwidth was standardized by ITU too; this standard was named G.9954v2 Recommendation). Protocol stack of HomePNA3.1 was depicted in Figure 3.
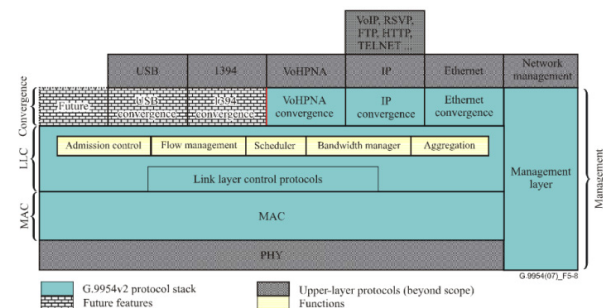

Fig. 3. protocol stack of HomePNA3.1 [4]

2.1.1. physical layer

Physical layer of HomePNA3.1 composed of two physical layer types, where the first type is specified for phoneline network, and the other type is specified for a coaxial cable-based network. Each of them maintains compatibility with existing services on the same network [22].

The physical layer over phoneline maintains backward compatibility with HomePNA3.0 using spectral mode A. It is also compatible with other phoneline services such as POTS, V.90, ISDN and HomePNA2. Frequency used by phoneline technologies demonstrated in Figure 4 [22].
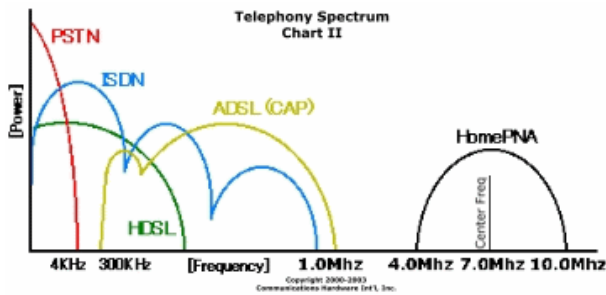
Fig. 4. Frequency used by phone line's technologies[3]

The HomePNA3.1 nodes use the same frequency band for the phoneline and coaxial line. This frequency band is above digital subscriber line signals on phoneline channels and is below television channels on coaxial cable [22].

2.2.1.Data link layer

As mentioned above, data link layer constitutes from three sublayers.

The HomePNA3.1 MAC uses a resource reservation scheme to guarantee media resources for network devices and to prevent collisions between multiple network devices contending for access to the media.

In other words, the media access method of a HomePNA3.1 devices depend on the existence of a device on the network that was able to perform the role of network master. A master-capable device is a regular HomePNA3.1 device that also supports the functional role of master [3].

The master is responsible for controlling media access by planning media access timing on the network and periodically advertising the media access plan to all devices. This periodic timing is referred to a MAC cycle. HomePNA3.1 nodes synchronize themselves by the periodic MAC cycle and their transmissions time that was described in the media access plan (MAP). The MAP specifies media access timing of a network. Media access time is broken up into transmission opportunities (TXOP) with a specified length. TXOPs are allocated to specific network devices in accordance with their resource demands. Media access timing is planned to normally avoid collisions. However, collisions may occur within TXOPs that are designated as contention periods. Collisions are similarly resolved using the master-less collision resolution method [3].

If there is no master node, HomePNA3.1 node use CSMA/CD's like for access to media; but this media access mechanism has a priority mechanism that is defined to allow higher layers to label outgoing frames with priority value, and guarantee that those frames will have preferential access to the media over lower priority frame. The priority slots are numbered in decreasing priority, with the highest priority starting at level 7. Higher priority transmissions commence

transmission in earlier slots and acquire the media without contending with the lower priority traffic [4].

Two or more stations may begin transmitting in the same priority slot, in this situation collision occurs. Generally, in HomePNA3.1, collisions are between frames at the same priority level. After a collision, a distributed collision resolution algorithm is run. This mechanism differs from the Binary Exponential back-off algorithm used in Ethernet. It uses some signal slots and counters who were described in standard. This mechanism is more complex than Ethernet collision resolution mechanism [3].

LLC is responsible for performing link functions control. Particularly, it is responsible for managing information concerning network connections, for enforcing quality of Service (QoS) constraints [3].

Convergence sublayer is the responsible to translate the native protocol into the underlying framework. It may use protocol or configuration specific information to perform the translation [3].

3.3. similarities and dissimilarities

In this subsection, we will demonstrate similarities and dissimilarities between HomePNA and Ethernet at first and then HomePNA3.0 and HomePNA3.1.

3.1.1.HomePNA versus Ethernet

Media access mechanism of Ethernet and master-less HomePNA is the most significant similarity of HomePNA3.1 and Ethernet. But HomePNA3.1 protocol stack supports synchronous collision-free media access method too [22].

Table 1 shows some important similarities and dissimilarities of these two protocols.

Table 1. Similarities and dissimilarities

	Ethernet	HomePNA
Interface to lower layer	MII	MII
Priority on access to media	No	Yes
Collision resolution	Binary Exponential back-off algorithm	Slotted back-off
CRC	CRC16 and CRC32	CRC32
Media access mechanism	CSMA/CD	like CSMA/CD but with priority in master-less mode
		Scheduled in master-controlled mode
Frame format	Figure 5 –a	Figure 5 –b

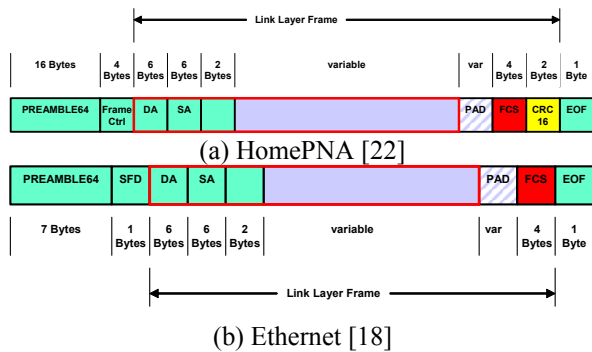(a) HomePNA [22]

(b) Ethernet [18]

Fig. 5. HomePNA and Ethernet frame format

Of course, there are some other dissimilarities like deference between parameter (such as minimum frame length and Inter Frame Gap (IFG) and etc.), deference between preamble format and etc.

Similarities between HomePNA3.0 and Ethernet had been used to reach a reconfigurable architecture for HomePNA3.0 and Ethernet. In following section, we discuss the difference between HomePNA3.1 and HomePNA3.0, that was caused change our earlier architecture and present architecture.

3.2.1. HomePNA3.0 versus HomePNA3.1

In this subsection, we study dissimilarities between HomePNA3.0 and HomePNA3.1.

HomePNA3.1 nodes must be backward compatible with HomePNA3.0 and HomePNA2, i.e. a HomePNA3.1 node must act as HomePNA3.0 or HomePNA2 in a network with HomePNA3.0/HomePNA2 nodes.

Most important difference between HomePNA3.0 and HomePNA3.1 may be bandwidth. As mentioned above HomePNA3.0 has 100Mbps bandwidth but HomePNA3.1 has 320Mbps bandwidth.

MII transfers 4 bit data to the MAC in each transmission. Therefore, therefore MAC should work with 1/4 transmission bit rate. This implies interface clocks to be fixed frequency of 25MHz ±100 ppm for HomePNA3.0 and 80MHz ±100 ppm for HomePNA3.1. However, maximum clock rate of our last implementation to be fixed frequency of 25MHz. We couldn't use that architecture and had to present a new architecture.

On the other hand, HomePNA3.1work on two physical layers and when operating on the coaxial line, HomePNA3.1 nodes only use the master-controlled mode which can be more than 90% efficient and increasing the bit rate available for the users.

Another difference between them is their state-transition diagram. Figure 6 (a),(b) describe the state-transition diagram of them.
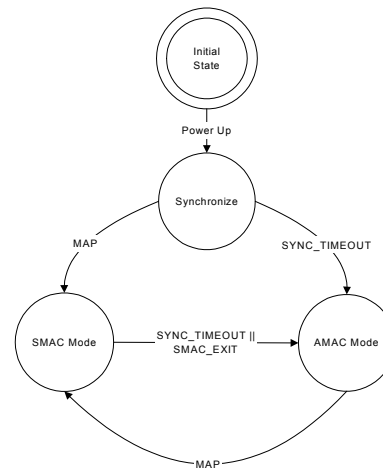
a) HomePNA3.0 modes of operation – State diagram [21]
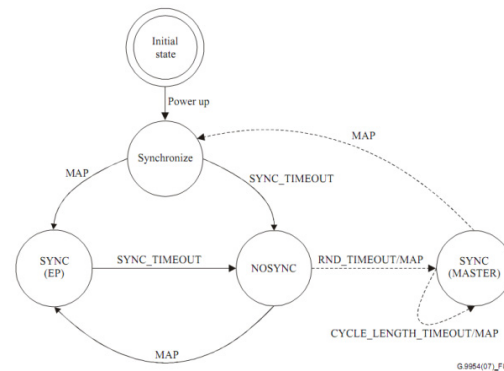
b) HomePNA3.1 modes of operation – State diagram [22]

Fig. 6. HomePNA3.0 and HomePNA3.1 state diagrams

Of course, there is another difference between them that affect on LLC, and some other differences that are partial and must be considered in implementation.

4. PROPOSED HYBRID ARCHITECTURE

In this section, we describe our proposed hybrid architecture for a reconfigurable MAC which can function as either an ordinary Ethernet network MAC or a HomePNA3.1 MAC.

For implementing a system on hardware, first system was exactly described and its component and their interfaces were determined. So before implementing a system, we have to present architecture of a system. Architecture is selecting and interconnecting hardware components to create a system that meets functional, performance and cost goals and the formal modeling of that system. We have to present architecture for our system. Our criteria to create an appropriate architecture are:

- Simplicity
- Completeness
- Cost effective

- Low complexity

One way for producing a reconfigurable system separately implement two systems, but it is expensive. Because some share parts will be repeated. In providing our architecture, we have taken advantage of hardware partitioning techniques.

Hardware partitioning is one of the most important elements of hardware design; it has a significant effect performance and cost final system. Inputs of the hardware partitioning scheme are system functionality specification. In the process of partitioning the system partitioned to hardware and software blocks, and many parameters must be considered. These parameters include speed, power consumption, parallelism, reliability, flexibility, cost, time-to-develop, and time-to-market [17].

In this research, we add reconfigurability of the system as a new parameter to the parameters set that must be considered in architecture design.

Usually, a reconfigurable device consists of a constant part (some parts of its algorithm that is never changed), which is coupled to a reconfigurable part. The ability of changing the functionality of the circuit cause we have a flexible system. The structure of the reconfigurable part can be changed via a control unit, respect to applications [14].

As an example, HomePNA3.1 and Ethernet, which had common characteristics, can be implemented as two functions of a reconfigurable system.

Our policy in partitioning is to increase the hardware implementation weight of the shared blocks and to decrease the weight of other (not common) blocks. The main reason is to make the design more flexible and to achieve easy and cheap reconfigurability.

As Figure 7 shows, presented architecture is formed by five basic modules and some interface signals.

These modules do different function based on mode of operation. MAC management module controls all modules and makes some signals to control them.

Since full duplex, Ethernet may be active on both sending and receiving paths, we used two CRC&FCS generators in transmitter and receiver paths and two memories were placed in two paths. However, maximum memory size was considered 1.5kB because maximum frame size is 1500 Bytes. However, memories' functionalities don't depend on mode of operation. They store received packet and packet that must be transmitted. These memories were controlled by LLC and MAC management module.
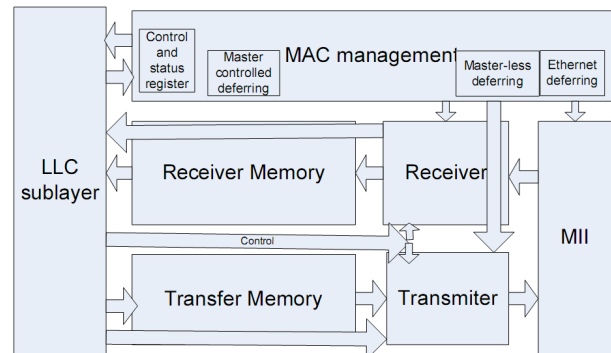
In continue each module is illustrated.

Fig. 7. Presented reconfigurable hybrid architecture of HomePNA3.1 and Ethernet

4.1. Receiver

Frames are received from MII by Receiver module. It put them into Receiver Memory. This module does below function in addition to its main function too. However, these functions should do respect to modes of operation (Ethernet or HomePNA).

- Module's frequency must operate at least on 80MHz.
- Activate rx_finished signal when receive finished.
- Receive frame from MII interface and based on frame length.
- Detach various fields of the frame depend on mode of operation.
- Specify the PAD and detach PAD depend on the frame format (Ethernet and HomePNA).
- Error detection with produce and check CRC & FCS.
- Receiving jam or backoff20 signal and change BL and MBL counter who was used by HomePNA.
- Check the receiver address (address may be multicast or broadcast.)
- Check rx_dv and CRS on reception.

We implement this module by using components that were shown in Figure 8. Each component does some of the above function base on mode of operation. For example, when the device is on HomePNA mode generates and check both CRC16 and FCS (CRC32) simultaneously. But on Ethernet mode, only generates and checks CRC16. They were controlled by signals that were generated by MAC management module.
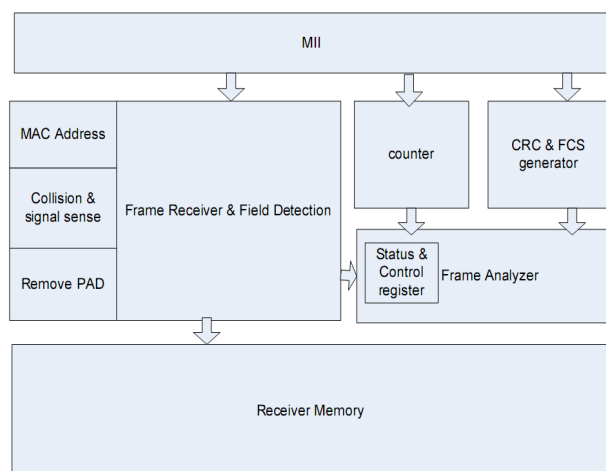
Fig. 8. Receiver architecture

Some data link layer protocols (such as LARQ: Limited automatic repeat request protocol, Frame bursting protocol) need to receive frames with error, so they are passed to LLC but CRC_check_error or FCS_check_error was activated.

4.2. Transmitter

A station shall defer for a quiet period on the media (no other station is transmitting) and waits for the arrival of a TXOP assigned to it. This function performs by MAC management module. MAC management module activate start_transmit signal at the appropriate time.

Transmitter gets the frame from Transmitter memory. Then it sends it to MII. This module does below functions in addition to its main function. However, these functions should do respect to the modes of operation.

- Check start_transmit before sending.
- Module's frequency must at least be 80MHz.
- Activate tx_finished signal when transmission finished.
- Attach various fields of the frame depend on mode of operation and frame length field.
- Specify the PAD and attach PAD.
- Produce CRC or FCS of a frame.
- Sending jam or backoff20.

We implement this module by using components that were shown in Figure 9. Each component does some of the above function base on mode of operation. They were controlled by signals that were generated by MAC management module.
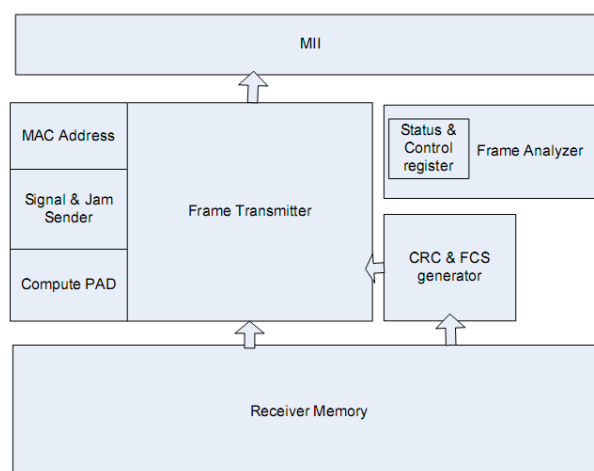

Fig. 9. Transmitter architecture

4.3. MAC management module

MAC management module is responsible to control all other modules. This module consists of four components. It does deferring and implements collision resolution mechanism.

Our implementation must act as master-controlled HomePNA3.1, master-less HomePNA3.1 and Ethernet, so there are three deferring component in MAC management module. These components control media access and MAC management module enables one of them based on mode of operation.

In master-controlled mode, each node can send data on its TXOP. LLC studies MAP frame and generate TXOP_sig. TXOP set on begin and clear on end of a node TXOP. The length of TXOP_sig must equal to frame length and frames, which need more time to transmit must not be sent to MAC. Master-controlled deferring component generate appropriate signal and control transmitter or receiver in this mode.

In master-less mode, frames are transmitted inside a specific priority slot. If collision occurs, nodes execute a collision resolution mechanism that was described by standard. Master-less deferring component generate appropriate signal and control transmitter or receiver in this mode.

In the Ethernet mode, nodes transmit each time media is empty and Exponential back off algorithm is used to resolve a collision. Ethernet deferring component generate appropriate signal and control transmitter or receiver in this mode.

We implement each of these components by using a Finite State Machine (FSM).

5. EXPERIMENTAL RESULTS

We implement our proposed architecture by VHDL and simulate in Modelsim using several test-benches designed to validate system functionality. The correctness of the developed MAC functions was validated with twice the method:

- Loop back test: in this approach output of MAC is connected to its input. Then MAC sends frames and simultaneously receives them on its input.
- Connection of two MAC: In this approach, two MAC connect together that one sends frames and other receives them. Collision, transmission error and link errors (ex. disconnection) could be simulated in this method.

Our simulations show that the proposed architecture is a viable solution to be implemented and used by HomePNA and Ethernet. It fulfills the objectives of HomePNA and Ethernet. 100Mbps bit rate is achieved on the Ethernet, also 320Mbps bit rate is achieved on the HomePNA3.1, and it supports simultaneous transmission and reception without interference.

Figure 10-13 shows some of our simulations result.

Then, we synthesize our implementation by using Quartus II on a chip from Altera© Company and Startix family. Table 2 shows our result.

The first row of table 2 shows the number of Logical Element (LE) in hardware implementation of Ethernet MAC. We use an open Ethernet MAC IP core that has been implemented in Verilog [23].

HomePNA was previously implemented by industrial company, but they don't publish information about their implementation. So we don't know the real number of LE of a HomePNA MAC. However, HomePNA is more complicated than Ethernet, thus we estimate its implementation at least need as Ethernet LE. The next row of table 2 shows our estimated number of LE for HomePNA.

HomePNA3.1/Ethernet coupled system haven't presented yet, so HomePNA3.1/Ethernet coupled system need 2156+2156=4312 LE. Since there wasn't any HomePNA3.1/Ethernet reconfigurable implementation, we compare our implementation with HomePNA3.1 and Ethernet separately.

The 3rd row of table 2 shows number of LE for our architecture.

Thus implementation of the proposed hybrid reconfigurable architecture will reduce the silicon area by (4312-2852)/4312*100%=33.7% when compared to the implementation of a hardware system that renders the same functionalities (both HomePNA3.1 and Ethernet).

The reconfigurable hybrid architecture proposed in this paper renders the flexibility to statically reconfigure the system to one of the alternate functions. In addition, the cost of implementing our proposed solution is low due to its smaller silicon area.

On the other hand, Comparing our reconfigurable MAC and Ethernet MAC shows the number of LE increased by (2852-2156)/2154*100%=32%.

Thus, we propose Ethernet NIC manufactories implement reconfigurable HomePNA3.1/Ethernet NICs instead pure Ethernet NICs.

Cost of each part of a NIC isn't available. Therefore, w can t say i is how much more expensive.

The fourth row of table 2 shows number of LE of our last architecture. So, our new architecture needs (2852-2561)/2561*100%=11% more LE comparing with our last implementation, but this new implementation can achieve 320Mbps bit rate and operate on 80MHz.

Table 2. Number of gate of hardware implementation

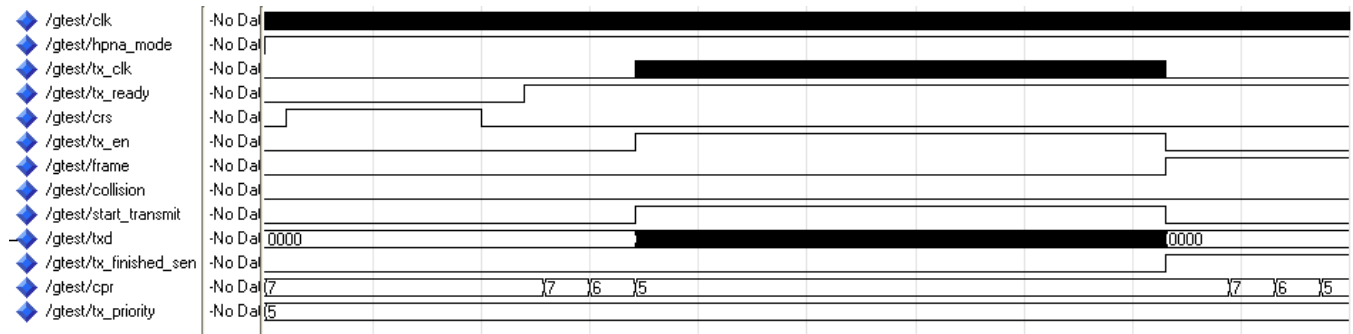| Hardware Implementation	Number of LE
Ethernet MAC IP core	2156
Estimated HomePNA MAC core	2156
Our Reconfigurable Ethernet/HomePNA3.1 MAC	2852
Our last Reconfigurable Ethernet/HomePNA3.0 MAC	2561

Fig. 10. Master-less mode of HomePNA3.1 of implemented architecture
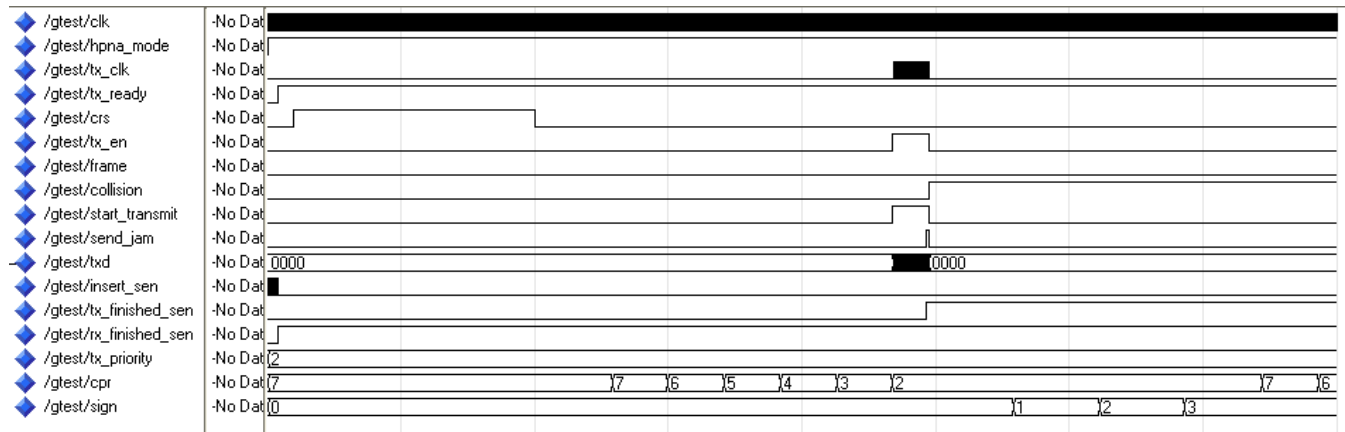
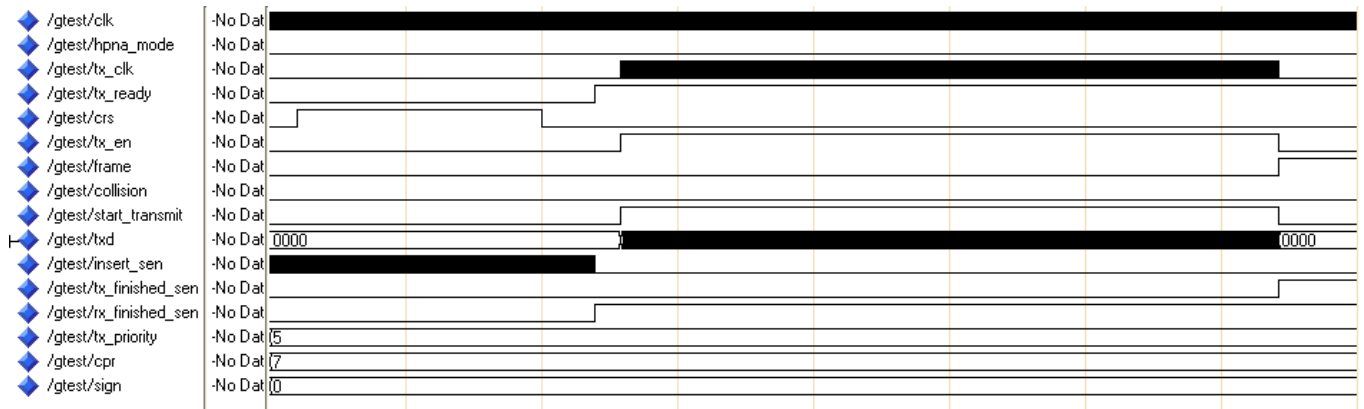**Fig. 11.** Master-less mode of HomePNA3.1 of implemented architecture

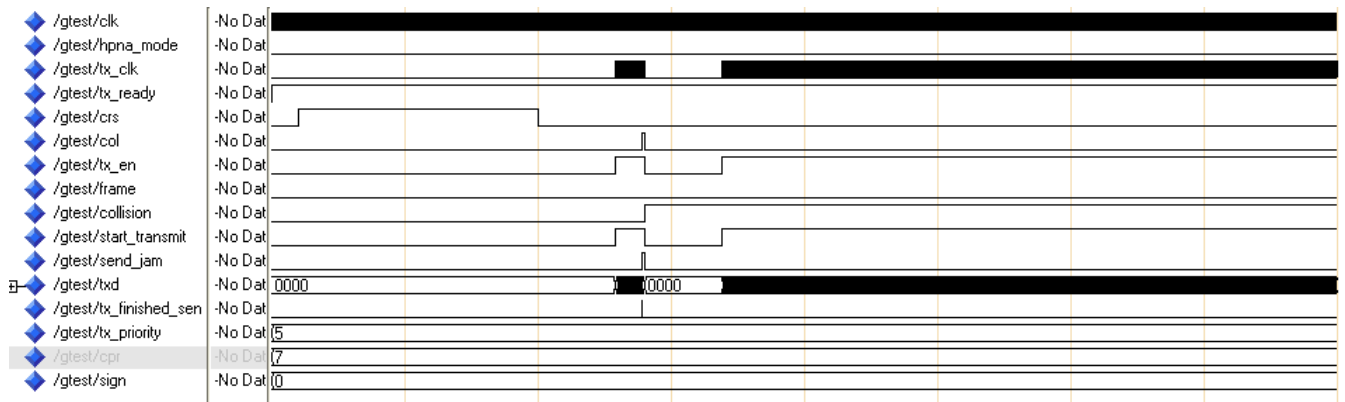**Fig. 12.** Ethernet mode of implemented architecture

Fig. 13. Conflict resolution in Ethernet mode of implemented architecture

6. CONCLUSIONS

In this paper, architecture for a HomePNA3.1/Ethernet reconfigurable MAC is proposed. This architecture renders a high measure of flexibility and possibility of gradual adoption of HomePNA3.1 to users. In addition, our experiments show that 33.7% reduction in area was achieved using the proposed hardware architecture instead of a total hardware implementation of HomePNA3.1/Ethernet double-purpose device.

The reconfigurable hybrid architecture for these MACs leads to 32% area overhead only in compare to independent implementation of Ethernet MAC.

The proposed architecture meets all the requirement of HomePNA3.1 and Ethernet. It seems that it is reasonable to replace the Ethernet chip with the proposed chip on the Ethernet NICs to have ability use both Ethernet and HomePNA3.1 optionally.

However, maximum achievable clock frequency of our implementation is 80MHz, and we can achieve

320Mbps bit rate, and it can't use for 1Gbps Ethernet.

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