A New Topology of Three-Phase Four-Wire UPQC with a Simplified Control Algorithm

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ABSTRACT:
In this paper, a simplified control algorithm based on unit vector template generation (UVTG) is proposed for a star-delta supported three-phase four-wire (3P-4W) unified power quality conditioner (UPQC) topology for the improvement of different power quality problems. Different topologies reported in literature for 3P-4W UPQC use active compensation for the mitigation of source neutral current along with other power quality (PQ) problems, while the uses of passive elements for the mitigation of source neutral current are advantageous over the active compensation due to ruggedness and less complexity of control. Hence, in this paper a star-delta transformer is connected in shunt near the load for mitigation of source neutral current, while three-leg voltage source inverters (VSIs) based shunt and series active power filters (APFs) of 3P-4W UPQC mitigate the current and voltage based distortions, respectively. A simple control algorithm based on Unit Vector Template Generation (UVTG) is used as a control strategy of UPQC for mitigation of different PQ problems. In this control scheme, the current/voltage control is applied over the fundamental supply currents/load voltages instead of fast changing APFs currents/voltages, thereby reducing the effects of computational delay and the required sensors. The performance of the proposed topology of UPQC is analyzed through simulations results using MATLAB software with its Simulink and Power System Block set toolboxes.

KEYWORDS: Power-factor correction, Load balancing, UPQC, Voltage and Current harmonics, Neutral current mitigation, Star-delta transformer.

1. INTRODUCTION

In the deregulated power market, adherence to different power quality standards [1-2] laid down by different agencies has become a figure of merit for the utilities. On the other hand three-phase four-wire distribution systems are facing severe PQ problems. Some of these are high reactive power burden, voltage and current harmonics, poor power-factor, voltage sag, swells and voltage dip etc. Different devices such as rectifiers, inverters, adjustable speed drives, computer power supplies, furnaces and traction drives lead to non-linear current waveforms and hence degrade the quality of power. The quality degradation leads to low power-factor, low efficiency, overheating of transformers and so on [3]. In addition to this, the load on a 3P-4W distribution system hardly found balanced. Because of this there is an excessive neutral current of fundamental and as well harmonic frequencies in the neutral conductor [4-5].

For the mitigation of neutral current along with other power quality compensations, different topologies of UPQC reported in literature are three-leg VSI with split capacitor [7], three-single phase VSI [11], four-leg VSI [8],[11-12], current source inverter [13] etc. Out of these proposed topologies, the four-leg VSI topology is most popular, but has the disadvantages of greater number of semiconductor switches, complexity of control, etc.

The reported topologies of 3P-4W UPQC [7-13] use active compensation of source neutral current, while the uses of passive elements for the mitigation of source neutral current are advantageous over the active compensation due to ruggedness and less complexity of control. Hence, in this paper a star-delta supported 3P-4W UPQC is proposed for the mitigation of different PQ problems. The delta connected secondary of a star-delta transformer provides a circulating path to the zero sequence current (i_o) in case of unbalanced load and hence the supply neutral current is reduced to zero. Moreover, star-delta supported 3P-4W UPQC may be realized using readily available three-leg VSIs.

In addition to this, in a transformer supported 3P-4W UPQC no extra control is required for the mitigation of source neutral current; hence the control

algorithms of 3P-3W UPQC are equally effective for 3P-4W UPQC without any modification. Moreover, the shunt APF neutral current or load neutral current are not sensed, hence required numbers of current sensors are reduced. The most important feature of a transformer supported 3P-4W UPQC lies in its simplicity. A transformer supported 3P-4W UPQC may be realized by simply clubbing a transformer in shunt near the load to a 3P-3W UPQC.

There are many control strategies reported in the literature to determine the reference values of the voltage and the current of three-phase four-wire UPQC, the most common are the p-q-r theory [7], modified single-phase p-q theory [8], synchronous reference frame (SRF) theory [9], symmetrical component transformation [10], and unit vector template generation (UVTG) [11] etc. Apart from this one cycle control (OCC) [12] (without reference calculation) is also used for the control of 3P-4W UPQC. In this paper a simplified control algorithm based UVTG is used as a control scheme for the UPQC system. In this control scheme, the current/voltage control is applied over the fundamental supply currents/load voltages instead of fast changing APFs currents/voltages, thereby reducing the effect of computational delay and the required sensors.

2. STATE OF THE ART

The different topologies reported in literature of three-phase four-wire UPQC [7-13] use active compensation for the mitigation of source neutral current along with other PQ problems. For the mitigation of source neutral current, the uses of passive elements are advantageous over the active compensation due to ruggedness and less complexity. There are many techniques proposed for the compensation of neutral current using star-delta transformer in a three-phase four-wire distribution system and some of these have been patented [14-17].

The application of star-delta transformer along with an APF is also used for harmonic current reduction in the neutral conductor [16]. A filter employing three single-phase transformers with a capacitor has been used for removing harmonic current from the neutral conductor and has been patented [14]. Another scheme by providing a six-phase system, with the help of two transformers connected in anti-phase has been reported for canceling third harmonic current in neutral conductor [15]. The star-delta transformer along with a diode rectifier and a half-bridge PWM inverter is also reported for the compensation of neutral current [17].

For the mitigation of source neutral current along with other current based distortions, the integration of readily available three-leg VSI with star-delta transformer has been reported in literature for 3P-4W DSTATCOM [6]. Unfortunately, for the mitigation of neutral current the performance of the star-delta transformers is affected to an extent under distorted or unbalanced source voltages, which is very common in practice. The UPQC is one of the key CPDs, which takes care of both voltage and current based distortions simultaneously. Hence, for neutral current mitigation the integration of star-delta transformer with UPQC is more justified. In this paper, a simple star-delta configuration is utilized for the mitigation of source neutral current, while other options such as zig-zag transformer or T-connected transformer require specially designed transformers.

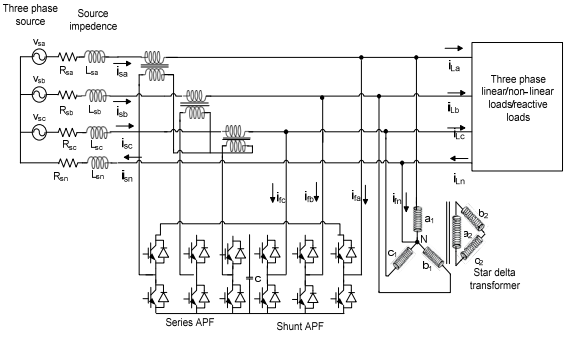

Fig. 1. Detailed configuration of proposed 3P-4W UPQC

3. SYSTEM CONFIGURATION AND DESIGN

Fig. 1 shows a 3P-4W UPQC topology, which is feeding a combination of linear and non-linear unbalanced load. The series and shunt APFs are realized using two readily available three-leg VSIs. The dc links of both APFs are connected to a common dc link capacitor. The series APF is connected between the supply and load terminals using three single phase transformers with turn's ratio of 5:1. The primary winding of these transformer are star connected and the secondary windings are connected in series with the three-phase supply. In addition to provide the required injecting voltages, these transformers are used to filter the switching ripple content in the series APF. A small capacity rated R-C filter is connected in parallel with the secondary of each series transformer to eliminate the high switching ripple content in the series APF injected voltage. The voltage source inverters for both the APFs are implemented with Insulated gate Bipolar Transistors (IGBTs). In Fig.1 ($i_{sa,}$ i_{sb} , i_{sc}), ($i_{la,}$ i_{lb} , i_{lc}) and ($i_{fa,}$ i_{fb} , $i_{fc,}$) represent the source currents, load currents and shunt APF currents in phase a, b and c respectively. The source neutral current, load neutral current and neutral current of the additional connected transformers are represented by i_{sn}, i_{ln} and i_{Tn}, respectively. The injected voltages by the series APF in phase a, b and c is represented by v_{inja}, v_{injb} and v_{injc}, respectively.

In this topology, a star-delta transformer is connected in shunt near the load for the mitigation of

the source neutral current. The delta connected secondary provides a circulating path to the zero sequence current (i_o) in case of unbalanced load and hence the supply neutral current is reduced to zero. The load under consideration is a combination of linear and non-linear load. Two single-phase R-L loads are taken as unbalanced linear load, where as a three-phase diode bridge rectifier with a resistive load on dc side is considered as a non-linear load. The values of the circuit parameters and load under consideration are given in Appendix. The selection criteria of interfacing inductor, DC capacitor, ripple filter and star-delta transformer is given in the following section.

3.1. DC Capacitor voltage

The value of the common link DC bus voltage of back to back connected VSIs of the UPQC depends on the instantaneous energy available to the UPQC [18]. For a VSI the DC link voltage is defined as

$$V_{dc}=\frac{2\sqrt{2}V_{LL}}{\sqrt{3}m} \quad (1)$$

where m is the modulation index and V_{LL} is the ac line out voltage of UPQC. Considering modulation index as 1 and for line to line voltage (V_{LL} =415 V), the V_{dc} obtained is 677.69 V and is selected as 700 V.

3.2. DC Bus Capacitor

The value of DC capacitor (C_{dc}) of back to back connected VSIs of the UPQC depends on the change of DC voltage during increase and decrease of the load. Using the principle of energy conservation, the equation [18] for C_{dc} is as follows

$$\frac{1}{2}C_{dc}\left[\left(V_{dc}^{2}\right)-\left(V_{dc1}^{2}\right)\right]=3V\left(\alpha I\right)t \quad (2)$$

where V_{dc} is the reference dc voltage and V_{dc1} is the minimum voltage level of dc bus, α is the overloading factor, V is the phase voltage, I is the phase current, and t is the time by which the DC bus voltage is to be recovered.

Considering the minimum voltage level of DC the bus, V_{dc1}=690 V, V_{dc}=700 V, V=415/sqrt (3) =239.60 V, I=25.40 A, t=350μs, α=1.2, the calculated value of C_{dc} is 2340μF. Hence C_{dc} is selected as 3000 μF.

3.3. AC Inductors

The selection of the ac inductance (L_f) of VSI depends on the current ripple $i_{cr,p-p}$, switching frequency f_s, DC bus voltage (V_{dc}), and L_f is given as [18]

$$L_f=\frac{\sqrt{3}mV_{dc}}{12\,\alpha\, f_s\, i_{cr(p-p)}} \quad (3)$$

where m is the modulation index and α is the overload factor. Considering, $i_{cr,p-p}$=2.5%, f_s=10 KHz, m=1,V_{dc}=700 V, α=1.2, the L_f value is calculated to be 4.88 mH. A round-off value of L_f of 5 mH is selected in this work.

3.4. Ripple Filter

A low-pass first-order filter at half the switching frequency is used to filter the high-witching frequency noise from the injected voltage of series APF. Considering a low impedance of 8.1Ω for the harmonic voltage at half the switching frequency 10 KHz /2=5 KHz, the ripple filter capacitor is designed as C_f =5μF. A series resistance (R_f) of 7 Ω is included in series with the capacitor (C_f). The impedance is found to be 638Ω at fundamental frequency, which is sufficiently large, and, hence, the ripple filter draws negligible fundamental current.

3.5. Design of Star-delta transformer [6]

Fig. 2(a) shows the connection diagram of star–delta transformer and phasor diagram of the secondary voltages are shown in Fig. 2 (b). The delta connected secondary provides a circulating path to the zero sequence current (i_o) in case of unbalanced load and hence the supply neutral current is reduced to zero. The current rating of a star-delta transformer depends on the zero sequence circulating current in the load and the neutral current to be compensated. For a line to line voltage of 415 V, primary winding phase voltage of star connected transformer is

$$V_a=\frac{V_{LL}}{\sqrt{3}}=\frac{415}{\sqrt{3}}=239.60V \quad (4)$$

Hence, a 240 V winding is selected in the star-delta transformer. In the proposed UPQC system, three single-phase transformers with turn's ratio 1:1 of 5 KVA, 240V/240 V are selected for neutral current compensation.

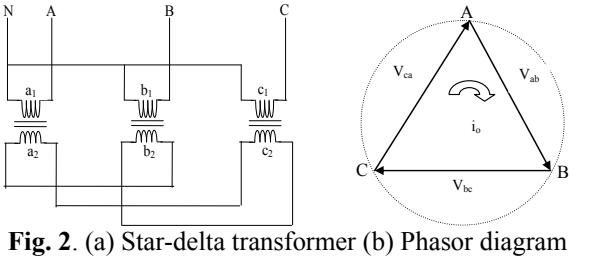

Fig. 2. (a) Star-delta transformer (b) Phasor diagram

4. CONTROL SCHEME OF SERIES APF

A simple control algorithm based on UVTG is used to control the series APF of proposed topology. The series is controlled in such a way that it injects voltages (v_{fa}, v_{fb} and v_{fc}), which cancel outs the distortions present in the supply voltages (v_{sa}, v_{sb} and v_{sc}), thus making the voltages at PCC (v_{la}, v_{lb} and v_{lc}) perfectly sinusoidal with the desired amplitude. In other words, the sum of supply voltage and the injected series filter voltage makes the desired voltage at the load terminals.

The control strategy for the series APF is shown in Fig. 3. Three-phase distorted supply voltages are sensed and given to PLL which generates two quadrature unit vectors (sin*wt,*coswt). The in-phase sine and cosine outputs from the PLL are used to compute the supply in phase,120^o displaced three unit vectors (u_a ,u_b u_c) using eqn.(5) as:

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix} \quad (5)$$

The computed three in-phase unit vectors then multiplied with the desired peak value of the PCC phase voltage (V^*_{lm}), which becomes the three-phase reference PCC voltages as:

$$\begin{bmatrix} v^*_{la} \\ v^*_{lb} \\ v^*_{lc} \end{bmatrix} = V^*_{lm} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad (6)$$

The desired peak value of the PCC voltage under consideration is 338V (=415sqrt (2)/sqrt(3)). The computed voltages from reference voltages from eqn. (2) are then given to the hysteresis voltage controller along with the sensed three phase PCC voltages ($v_{la,}$ v_{lb} and v_{lc}). The output of the hysteresis controller is switching signals to the six switches of the VSI of series APF. The hysteresis controller generates the switching signals such that the voltage at PCC becomes the desired sinusoidal reference voltage. Therefore, the injected voltage across the series transformer through the ripple filter cancels out the harmonics present in the supply voltage.

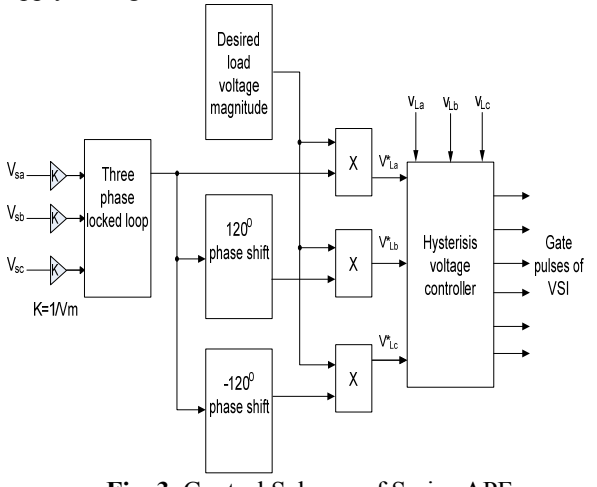

Fig. 3. Control Scheme of Series APF

5. CONTROL SCHEME OF SHUNT APF

The control algorithm for shunt APF consists of the generation of three-phase reference supply currents ($i^*_{sa,}$ i^*_{sb} and i^*_{sc}) and it is depicted in Fig.4. This algorithm uses supply in-phase; 120^o displaced three unit vectors computed in eqn. (3). The amplitude of the reference supply current (I^*_{sp}) is computed from the comparison of average and the reference value of the dc bus voltage of the back to back connected VSIs results in voltage error, which is fed to a proportional integral (PI) controller. The out put of the PI controller is taken as the reference amplitude (I^*_{sp}) of the supply currents. The three in-phase reference supply currents are computed by multiplying their amplitude (I^*_{sp}) and in-phase unit current vectors as:

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = I^*_{sp} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad (7)$$

The computed three-phase supply reference currents are compared with the sensed supply currents and are given to a hysteresis current controller to generate the switching signals to the switches of the shunt APF which makes the supply currents fallow its reference values. In this control scheme, the current control is applied over the fundamental supply currents instead of the fast changing APF currents, thereby reducing the computational delay and number of required sensor. In addition to this, no extra control is required for the mitigation of source neutral current.

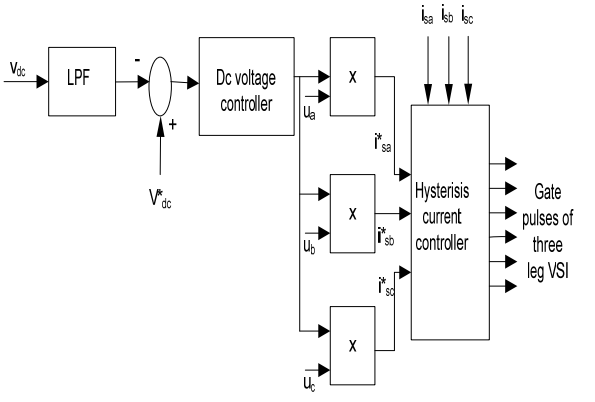

Fig. 4. Control Scheme of Shunt APF

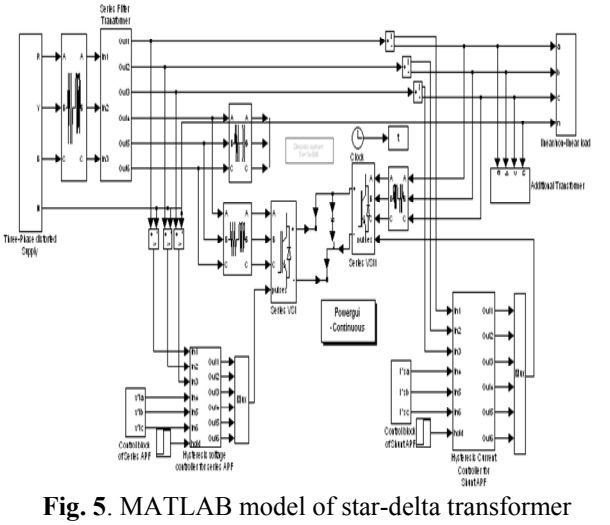

Fig. 5. MATLAB model of star-delta transformer supported 3P-4W UPQC

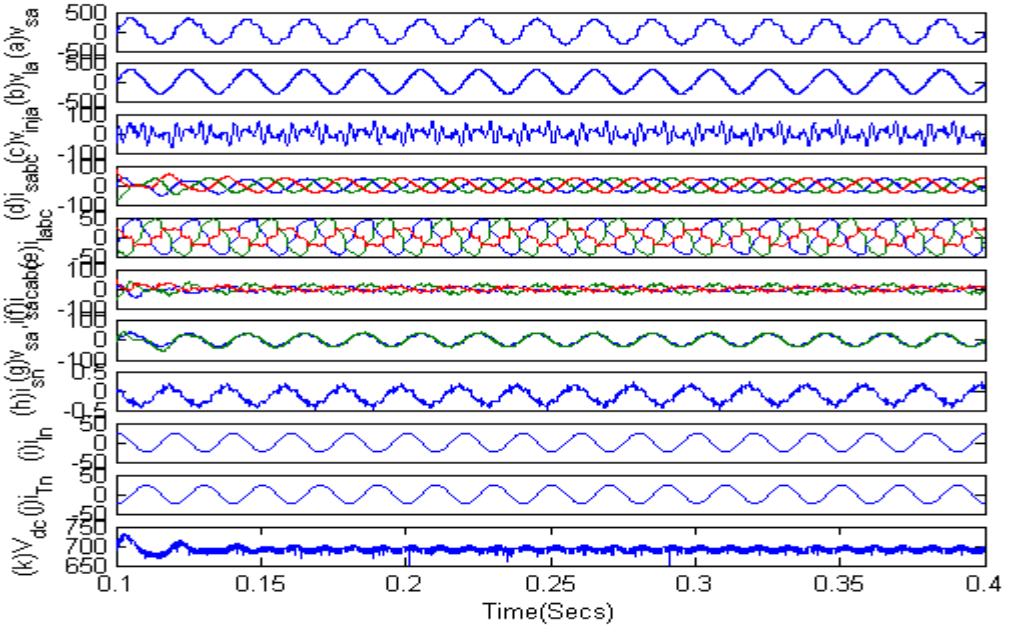

Fig. 6. Performance of star-delta transformer supported 3P-4W UPQC

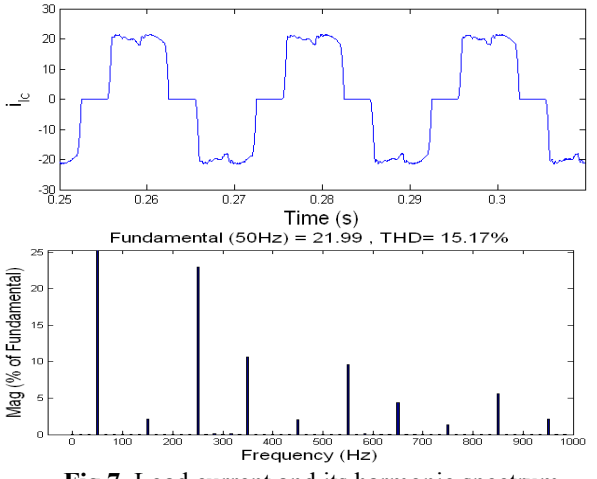

Fig.7. Load current and its harmonic spectrum

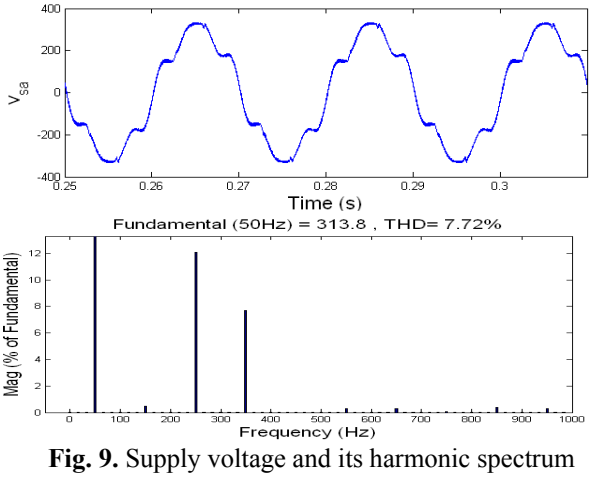

Fig. 9. Supply voltage and its harmonic spectrum

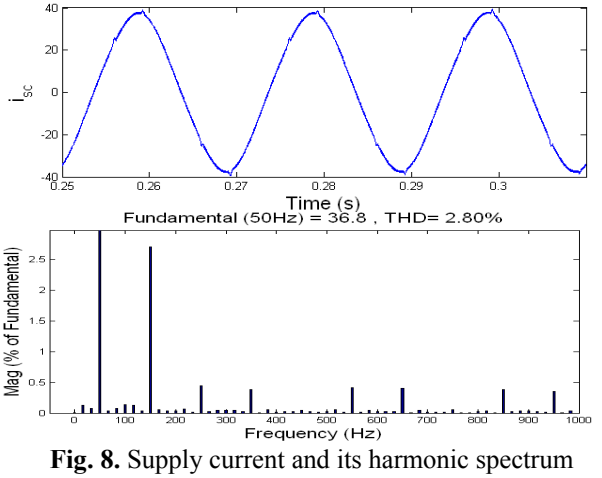

Fig. 8. Supply current and its harmonic spectrum

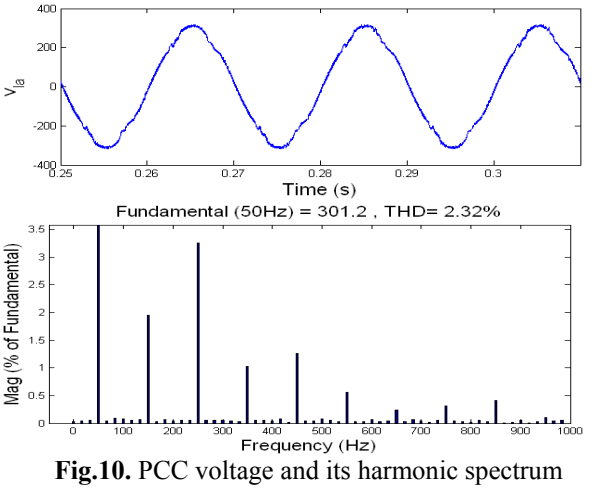

Fig.10. PCC voltage and its harmonic spectrum

6. RESULTS AND DISCUSSION

Fig. 6 shows the response of a three-phase four-wire UPQC with star-delta transformer at the load side. At t=0.05 sec both the shunt and series APF are switched on simultaneously. It is observed from Fig. 6 (d) that the supply currents are balanced and sinusoidal while, the load currents are distorted and unbalanced, as shown in Fig. 6 (e). It is also observer from the Fig. 6 (g) that source current and source voltage in phase 'a' are exacting in phase, hence shunt APF is compensating for the reactive power along with load balancing and current harmonic mitigation. Fig. 6 (i) shows that there is a neutral load current because of the unbalanced load, but the star-delta transformer is able to mitigate the neutral current as shown in Fig. 6 (h). Fig. 6 (i) shows the neutral current of the star-delta transformer, which is exactly opposite to the load neutral current.

In addition to this, the series APF starts compensating voltage harmonics immediately by injecting out of phase harmonic voltage, making load voltage at load distortion free. The voltage injected by series APF is shown in Fig. 6 (c). Fig. 6 (k) shows that during the operation of UPQC DC voltage across the capacitor of back to back VSI is maintained to its reference value. In phase 'c' the THD of load current THD is15.17%, while the THD of source current is 2.80% as shown in Fig. 7 and Fig. 8, respectively. The harmonic spectrum of load voltage before compensation is shown in Fig.9, while the harmonic spectrum of load voltage after compensation is shown in Fig. 10. The load voltage THD is improved form 7.72% to 2.32 %.

7. CONCLUSION

The effectiveness of star-delta transformer supported 3P-4W UPQC topology has been demonstrated for voltage, harmonic elimination, mitigation of current harmonics, load balancing and power-factor correction. Supply currents and load voltage harmonics levels are maintained below IEEE-519 standards under all conditions. The star-delta transformer connected near the load effectively compensates the source neutral current. By connecting a star-delta transformer on the load side, the rating of the UPQC is reduced due to elimination of a fourth leg compared to three-phase four-leg VSI based 3P-4W UPQC. In addition to this, no extra control is required for the mitigation of neutral current; hence numbers of current sensors are reduced. The experimental set-up and results are planned for future work.

8. APPENDIX

The system parameters used are as follows:
Supply voltage: 415 V (L-L) RMS, 50Hz.
Supply impedance: 1.5mH, 0. 1Ω.
DC link capacitance value: 3000μF
DC link voltage: 700 V
Ripple filter: 7Ω, 5μF
K_p=2, K_i=2
Transformer: 250MVA, 58KV/12KV
Linear load: 12KW, 8KVar lagging load in phase 'a' and 'b'.
Non-Linear load: Three-Phase Rectifier Load R=15 on dc side
Star-delta transformer: 5 KVA, 240V/240 V

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