Improved Level Balancing with Diode-Clamped Multi-Level Inverter Configuration Based on Multi-Winding Transformer

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ABSTRACT:
A new configuration for a diode-clamped multi-level inverter based on a multi-winding transformer was proposed and simulated. The most important difference between this proposed DC-AC-AC structure, and the basic structure is that; in the proposed structure, the back-to-back connected outputs of a multi-winding transformer supersede the capacitors in the basic structure. The proposed structure provides the equilibrium in the total time of drawing power between the voltage source steps, as a result, decreasing the unbalancing effect. Isolation and capability to produce more output steps are other advantages of the proposed schematic compared with the conventional capacitor based diode-clamped structure. The simulation result shows the ability of this inverter to feed inductive loads.

KEYWORDS: level balancing, multi-winding, multi-level inverter, diode-clamped inverter.

1. INTRODUCTION

Recently, there has been much interest in research on multi-level inverters. Multi-level inverters synthesize a desired voltage close to sinusoidal voltage using separated or back-to-back connected voltage sources [1-7].

From the perspective of control method, inverters are classified into two major groups: the Line-Frequency controlled multi-level inverters, and the PWM controlled multi-level inverters.

In the Line-Frequency controlled multi-level inverters, the switches are controlled by low frequency signals, hence, generating a staircase output, the more number of levels, the lower the THD and *dv/dt* across the switches. As for the PWM controlled multi-level inverters, the switches are controlled by high frequency PWM signals. Depending on the application of the inverter, both methods are applied to multi-level inverters.

Diode-clamped multi-level inverter was introduced by some scientists in the last decade [8-11]. The basic structure of a diode-clamped inverter is based on N-series connected capacitors that act as DC sources, in which the load is clamped to them to reach the desired output voltage. Reference [12] describes the improved diode-clamped inverter.

2. UNBALANCING IN CAPACITOR BASED DIODE-CLAMPED STRUCTURE

Unbalancing in voltage of capacitors is a drawback in a diode-clamped multi-level inverter. This arises from the fact that the discharging time for each capacitor is different. Repeating such a charging profile of capacitors at every half cycle, results in unbalanced voltages between the different levels [3]. "Due to capacitor voltage balancing issues, practical diode-clamped inverters have been mostly limited to the original three-level structure" [13]. Hence, to overcome the unbalancing problem between the levels, a new configuration based on a multi-winding transformer as the voltage source is proposed, and a 7-level inverter is simulated.

3. BASIC STRUCTURE OF THE PROPOSED INVERTER

The basic concept of the proposed inverter was described in [14]. This inverter, as shown in Fig. 1, is a three-stage DC-AC-AC converter. It consists of a simple low frequency H-Bridge block and a switch array similar to the conventional diode-clamped converter.

The H-Bridge block converts the DC voltage of the voltage source to a low frequency square wave AC voltage with $+V_{DC}$ and $-V_{DC}$ peak amplitudes (see Fig. 1). The dead time must be considered to prevent short circuit. In addition, this AC voltage is applied to the primary of a multi-winding transformer. The transformer then converts this square wave input to a multiple synchronous low frequency output with the desirable amplitude [15]. By choosing an appropriate switching strategy, these voltages are synthesized to reach the desired near sinusoidal output. Depending on the application, a suitable filter is chosen to eliminate unwanted harmonics.

Table 1. Switching pattern in positive cycle

Switches in Block A												Switches in Block B					
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Freewheeling path				S_1	S_2	S_3	S_4	S_5 to S_8 and S_1' to S_4'	Output
								S_1'	S_2'	S_3'	S_4'						
0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1		0
0	0	0	1	0	1	0	0	1	1	1	0	1	1	1	1		$+V_1$
0	0	1	1	0	0	1	0	1	1	0	0	1	1	1	1	0	$+V_1+V_2$
0	1	1	1	0	0	0	1	1	0	0	0	1	1	1	1		$+V_1+V_2+V_3$
1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1		$+V_1+V_2+V_3+V_4$

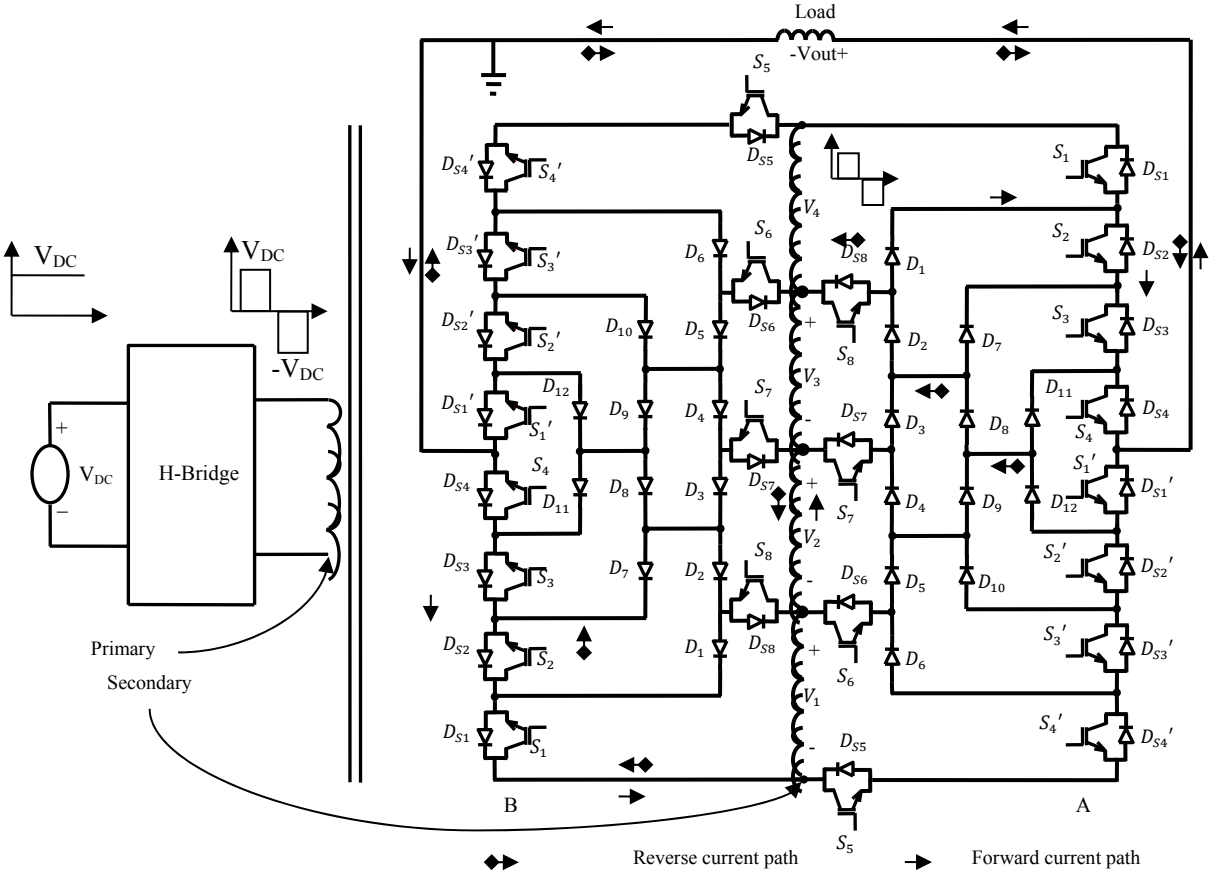

Fig. 1. Forward and reverse current paths for the proposed inverter when the output voltage equals $+V_1+V_2+V_3$

4. NORMAL OPERATION OF CIRCUIT IN POSITIVE CYCLE

Table 1 shows the switching strategy of the positive cycle for the proposed inverter. All instances in the positive cycles, S_5 to S_8 and S_1' to S_4' from Block B are turned off, while for S_1 to S_4, they are turned on (i.e. standby for reverse path). If S_6 and S_4 from Block A are turned on, the output equals V_1. At this stage, S'_1 to S'_3 are kept on to provide probable freewheeling path. In addition, if S_7, S_3 and S_4 are turned on, the output equals $V_1 + V_2$. At this stage, S_1' and S_2' are kept on to provide probable reverse path. If S_8, S_2, S_3 and S_4 are turned on, the output equals $V_1 + V_2 + V_3$. At this stage, S_1' is kept on to provide the reverse path. Fig. 1 shows this condition. To reach the maximum in positive cycle, S_1 to S_4 are turned on. In this case, D_{S4} to D_{S1} from Block A and S_1 to S_4 from Block B provide the reverse path.

Finally, to reach the output that equals zero, S_5 and S_1' to S_4' from Block A are turned on. Thus, the forward current path includes D_{S4} to D_{S1} from Block B and S_5 and D_{S4}' to D_{S1}' from Block A.

The important point here is that in the positive cycle, S_5 to S_8 from Block B must be kept off, otherwise, short circuit will occur. Even in the dead time of H-Bridge (from positive to zero), because there may be some stored energy in the secondary, turning on S_5 from Block B will cause a short circuit.

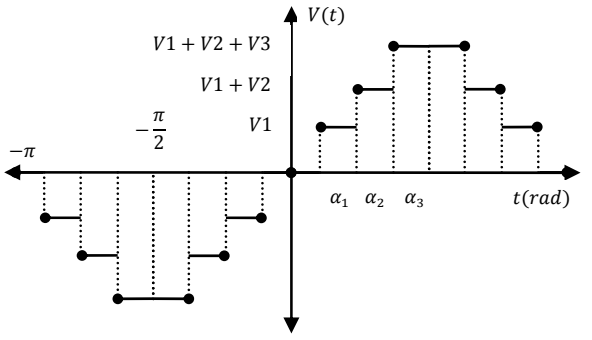

Fig. 2. Output of a 7-level line-frequency controlled multi-level inverter

5. NORMAL OPERATION OF CIRCUIT IN NEGATIVE CYCLE

The process is similar to the positive cycle but the order of applying the voltages to the load is different. In the first interval of positive cycle, V_1 is applied to the load, whereas in the first interval of negative cycle, $-V_4$ is applied to the load. This causes the improvement in equivalency of the drawing power from the voltage source steps.

6. BETTER BALANCING IN DRAWING POWER FROM VOLTAGE STEPS

The effect of unbalancing in conventional diode-clamped inverters can be decreased by using the inductive sources, such as the output ladder of a multi-winding transformer. These elements can act as the voltage sources. The presence of magnetic flow guarantees a relatively constant voltage in the secondary of transformer in that frequency. No unbalancing in the output steps was reported in the previous structures based on the multi-winding transformer [15] nor the multiple transformers[16].

Besides, unlike the conventional diode-clamped inverter, the drawing power from the voltage source steps is symmetrical in the proposed inverter.

In Section 2, it was denoted that the most important reason for unbalancing is the inequality in the total time of drawing power in a cycle. With reference to the switching strategy in a 7-level diode-clamped inverter, obviously, for all instances in the positive and negative cycles (except for the dead time), V_1 (C_1) feeds the load for $4*(\alpha_1+ \alpha_2+ \alpha_3)$ in a full period, while V_2 (C_2) feeds the load for $4*(\alpha_2+ \alpha_3)$ and V_3 (C_3) feeds for $4*(\alpha_3)$. This shows unbalancing in the drawing power from the capacitors. Notably, following the voltage's law, by decreasing the voltage in C_1, voltage is increased in other capacitors, resulting in more voltage differences between the output steps and the worst THD. Nevertheless, the intensity of this unbalancing depends on the type and size of the load.

In the same condition for the proposed structure, V_1 feeds the load for $2*(\alpha_1+ \alpha_2+ \alpha_3)$ in the positive cycle and $2* \alpha_3$ in the negative cycle, giving the total $2*(\alpha_1+ \alpha_2+2* \alpha_3)$ in a period. Meanwhile, V_2 feeds the load for $2*(\alpha_2+ \alpha_3)$ in the positive cycle and $2*(\alpha_2+ \alpha_3)$ in the negative cycle, giving the total $4*(\alpha_2+ \alpha_3)$ in a period. At last, V_3 feeds the load for $2* \alpha_3$ in the positive cycle and $2*(\alpha_1+ \alpha_2+ \alpha_3)$ in the negative cycle, giving the total $2*(\alpha_1+ \alpha_2+2* \alpha_3)$ in a period (see Table 2). This shows more equality between the voltage steps in feeding the load. Moreover, by increasing the number of levels, the total time that the steps feed the load approaches each other.

Table 2. Total time each voltage step feeds the load in one cycle

	Conventional Diode-Clamped Inverter	Proposed inverter
V_1	$4*(\alpha_1+ \alpha_2+ \alpha_3)$	$2*(\alpha_1+ \alpha_2+2* \alpha_3)$
V_2	$4*(\alpha_2+ \alpha_3)$	$4*(\alpha_2+ \alpha_3)$
V_3	$4*(\alpha_3)$	$2*(\alpha_1+ \alpha_2+2* \alpha_3)$

Advantages of the proposed inverter are as follows:

- Unlike the conventional diode-clamped inverter, the proposed art provides isolation. Hence, this ensures the standards in grid-tie inverters.
- The input DC sources can be chosen with various ranges of voltages.

The structure improves unbalancing between the output steps.

- The structure provides possibility to produce more voltage steps. Thus, this decreases the size of output filter, which means better THD.
- It has an easy switching pattern. Moreover, unlike the one proposed in [13], PWM switching is possible. Also, the structure provides more immunity when switches fail in short circuit behaviour compared with [13].

Recycling the transformer is more cost effective than the capacitors. Besides, the transformers are more reliable.

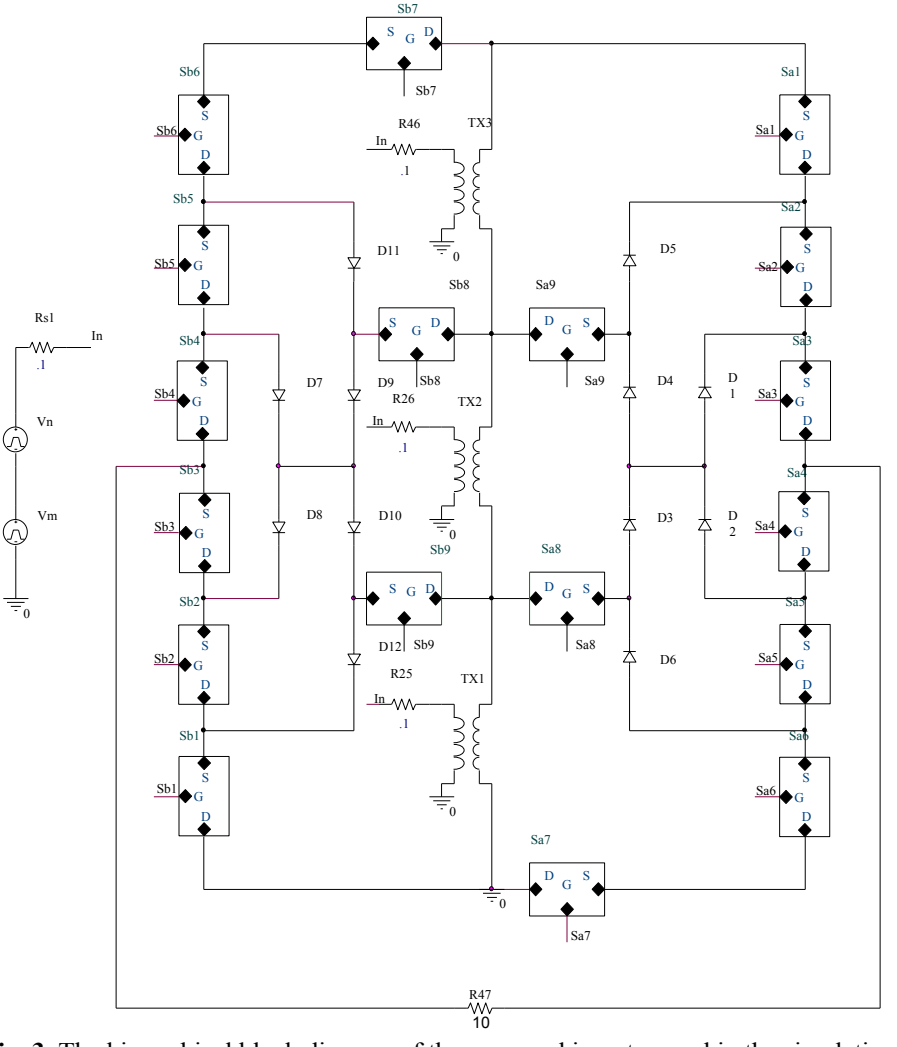

Fig. 3. The hierarchical block diagram of the proposed inverter used in the simulation

On the contrary, the proposed structure has some disadvantages as well, described as follows:

- The non-linear loads cause unbalancing in the transformer. Nevertheless, removing this problem is possible and has been described in [15].
- Some switches must tolerate the DC link voltage.

Increasing the number of steps leads to the increase in the total on-state voltage drop of switches, which also increases the THD. However, decreasing this effect is possible by changing the switching angles. This effect strongly depends on the loads and type of the selected switches (i.e. MOSFET or p-n junction switches). If N represents the number of windings, in nth step, (n+1) switches and (2N-n) diodes are conducting. A model for calculating the on-state power dissipation is described in [17].

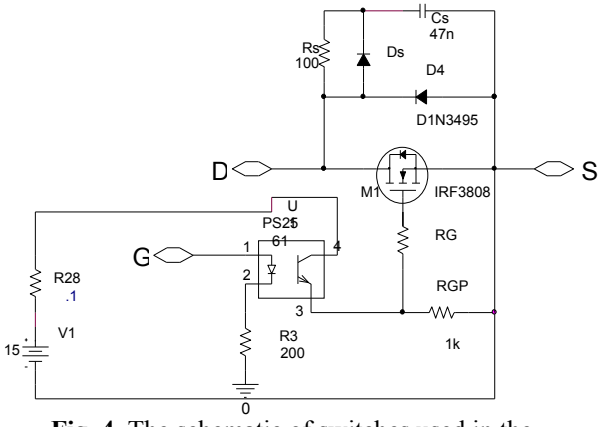

Fig. 4. The schematic of switches used in the simulation

7. SIMULATION AND RESULTS

OrCAD16.2[1] was used to simulate the 7-level proposed inverter. The auto-convergence ability of this software provides the possibility to simulate high current

[1] Note that we tried to simulate the proposed structure using OrCAD16, but failed because of convergence problem.

and voltages beside low current and voltages of the controlling modules.

To simulate the multi-winding transformer, the proposed ladder model in [18] was applied. Fig. 3 shows the hierarchical schematic used for the simulation of the proposed inverter. In this figure, the primary and secondary of TX_1, TX_2 and TX_3 were connected in parallel and series respectively to act as a multi-winding transformer. In addition, S_a and S_b Blocks represent the switches. To reach the near sinusoidal output, the firing angles for MOSFET gates (S_a and S_b signals) were calculated from this equation [19]:

$$\theta_n = \sin^{-1}\left(\frac{n-0.5}{N}\right) \quad (1)$$

Where N is the number of sources. Fig. 4 illustrates the schematic of switches used to simulate the switches in Fig. 3. The floating 15V DC source acts as a voltage source feeding the driver module. In reality, this voltage is generated by a low power multi-winding transformer with isolated outputs or by isolated DC-DC converters. To provide a more realistic condition, RCD Snubbers are also added to the switches.

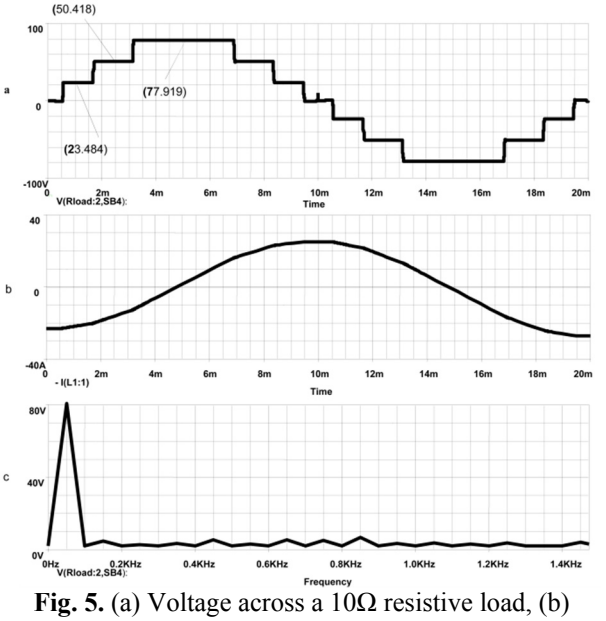

Fig. 5. (a) Voltage across a 10Ω resistive load, (b) Output current for a pure inductive load and (c) Frequency spectrum of voltage

Fig. 5 illustrates the simulation results for the 7-level proposed inverter with MOSFET switches. Fig. 5(a) and Fig. 5(b) illustrate the voltage and current through a 10Ω resistive and a pure inductive load respectively. Meanwhile, Fig. 5(c) is the FFT of the voltage across the 10Ω load. This figure shows the ability of the proposed inverter to feed the inductive loads. The voltage levels show the acceptable voltage balancing. To decrease the effect of voltage drops of diodes on balancing (THD) and efficiency, for low voltage inverters like the ones used in stand-alone or grid-tie inverters, it is advised to use the conventional model proposed in [11]. Besides, it is also possible to use the PWM method with a lower number of switches.

8. CONCLUSION

A new configuration for diode-clamped multi-level inverter based on a multi-winding transformer was proposed and simulated in this research. In the proposed diode-clamped structure, the capacitors were replaced by a multi-winding transformer to shape a DC-AC-AC converter. Apparently, the most important advantages of the proposed inverter are the ability to produce more output voltage steps and better balancing between the output levels. In addition, the structure has a simple switching strategy. The simulation results showed the ability of this inverter to feed resistive and inductive loads. Besides, there was no considerable unbalancing between levels.

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