Design Issues for Low Voltage Low Power CMOS Folded Cascode LNAs

Ehsan Kargaran[1], Mohammad Javad Zavarei[1], Nahid Fatahi[1], Seyedeh Sara Hassani[1], Khalil Mafinezhad[1], Hooman Nabovati[1]
1- Microelectronic Laboratory, Sadjad Institute of Higher Education, Mashhad, Iran.
Email: e.kargaran725@sadjad.ac.ir

Received: April 2012 Revised: June 2012 Accepted: August 2012

ABSTRACT:
Design and simulation results of fully integrated 5-GHz CMOS LNAs are presented in this paper. Three different input impedance matching techniques are considered. Using a simple L-C network, the parasitic input resistance of a MOSFET is converted to a 50 Ω resistance. As it is analytically proven, that is because the former methods enhance the gain of the LNA by a factor that is inversely proportional to MOSFET's input resistance. The effect of each input impedance matching on the amplifier's noise figure and gain is discussed. By employing the folded cascode configuration, these LNAs can operate at a reduced supply voltage and thus lower power consumption. To address the issue of nonlinearity in design of low voltage LNAs, a new linearization technique is employed. As a result, the IIP3 is improved extensively without sacrificing other parameters. These LNAs consume 1.3 mW power under a 0.6 V supply voltage.

KEYWORDS: Low noise amplifier (LNA), Folded cascode, low power, Low voltage, Parasitic input resistance.

1. INTRODUCTION

The increasing demands for portable wireless devices have motivated the development of CMOS radio frequency integrated circuits (RFIC). Such devices require low power dissipation to maximize their battery lifetime. Some low power applications, such as wireless medical telemetry, require the portable devices to operate at low supply voltage with a small battery or environment energy, which makes the power and supply voltage constriction is a crucial issue for such circuits [1]. Being the first stage of the receiver, the design of a low noise amplifier (LNA) involves trade-offs between multiple concurrent objectives. Typical objectives include (i) providing a stable 50 Ω input impedance to the output of the filter following the antenna, (ii) minimizing the noise figure, and (iii) increasing the gain which should be high enough to lower the noise contribution of the following blocks without affecting the system linearity. Furthermore, in portable systems, the power and supply voltage constraint makes such optimization more complicated.
The folded cascode and current-reused design methods are effective ways to decrease the power consumption. Several low-powers LNA designs have been previously reported [1-3]. The cascode amplifier is widely used for LNA design layouts [3-4], where in conjunction with the current-reused topology, the desirable gain can be achieved with relatively low current consumption [2]. However, due to the use of a stack of multi transistors, it increases the required supply voltage. By employing the folded cascode topology, LNA circuit was implemented in a standard 0.18μm CMOS technology for demonstration, exhibiting enhanced RF performance at reduced supply voltage and power consumption.

In order to minimize reflections between the LNA and the antenna, input of the LNA needs to be matched to the output of the filter following the antenna. Source inductive degeneration, shown in Fig. 1(a), has been used in most of the LNAs in recent years [4-7]. Although this technique is an effective narrow frequency matching technique, it degrades the power gain of the LNA, hence, requires more dc current to compensate the gain loss.

In this paper, a design methodology based on elimination of the degenerative inductor is presented. It is demonstrated that the parasitic input resistance of a MOSFET, R_p, which is always significant in radio-frequency applications, can be converted to 50Ω in a narrow frequency band of interest with a simple L–C network.

The previously mentioned matching methods are discussed in Section 2. Their effects on the gain and NF of the LNA are studied in Sections 3 and 4, respectively. The folded cascode structure is presented in section 5. A new linearization technique is proposed

and studied in Section 6. Section 7 presents Simulation results and finally Conclusions are made in Section 8.

2. INPUT POWER MATCHING METHODS

Three different input matching techniques, which are employed for narrowband CMOS LNAs are discussed in this section. As mentioned earlier, these techniques are used to provide matching criteria between the input of the LNA and the output of antenna, which thus minimizes the reflection coefficient between the two sub-circuits.

2.1. Source Inductive Degeneration (SID)

SID is one of the most popular input matching methods for designing LNAs [7-9]. As shown in Fig. 1(a), SID employs a small inductor, L_s, in series with the source of the MOSFET to generate a real 50Ω resistance at the input of the LNA.

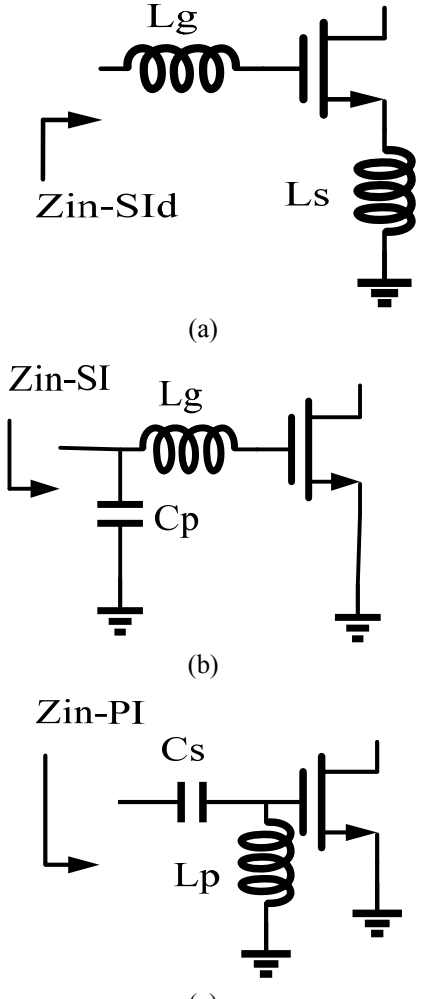


Fig. 1. (a) SID, (b) SI, (c) PI matching methods

The imaginary part of MOSFET's input impedance is cancelled by another inductor, L_g, placed at the input of the LNA. The value of the real resistance generated by L_s is approximately given by $R_s = \omega_T L_s$ [7]. Consequently, the input impedance seen at the input of the LNA, $Z_{in\text{-}SID}$, is given by

$$Z_{in-SID} = \frac{1}{j\omega C_{gs}} + R_{inM} + \omega_T L_s + j\omega(L_g + L_s) \quad (1)$$

where C_{gs} and R_{inM} are gate to source capacitance and parasitic input resistance of MOSFET, respectively, which results in $R_{inM}+\omega_T L_s$ being equal to 50Ω and $(L_g+L_s)=1/(\omega^2 C_{gs})$, when matched. As it will be shown later, this technique degrades the power gain of the LNA, hence may not be suitable for low-power applications.

2.2. Series Inductive (SI)

The SI method, shown in Fig. 1(b), converts the parasitic input impedance of the MOSFET $Z_{inM} = R_{inM} - jX_{inM}$ to 50Ω with a simple LC network. The former is the real part of Z_{inM}, which is obtained from the reflection coefficient S_{11} as $Z_{inM}=50(1+S_{11})/(1-S_{11})$ in a 50Ω system, whereas the latter is equal to the real part of $1/Y_{11}$ [11] .

Considering the circuit shown in Fig. 1(b), the input impedance of the LNA, which is designed with the SI method, can be expressed as;

$$Z_{in-SI} = \frac{R_{inM} + j\omega[L(1-\omega^2 LC_p) - C_p R_{inM}^2]}{(\omega C_p R_{inM})^2 + (1-\omega^2 LC_p)^2} \quad (2)$$

Where $L=L_g-1/(\omega^2 C_{gs})$. Satisfying the matching criteria at the input of the LNA, the imaginary and real parts of $Z_{in\text{-}SI}$ should be equal to zero and 50Ω, respectively, which yields [3];

$$L = \frac{\sqrt{50\, R_{inM} - R_{inM}^2}}{\omega} \quad (3)$$

$$C_p = \frac{\sqrt{50\, R_{inM} - R_{inM}^2}}{50\, \omega R_{inM}} \quad (4)$$

2.3. Parallel Inductive (PI)

Considering Fig. 1(c), the input impedance of the LNA designed with the PI method can be expressed as

$$Z_{in-PI} = ((\omega L_{p1})^2 / R_p) + j(\omega L_{p1} - 1/(\omega C_s)) \quad (5)$$

where $R_p = 1/(R_{inM}(\omega C_{gg})^2)$. L_{p1} is the inductance which is seen by C_s when looking towards the LNA. Therefore, when the input of the LNA is matched, one obtains $(\omega L_{p1})^2/R_p=50$, and $\omega L_{p1}=1/(\omega C_s)$, which yields;

$$C_s = C_{gg}\sqrt{\frac{R_{inM}}{50}} \quad (6)$$

$$L_p = \frac{1}{\omega^2 C_{gg}(1+\sqrt{\frac{R_{inM}}{50}})} \quad (7)$$

The minimum value of S11 is adjusted by L_g and C_p, in SI-LNA and by L_p and C_s, in PI-LNA respectively.

3. EFFECTIVE TRANSCONDUCTANCE

The trans-conductance, g_m, of the MOSFET is normally used to characterize the gain performance of low-frequency amplifiers. However, since radio frequency amplifiers are matched for maximum power delivery, a more accurate parameter to estimate their power gain is the effective trans-conductance, G_m. The effective transconductance is defined as the amplitude of the output current, i_{out}, divided by the input voltage, v_{in}. Evidently, G_m is proportional to the g_m of the MOSFET; however, as it will be demonstrated in this section, this proportionality depends on selecting input matching network. To derive compact analytical expressions for G_m, a simple equivalent circuit model for the input stage is used. Although C_{gd} and the substrate network are neglected in deriving these compact expressions, the model is still applicable for comparing the effect of different matching methods on the G_m of the cascode LNAs, as the neglected elements will have the same effect on the G_m in all methods. Since the focus of this paper is design of narrowband amplifiers, then G_m of the LNAs are derived in a narrow frequency band of interest, where the input is matched and the equations presented in the previous section are valid.

3.1. SID Method

According to our definition, and Fig. 2(a), the Gm of a LNA in this case is equal to

$$G_{m-SID} = \left|\frac{i_{out1}}{v_{in}}\right| = \left|\frac{\frac{g_m}{j\omega C_{gs}}}{\frac{1}{j\omega C_{gs}} + R_{inM} + \omega_T L_s + j\omega(L_g + L_s)}\right| \quad (8)$$

Therefore, in the narrow frequency band of interest where L_g is chosen such that $\omega^2 C_{gs}(L_s+L_g)=1$, and $R_{inM}+\omega_T L_s=50\Omega$ one obtains;

$$G_{m-SID} = \left|\frac{i_{out\ 1}}{v_{in}}\right| = \frac{\omega_T}{\omega . R_s} = \frac{\omega_T}{50\ \omega} \quad (9)$$

As seen from (8), $G_{m\text{-}SID}$ increases if L_s is removed; however, this is not a practical option since the input of the LNA has to be matched to the antenna. Therefore, there is a tradeoff between the power gain and the input return loss of the LNA in this case.

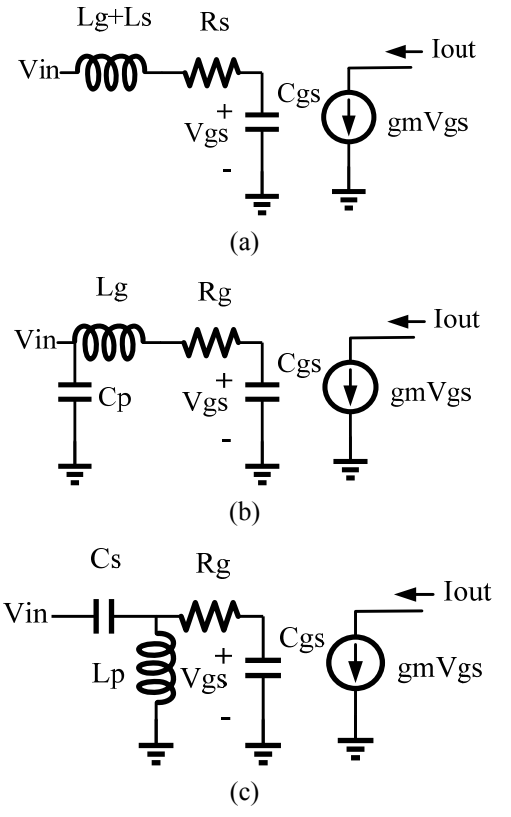


Fig. 2. Simplified equivalent circuit model of the input stage matched with (a) SID, (b) SI, (C) PI methods.

3.2. SI Method

Using the equivalent circuit model of Fig. 2(b), the effective trans-conductance of the SI LNA can be derived as

$$G_{m-SI} = \left|\frac{i_{out1}}{v_{in}}\right| = \left|\frac{g_m(1/j\omega C_{gs})(1/j\omega C_p)}{(1/j\omega C_{gs})+(1/j\omega C_p)+R_{inM}+j\omega L_g}\right| \times \frac{1}{Z_{in-SI}} \quad (10)$$

Using (3) and (4) in (10) in the narrow frequency band of interest, it yields [3]

$$G_{m-SI} = \left|\frac{i_{out\ 1}}{v_{in}}\right| = \frac{\omega_T}{50\ \omega}\sqrt{\frac{50}{R_{inM}}} \quad (11)$$

3.3. PI Method

Using the equivalent circuit model of Fig. 2(c), the effective trans-conductance of the PI LNA can be derived as

$$G_{m-PI} = \left|\frac{\frac{1}{Z_{in-PI}}(g_m \times L_p / C_{gs})}{\sqrt{R_{inM}^2 + \frac{1}{(\omega C_{gs})^2} \times \frac{R_{inM}}{50} \times \frac{1}{(1+\sqrt{R_{inM}/50})^2}}}\right| \quad (12)$$

Using (6) and (7) in (12) in the narrow frequency band of interest, it yields

$$G_{m-PI} = \left| \frac{i_{out\,1}}{v_{in}} \right| \approx \frac{\omega_T}{50\,\omega} \sqrt{\frac{50}{R_{inM}}} \quad (13)$$

As demonstrated by (11) and (13), the G_m of SI and PI LNAs are larger than that of SID LNA by a factor of $(50/R_{inM})^{1/2}$ in the desired frequency band. The enhanced G_m of the SI and PI LNAs enable us to design both high-gain and low-power LNAs at higher frequencies, where the low-power operation is highly demanded to extend the battery life time of mobile devices. The effect of the three matching methods on the Noise Figure of the LNA is discussed in the next chapter.

4. NOISE FIGURE

The noise factor of a two-port network, such as the LNA, can be expressed as

$$F = F_{\min} + \frac{G_n}{R_{source}} \left| Z_{source} - Z_{opt} \right|^2 \quad (14)$$

where F_{min} is the minimum noise factor, G_n the equivalent noise conductance. $Z_{source}= R_{source} +jX_{source}$ is the impedance seen at the input of the LNA, when looking towards the antenna. $Z_{opt}= R_{opt}+jX_{opt}$ is the optimum source impedance for achieving minimum noise factor. Although F_{min} can be minimized by properly choosing the width of the MOS device, our simulations show that for a constant dc current, the change in F_{min} versus the transistor's width is only a few tenths of a decibel. Therefore, to minimize the NF, NF=10log F (dB), it is crucial to design the matching network of the LNA such that the second term in (14) be close to zero, which in turn means that Z_{source} should be very close to Z_{opt} . Using the noise sources and noise parameters expressions given in [12-14], one can obtain R_{opt} and X_{opt} of a MOSFET as follows;

$$R_{opt} = \frac{1}{\omega C_{gs}} \sqrt{\frac{R_g}{R_n - R_g}} \quad (15)$$

$$X_{opt} \approx \frac{1}{\omega C_{gs}} = X_{inM} \quad (16)$$

Here, $R_n=G_n(R_{opt}^2+X_{opt}^2)$ is the equivalent noise resistance of MOSFET, and X denotes the absolute value of the imaginary parts of the impedances. As seen from (16), X_{opt} and X_{inM} of a MOSFET are very close, which agrees with the results previously reported in [4]. Furthermore, equation (15) shows that R_{opt} is inversely proportional to the width of the transistor and the frequency of operation. Therefore, according to our definition of matching network, simultaneous noise and power matching of the LNA is possible when;

$Z_{source}= Z_{inM}^*=Z_{opt}$ (17)

Since X_{opt} and X_{in} of the MOSFET are very close, the condition in (17) translates to $R_{opt}=R_{source}=R_{inM}$.

4.1. SID Method

In this case, $Z_{source}= R_s+j\omega L_g$, where R_s is the characteristic impedance of the system and is usually 50Ω. Since according to (1), ωL_g is chosen to be very close to X_{inM} (or X_{opt}), the NF of the SID LNA can be minimized at the desired frequency, if only R_{opt} of the common source device is close to R_s. Therefore, for a given frequency of operation and defined dc current consumption, the width of the common source device should be adjusted such that R_{opt} is close to 50Ω. It should also be noted that in the above noise analysis it is assumed that inductors' loss are negligible.

4.2. SI and PI Methods

According to the definition of matching network, noise and power matching of the LNA, designed with this method, are achieved when $R_{opt}=R_{source}$ and $R_{source}=R_{inM}$. Therefore, when R_{opt} is larger than R_{inM}, which is usually the case at intermediate frequencies such as 5 GHz, there is a tradeoff between NF and input matching parameter, S_{11}. However, in this method R_{source} is selected equal to R_{inM}, when perfect input power matching is desired. As a S_{11} value of less than -10dB is adequate for the LNA in most applications, even when R_{opt} of the MOSFET is larger than R_{inM}, the value of R_{source} could be brought closer to R_{opt} by altering the values of C_p and C_s obtained from (4) and (6), for better noise matching [12].

5. LOW VOLTAGE LOW POWER FOLDED CASCODE LNAS

The schematics of three low voltage low power folded cascode LNAs based on SID, SI, and PI methods are shown in Fig. 3. These LNAs are designed for 5GHz application with low supply voltage. The folding of the common-gate transistor helps to extend the cut-off frequency of the common-source transistor. Furthermore, the parasitic capacitances at the drain node of the common-source transistor (M_1) can easily be eliminated by the resonance with the inductance at the supply pin L_d [15]. The elimination or the reduction of this parasitic capacitance helps suppress the noise contribution of the common-gate transistor at the output. A simple L-C network using an on-chip inductor of L_o and an on-chip capacitor of C_o are used to match the output of the LNA.

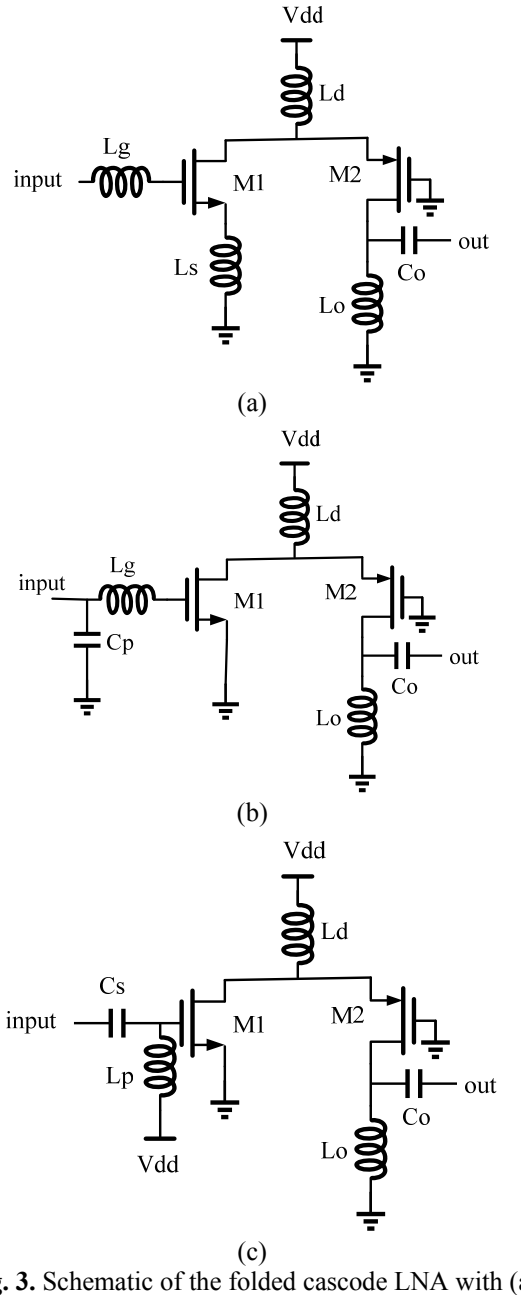


Fig. 3. Schematic of the folded cascode LNA with (a) SID, (b) SI, (c) PI methods [18].

6. LINEARITY

One of the important parameters that should be considered in design of LNAs is the linearity. The linearity of low voltage low power LNAs is generally degraded by other design limitations, thus linearity improvement techniques should be applied to improve the linearity. As presented in Fig. 4, a feed forward structure is employed by adding a NMOS transistor (M_3) and an inductor (L_2) to the conventional folded cascode configuration. Therefore, the output current is obtained from the difference between drain currents of M_2 and M_3. The aspect ratio, bias voltage, and the value of L_2 associated with the auxiliary transistor are chosen to tune the magnitude and phase of M_3 3rd order inter-modulation component, IM_3, canceling the IM_3 components generated by the main amplifier and it improves linear characteristic of conventional folded cascode circuit.

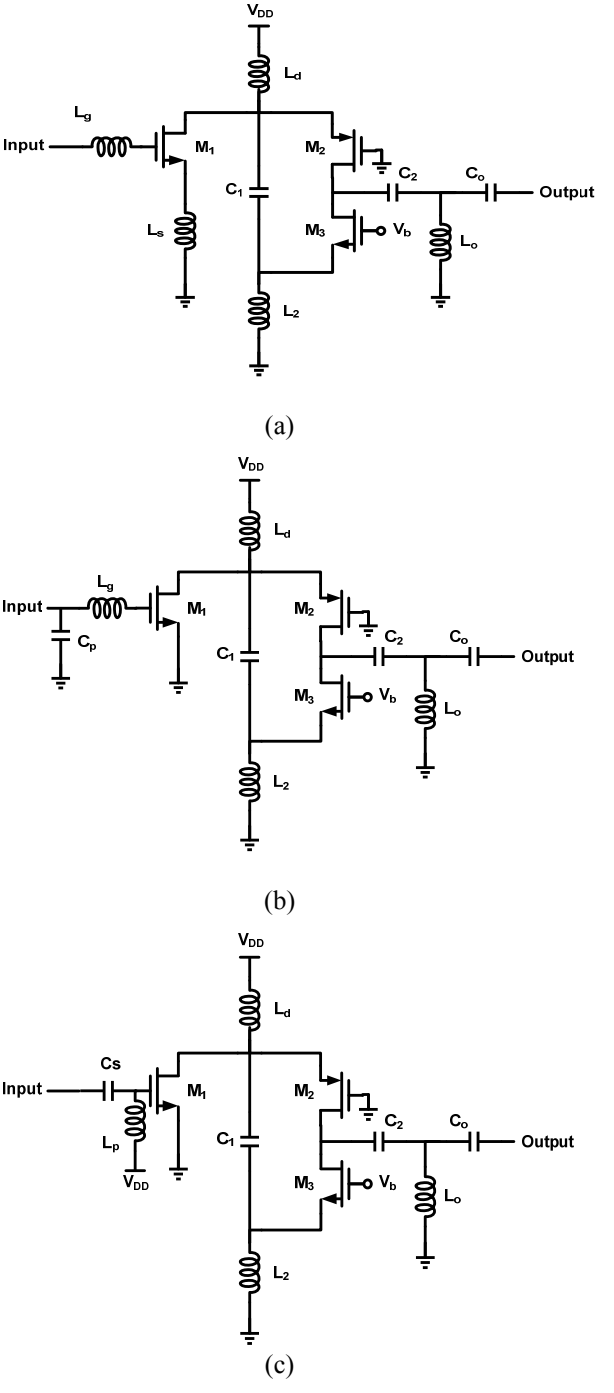


Fig. 4. Schematic of the proposed folded cascode LNA by applying linearity technique on (a) SID [19], (b) SI, (c) PI methods.

C_1 and C_2 are coupling capacitors. Since the auxiliary transistor (M_3) is added in the second stage of amplifier, it has a negligible effect on the amplifier's noise figure. Because of the reusing bias current via M_3, it does not dissipate any extra power either. one of the most common methods for linearity analysis is using Volterra-series. In this method, each significant nonlinear element must be characterized by a power series in terms of its small-signal controlling voltages [16]. The dominant nonlinearity behavior of a MOS transistor arises from its voltage-to-current (V–I) conversion. Thus, the currents through the M_1, M_2 and M_3 are given in terms of their gate–source voltages,

$$i_1 = g_{11}V_{gs1} + g_{12}V_{gs1}^2 + g_{13}V_{gs1}^3 \quad (18)$$

$$i_2 = g_{21}V_{sg2} + g_{22}V_{sg2}^2 + g_{23}V_{sg2}^3 \quad (19)$$

$$i_3 = g_{31}V_{gs3} + g_{32}V_{gs3}^2 + g_{33}V_{gs3}^3 \quad (20)$$

The V_{gs1} and i_1 could be given in term of the input voltage (V_i) by using Volterra series as the following equation;

$$i_1 = B_1(s_1)\circ V_i + B_2(s_1,s_2)\circ V_i^2 + B_3(s_1,s_2,s_3)\circ V_i^3 \quad (21)$$

where $B_1(s_1)$, $B_2(s_1,s_2)$ and $B_3(s_1,s_2,s_3)$ are first, second, and third nonlinearity coefficients. The operator "$\circ$" means that the magnitude and phase of each spectral component of V_i^n is to be changed by the magnitude and phase of $B_n(s_1,s_2,...,s_n)$,where the frequency of the component is $w_1+w_2+...+w_n$ [17].

The harmonic input method in the Volterra series analysis is used to analyze the various coefficients of nonlinearity in (21). The effect of all parasitic capacitances other than the gate–source capacitances is neglected.

By using Kirchhoff's laws in the small signal model and the harmonic input method in the Volterra series analysis, the following equations can be derived:

$$B_1(s_1) = \frac{g_{11}}{s_1 L_s x_1(s_1)} \quad (22)$$

$$B_2(s_1,s_2) = \frac{g_{12}\left(x_1(s_1+s_2) - g_{11}\right)}{s_1 s_2 L_s^2 x_1(s_1+s_2)x_1(s_1)x_1(s_2)} \quad (23)$$

where;

$$x_1(s) = sC_{gs1} + g_{11} + \frac{1+s^2 C_{gs1}L_g}{sL_s} \quad (24)$$

IMD_3 (Third order intermodulation distortion) at $2w_a$-w_b can be found by setting $s_1=s_2=s_a$ and $s_3= -s_b$. Assuming closely spaced frequencies, *i.e.*, $s_a \cong s_b \cong s$ and using three-tone excitation, we can derive;

$$B_3(s_a,s_a,-s_b) = \frac{\left(g_{11}-x_1(s)\right)\left(g_{13}x_1(2s) - 2g_{12}^2\right)}{3s^3 L_s^3 x_1^3(s)x_1(2s)x_1(-s)} \quad (25)$$

According to (19) and (20) the output current can be calculated as follows;

$$i_{out} = (g_{21}+g_{31})V_{sg2} + (g_{22}-g_{32})V_{sg2}^2 + (g_{23}+g_{33})V_{sg2}^3 \quad (26)$$

where $V_{sg2} = V_{sg3}$.

According to (26), it can be shown that the amplifier's total trans-conductance increases; the IM2 term decreases, as g_{22} and g_{32} have the same sign; and the IM3 term decreases, because g_{23} and g_{33} could have different signs. By properly choosing the circuit parameters such as transistor's aspect ratio and the biasing voltage, V_b, the optimum criteria could be achieved, where $g_{22} = g_{32}$ and $g_{23} = -g_{33}$, and therefore:

$$\begin{aligned} i_{out} &= (g_{21}+g_{31})V_{sg2} \\ &= C_1(s_1)\circ V_i + C_2(s_1,s_2)\circ V_i^2 + C_3(s_1,s_2,s_3)\circ V_i^3 \end{aligned} \quad (27)$$

Applying Kirchhoff's current law to drain of M_1, assuming L_d=L_2, the following equation can be derived;

$$i_{out} = \frac{-(g_{21}+g_{31})i_1}{x_2(s)} \quad (28)$$

where;

$$x_2(s) = g_{21} + g_{31} + \frac{2}{sL_1} + 2sC_t \quad (29)$$

And;

$$C_t = C_{gs2} + C_{gs3} \quad (30)$$

Using (27) and (28), the various coefficients of nonlinearity for output current for n=1, 2, 3 can be simplified as follow;

$$C_n(s_1,s_2,...,s_n) = \frac{-(g_{21}+g_{31})B_n(s_1,s_2,...,s_n)}{x_2(s_1+s_2+...+s_n)} \quad (31)$$

According to (31), the nonlinear coefficients of output current are proportional to the nonlinear coefficients of first stage. Therefore, according to this technique, the nonlinearity effect of the M_2 can be compensated by an auxiliary transistor (M_3).

Linearity is usually presented by the input-referred third-order intercept point (IIP_3). Therefore, the value of IIP_3 can be given in terms of nonlinearity coefficients of the output current as follows;

$$IIP3 = \frac{1}{6\,\mathrm{Re}(Z_s(s))}\left|\frac{C_1(s_a)}{C_3(s_a,s_a,-s_b)}\right| \quad (32)$$

where, Z_s(s) is considered as conjugate matched input impedance. By substituting (22), (25) and (31) in (32), the expression of IIP_3 could be simplified as:

$$IIP3 = \frac{1}{2}\left|\frac{s^2 C_{gs1}L_s x_1^2(s)x_1(2s)x_1(-s)}{\left(g_{11}-x_1(s)\right)\left(g_{13}x_1(2s) - 2g_{12}^2\right)}\right| \quad (33)$$

As a result, it is expected that the linearity performance of the SID method would be better than the other methods. Accordingly, there is a tradeoff between the power gain (and hence the dc power consumption) and the linearity of the LNA, which

makes the design challenging when low-power operation is desired.

7. SIMULATION RESULTS AND DISCUSSION

The proposed LNAs have been simulated by HSPICE RF using 0.18-µm CMOS process BSIM3 model parameters. All circuits operate with a 0.6 V power supply and consume only 1.3 mW power.

The folded cascode structures used in the design of these circuits are identical, with the width of the transistors M1 and M2 equal to 80 µm and 160 µm, respectively. To reduce the gate resistance, the multi-finger configuration is used for implementing these devices, in which the width and length of each finger are 8 µm and 0.18 µm, respectively.

Figures 5 and 6 shows the calculated gain and noise figure before linearization as a function of frequency at three different transistor size of 60, 80, and 100 µm for three different design methods.

As can be seen in these figures, increasing transistor size of M1 increases the power consumption, and decreases the noise figure at a constant frequency. By increasing the transistor size of M1 from 60 µm to 100 µm, noise figure at desirable frequency decreased in SID, SI and PI matching from 4.5 to 3.9 dB, 4.4 to 3.8 dB, and 4 to 3.5 dB, respectively. As can be seen in Fig. 6, a 0.42 mW increase in the power consumption led to about 0.5dB decrease in the predicted noise figure for three methods at center frequency.

Figure 7 shows the simulated IIP3 versus the fingers of M3 for various value of Vb. As shown in Fig. 7, by choosing Vb=0.5 V and 18 fingers for transistor of M3, these LNAs have the best performance for linearity than other Vb and fingers of transistor.

Figure 8 shows the variation of the output power and IM3 components at the output versus the input power, before and after linearization. It can be verified that the value of IIP_3 is improved by more than 15 dB, 10 dB and 12 dB for SID, SI and PI matching networks, respectively. After linearization, the value of IIP3 for SID, SI and PI matching is +7 dBm, -2.5 dBm, and -1 dBm, respectively.

The simulated S-parameters and NF performances of the LNA are plotted in Figs. 9, 10, and.11. As can be seen from Fig.11,using SI and PI matching causes the gain of LNA to increase more than the cases where SID matching was used, the increase of gain is about 3dB at center frequency.

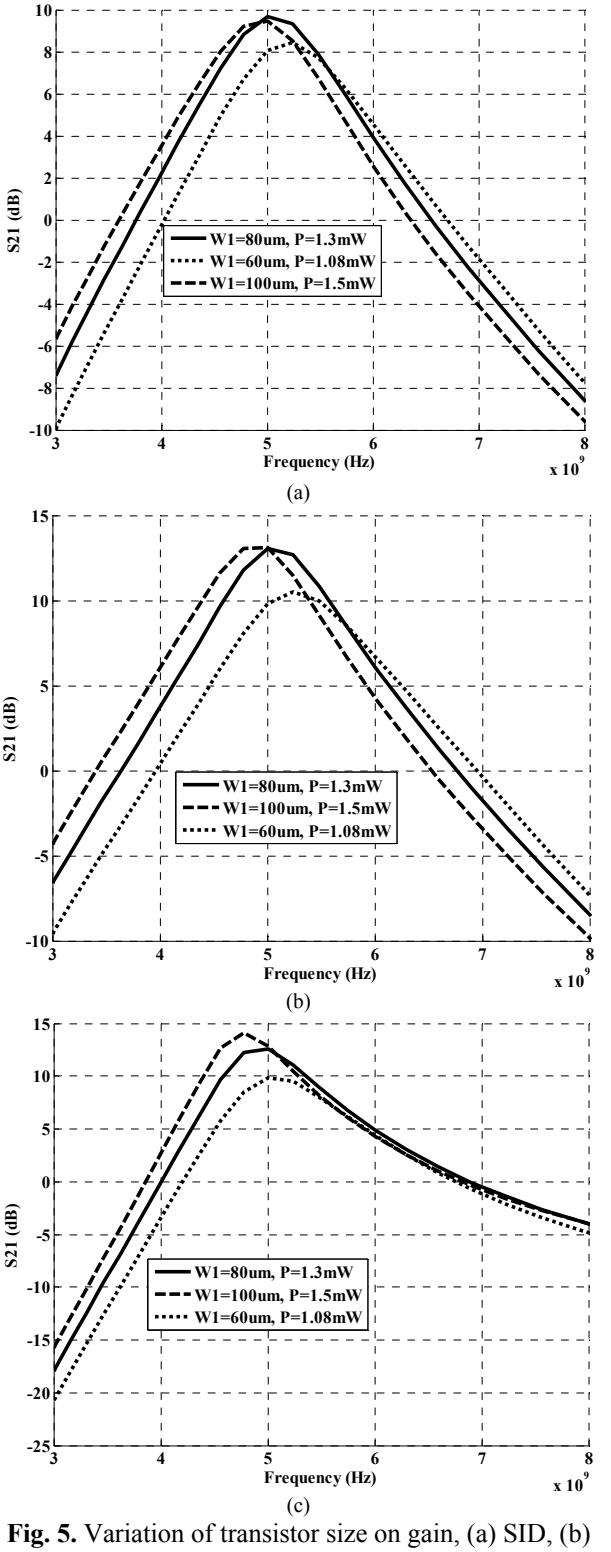
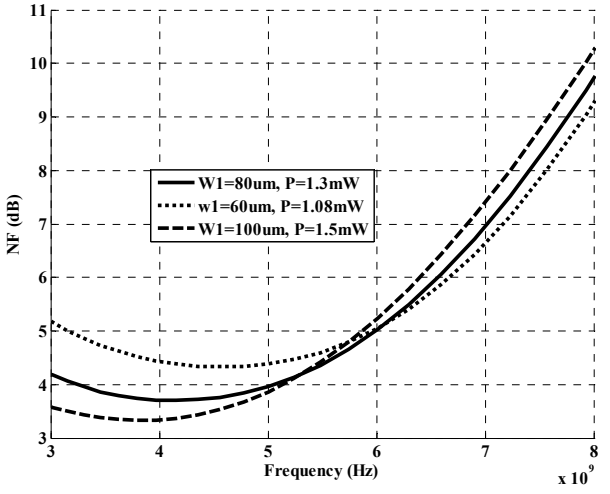
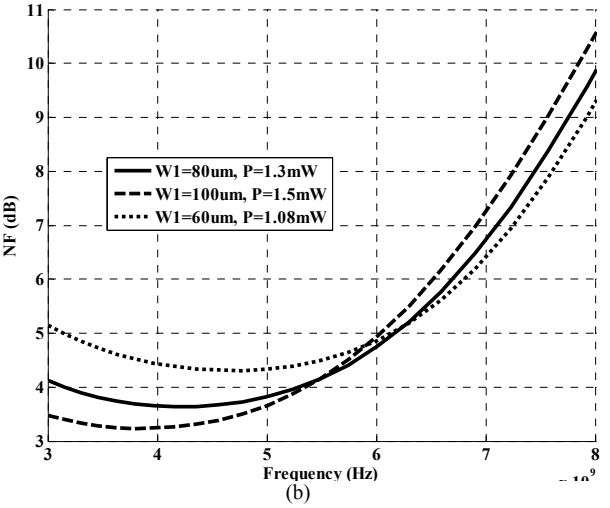


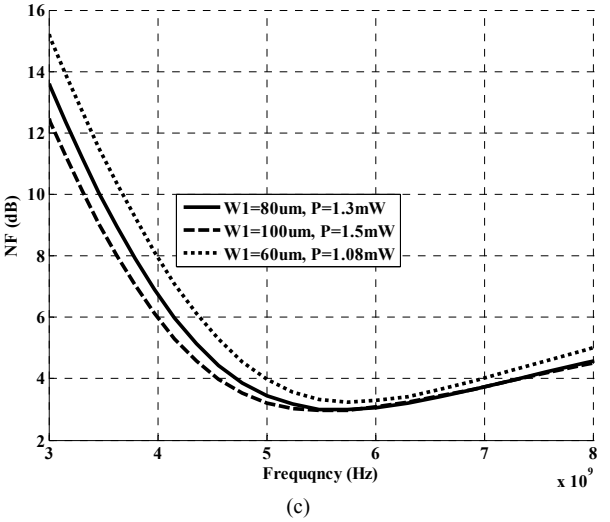
Fig. 5. Variation of transistor size on gain, (a) SID, (b) SI, (c) PI matching.



(a)

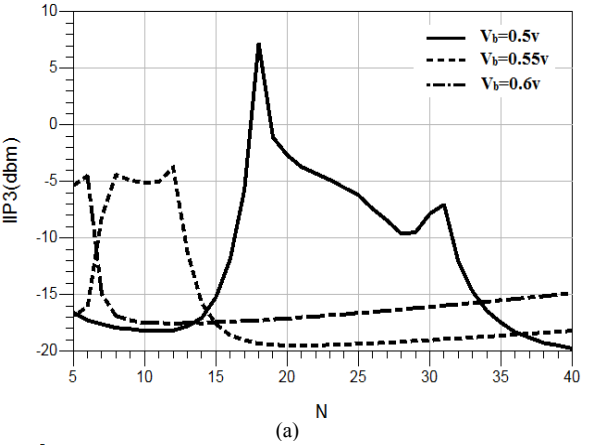


(b)

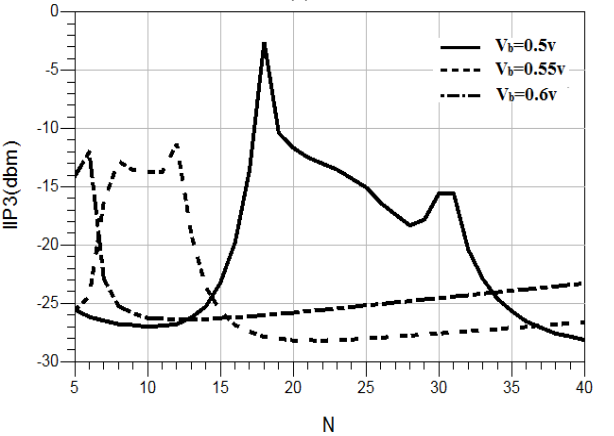


(c)

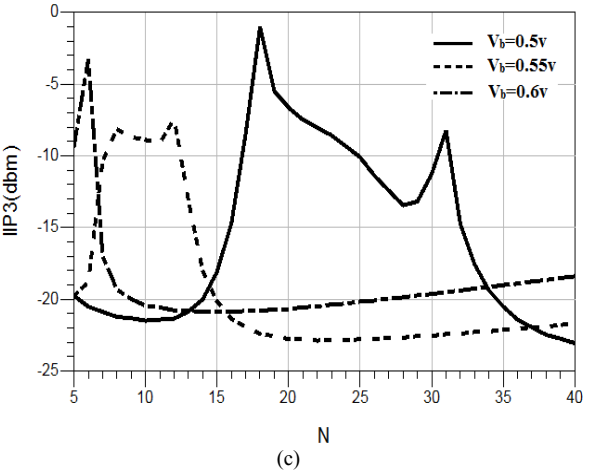
Fig. 6. Variation of transistor size on noise figure, (a) SID, (b) SI, (c) PI matching.



(a)

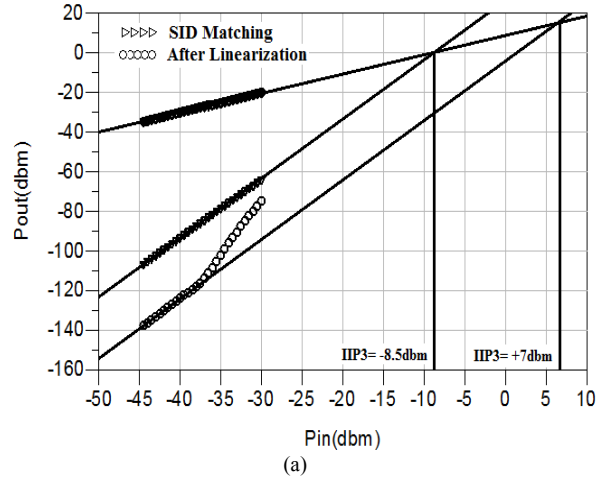


(b)

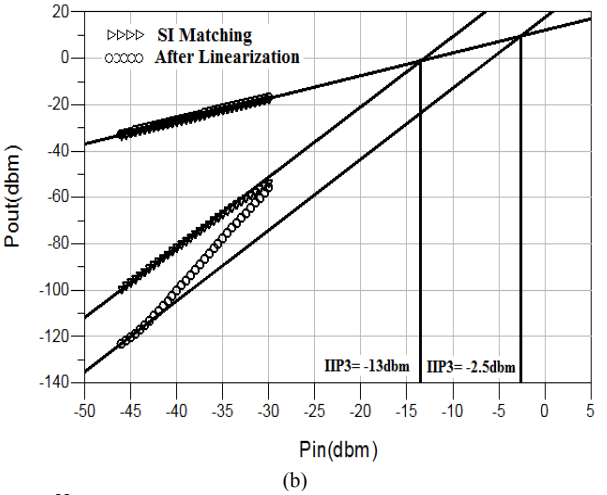


(c)

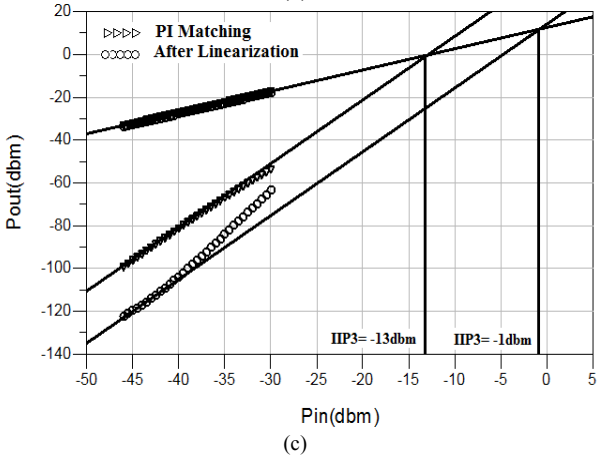
Fig. 7. The simulated IIP3 versus the fingers of M3 for various value of Vb, (a) SID, (b) SI, (c) PI matching.



(a)



(b)



(c)

Fig.8. IIP_3 simulated values before and after linearization for (a)SID, (b) SI, (c) PI matching.

The characteristics of LNAs are described below. The values of noise figure are 3.9 dB, 3.8 dB and 3.5 dB for SID, SI, and PI matching, respectively. The gain of SID matching is 10 dB, and using SI and PI methods for input impedance matching caused to increase gain from 10 dB to 13.5 dB and 12.3 dB, respectively.

The isolation S_{12} is less than –25 dB over the bandwidth. All of the elements are realized on the chip. Performance summary and comparison results of three input impedance matching are indicated in Table 1. It can be seen in this table that each input impedance matching has its pros and cons and according to application and design requirements, one of them can be chosen. For example, for highly linear applications, SID matching can be the best choice, while for low noise applications, PI matching is the best option.

To evaluate the performance of low voltage low power LNAs, different figures of merit (FOMs) are commonly used in the literature. One figure of merit (FOM_1) of the LNA is the ratio of the gain in dB to the supply voltage in volt. The SID, SI, and PI LNAs described in this work have values of 16.66, 22.6, and 20.4 for this FOM_1 after linearization, respectively. Furthermore, FOM can be extended to include the power consumption, linearity, and noise figure:

$$FOM_2 = \frac{gain\ (abs).IIP_3(mW)}{NF\ (abs).V_{dd}(v).power\ (mw)} \qquad (33)$$

As can be clearly seen from table 1, because of having high IIP3, the SID method has the highest FOM than other methods.

Table 1. Performance summary of folded cascode topologys and comparision of results

		NF(dB)	S21(dB)	S11(dB)	S22(dB)	IIP3(dBm)	Power(mW)	FOM1	FOM2
SID Matching	Before linearization	3.9	9.2	-20	-10	-8.5	1.29	15.33	0.56
	After linearization	3.9	10	-23	-17	+7	1.26	16.66	3.69
SI Matching	Before linearization	3.8	12.37	-14	-7	-13	1.3	20.6	0.49
	After linearization	3.8	13.56	-11	-12	-2.5	1.28	22.6	2.54
PI Matching	Before linearization	3.5	12.7	-11	-9	-13	1.3	21.16	0.98
	After linearization	3.5	12.25	-9	-13	-1	1.28	20.4	2.1

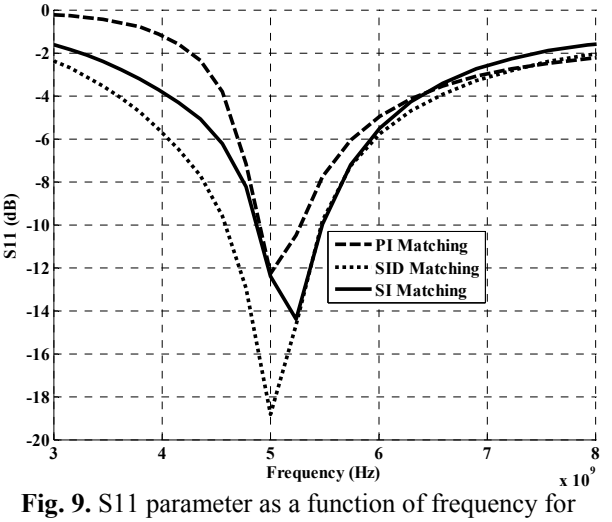


Fig. 9. S11 parameter as a function of frequency for three different of input matching

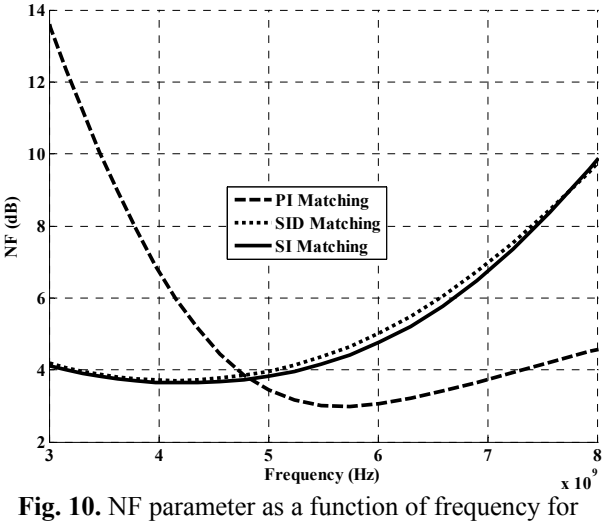


Fig. 10. NF parameter as a function of frequency for three different of input matching

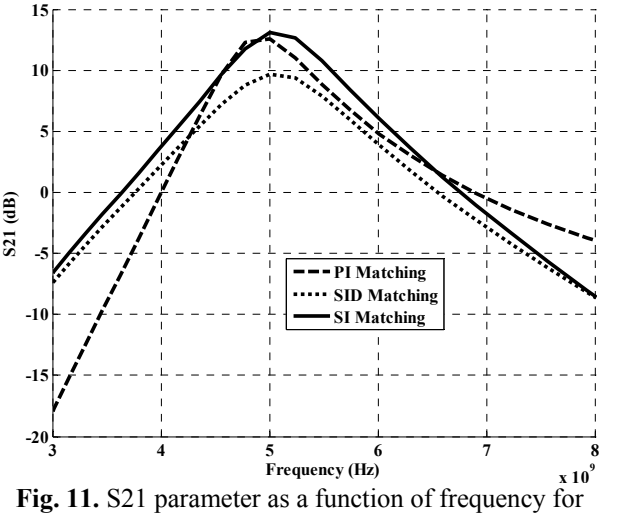


Fig. 11. S21 parameter as a function of frequency for three different of input matching

8. SUMMARY

Design of RF CMOS LNAs using the parasitic input resistance of a MOSFET was presented. The effect of using three different input matching methods on the gain and noise performance of the LNAs was investigated in detail. It was shown that using parasitic gate resistance for input impedance matching enhances the gain of the LNA by a factor of $(50/R_{inM})^{1/2}$ in the desired frequency band.

To demonstrate the merits and drawbacks of proposed methods, low voltage low power LNAs for 5 GHz application using 0.18µm CMOS technology were presented. It was shown that by employing folded cascode configuration, the fully integrated LNA can operate under the condition of low supply voltage of 0.6 V, consuming only 1.3 mW dc power. Furthermore, by introducing a new linearization technique, the IIP3 of LNAs was improved without any significant effect on other LNA parameters. The simulation results showed that the LNAs are suitable for low power and low voltage applications.

REFERENCES

[1] E.Kargaran, Gh.Nabovati, M.R.Baghbanmanesh. Kh.Mafinezhad and H.Nabovati, **"An ultra low voltage ultra high gain cmos LNA using forward body bias technique"** *in proceeding of IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Seoul, Korea,2011.

[2] E.Kargaran, M.Mohammad Kazemi, **"Design of 0.5V, 450µW CMOS LNA Using Current Reuse and Forward Body Bias Technique,"** *in Proceeding IEEE 5th European Conference on Circuits and Systems for Communications (ECCSC'10)*, Belgrade, Serbia, November ,2010, pp 93-96.

[3] S.Asgaran, M.J.Deen and C.H.Chen, **"A 4-mW monolithic CMOS LNA at 5.7 GHz with the gate resistance used for input matching,"** *IEEE Microwave and Wireless Components Letters* , vol. 16, no. 4, p. 188 - 190, 2006.

[4] H. W. Chiu, S. S. Lu, and Y.-S. Lin, **"A 2.17-dB NF 5-GHz-band monolithic CMOS LNA with 10-mW dc power consumption,"** *IEEE Trans. Microw. Theory Tech*., vol. 53, no. 3, pp. 813–824, Mar. 2005.

[5] C. H. Liao and H. R. Chuang, **"A 5.7 GHz 0.18 µm CMOS gain-controlled differential LNA with current reuse for WLAN receiver,"** *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 12, pp. 526–528, Dec. 2003.

[6] E. Kargaran, H.Kargaran and H.Nabovati , **"A 0.6v Ultra-High-Gain Ultra-Low-Power CMOS LNA at 1.5GHz in 0.18µm Technology ,"** *in Proceeding IEEE 2nd International Conference on Computer and Electrical Engineering (ICCEE)* , December 2009, pp. 123-125.

[7] E.Kargaran, H.Khosrowjerdi, K.Ghaffarzadegan and H.Nabovati, **"A 5.7GHz low noise figure ultra high gain CMOS LNA with inter stage technique,"** *IEICE Electron. Express*, Vol. 7, No. 23, pp.1686-1693, 2010.

[8] D. Linten, S. Thijs, M. I. Natarajan, P. Wambacq, W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Donnay, and S. Decoutere, **"A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS,"** *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1434–1442, Jul. 2005.

[9] D. Linten, L. Aspemyr,W. Jeamsaksiri, J. Ramos, A. Mercha, S. Jenei, S. Thijs, R. Garcia, H. Jacobsson, P.Wambacq, S. Donnay, and S. Decoutere, **"Low-power 5-GHz LNA and VCO in 90-nm RF CMOS,"** *in Dig. Tech. Papers IEEE Symp. VLSI Technology*, Jun. 2004, pp. 372–375.

[10] M. N. El-Gamal, K. H. Lee, and T. K. Tsang, **"Very low-voltage (0.8-V) CMOS receiver front-end for 5-GHz RF applications,"** *Proc. IEE Circuits, Devices, Syst.*, vol. 149, pp. 355–362, 2002.

[11] X. Jin, J. Ou, C.-H. Chen, W. Liu, M. J. Deen, P. R. Gray, and C. Hu, **"An effective gate resistance model for CMOS RF and noise modeling,"** *Dig. Tech. papers IEDM*, pp. 961–964, Dec. 1998.

[12] S. Asgaran, M. J. Deen, and C.-H. Chen, **"Analytical modeling of MOSFET's channel noise and noise parameters,"** *IEEE Trans. Electron. Devices*, vol. 51, no. 12, pp. 2109–2114, Dec. 2004.

[13] Y. Cheng, M. J. Deen, and C.-H. Chen, **"MOSFET modeling for RFIC design,"** *IEEE Trans. Electron. Devices*, vol. 52, no. 7, pp. 1286–1303, Jul. 2005.

[14] M. J. Deen, C. H. Chen, S. Asgaran, A. Rezvani, J. Tao, and Y. Kiyota, **"High-frequency noise of modern MOSFETs: Compact modeling and measurement issues,"** *IEEE Trans. Electron. Devices*, vol. 53, no. 9, pp. 2062–2081, Sep. 2006.

[15] E. Kargaran, G. Nabovati, K. Mafinezhad and H.Nabovati, **"An Ultra Low Voltage Ultra Low Power Folded Cascode CMOS LNA Using Forward Body Bias Technology for GPS application,"** *in the Proceedings of the IEEE 19th Iranian Conference on Electrical Engineering (ICEE)*, Tehran, Iran, May 2011.

[16] S. Maas, **Nonlinear Microwave and RF Circuits**, Artech House Publishers, 2003.

[17] V. Aparin and L. E. Larson, **"Modified derivative superposition method for linearizing FET low-noise amplifiers,"** IEEE Trans. Microw. Theory Tech., vol. 53, no. 2, pp. 571–581, 2005.

[18] E.Kargaran, et al, **"Gain increasing techniques for CMOS folded cascode LNAs at low voltage and low power operations,"** *in proceeding of IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, USA,2012.

[19] M.J.Zavarei, E.Kargaran, and H.Nabovati, **"New linearization method for low voltage, low power folded cascode LNAs,"** *in proceeding of IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, USA,2012.