A 3.1-10.6 GHz HEMT Distributed Amplifier for Ultra-Wideband Application

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ABSTRACT:

In this paper, a Distributed Amplifier (DA) by using HEMT technology for ultra-wideband application is presented. Creation of Distributed integrated circuit has been investigated for approximately seventy years rapidly to developing semiconductor process technologies in the modern IC design. By using of this method, multiple parallel signals are combined and obtain to increase the bandwidth, enhanced power combining amplitude, and novel design capabilities for IC process. The circuit was designed and simulated in ED02AH technology by using ADS2010. The 4-stage design achieves 15.5 dB of power gain (±0.5 dB) from 3.1 to 10.6 GHz. Reflected power of the input and output from loads matched to 50 Ohm are all below -10 dB over the bandwidth of the device, as is power transmitted from the output to the input. The device is stable for a wide range of input and output loads.

KEYWORDS: Distributed Amplifier (DA), Ultra-Wideband Amplifier, Traveling Wave Amplifier (TWA), HEMT Technology, Advanced Design System (ADS).

1. INTRODUCTION

The fundamental of distributed amplification was originally applied to vacuum tubes structures [1]. The principle has been applied in many other devices, including lasers, traveling wave tubes and, most relevant to us, microwave amplifiers. Because of its broad range of applications, extensive literature exists in the subject [2] contain many references in this literature.

In a common source microwave FET distributed amplifier, a discrete component transmission line is constructed out of the drain-source input admittance – the drain line. Another identical transmission structure is the gate-source input admittance of the gate line. If the transmission structures are identical, a wave can be launched on the gate line and be coherently amplified onto the drain line. It is a simple matter to construct transmission lines with identical properties of the gate and drain lines assuming a unilateral transistor over a very wide range of frequencies. Thus, these devices are naturally wideband. Furthermore, by using FET parasitics as a part of the transmission lines, some FET limitations can be avoided.

Certainly, one of the most resourceful examples of distributed circuit design conceived is the distributed amplifier (DA) formulated by William S. Percival in 1936 [3]. In that year, Percival proposed a design by

that the transconductances of individual vacuum tubes could be added linearly, therefore, arriving at a circuit that attained a gain bandwidth product greater than that of an individual tube. Percival's design did not gain widespread awareness. However, until a publication on the subject was authored by Ginzton, Hewlett, Jasberg, and Noe in 1948 [4]. It is to this later paper which the term distributed amplifier can actually be traced.

Traditionally, DA design architectures have been realized utilizing III-V semiconductor technologies, such as GaAs [5]-[7] and InP [8],[9], due to the superior performance of these technologies resulting from these technologies' higher bandgaps (higher electron mobility), higher saturated electron velocity, higher breakdown voltages and higher-resistivity substrates. The latter contributes much to the availability of higher quality-factor (Q-factor or simply Q) integrated passive devices in the III-V semiconductor technologies. Even so, in order to meet the marketplace demands on size, cost, and power consumption of monolithic microwave integrated circuits (MMICs), ongoing research continues on the development of mainstream digital bulk-CMOS processes for such purposes. The continuous scaling of feature sizes in current IC technologies has enabled microwave and mm-wave CMOS circuits to benefit directly from the result of increaseing unity-gain

frequencies of the scaled technology. This device scaling, along with the advanced process control available in today's technologies, has recently made it possible to reach an fT of 170 GHz and a maximum oscillation frequency (fmax) of 240 GHz in a 90nm CMOS process [10].

2. THEORY OF OPERATION

The operation of the DA can perhaps be most easily understood when explained in terms of the traveling wave amplifier (TWA) illustrated in Figure1. As seen in the figure, the DA consists of a pair of transmission lines with characteristic impedances of Z0 independently connecting the inputs and outputs of several active devices. An RF signal is thus supplied to the section of transmission line connected to the input of the first device. As the input signal propagates down the input line, the individual devices respond to the forward traveling input step by inducing an amplified complementary forward traveling wave on the output line. This assumes the delays of the input and output lines are made equal through intelligent selection of propagation constants and lengths of the two lines and as such the output signals from each individual device sum in phase. Terminating resistors Zg and Zd are placed to minimize destructive reflections
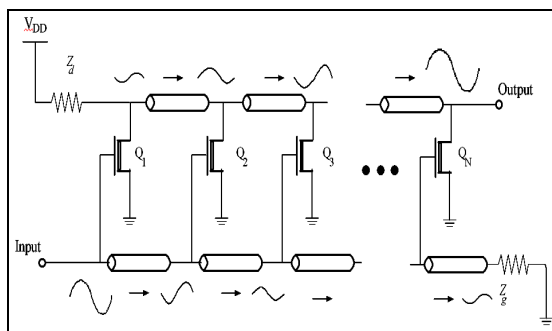

Fig. 1. TWA illustration of the DA

Denoting the transconductive gain of each device as gm and recognizing that the output impedance seen by each transistor is half the characteristic impedance of the transmission line one arrives at the overall voltage gain of the DA being [11]

$$AV = ng_mZ_0/2 \qquad (1)$$

Neglecting losses the gain demonstrates a linear dependence on the number of devices (stages). Unlike the multiplicative nature of a cascade of conventional amplifiers, the DA demonstrates an additive quality. It is this synergistic property of the DA architecture that makes it possible for it to provide gain at frequencies beyond that of the unity-gain frequency of the individual stages in a matched system. In practice the number of stages is limited by the diminishing input signal resulting from attenuation on the input line.

Means of determining the optimal number of stages are discussed in the subsequent section. Bandwidth is typically limited by impedance mismatches brought about by frequency dependent device parasitics.

Another way of understanding the benefits of the DA topology is recognize that the architecture realizes a distributed wideband matching network through absorption of the device parasitics into the matching network itself. In order to achieve greater gain from a conventional single device amplifier one would simply increase the size (width) of the device as desired. However in order to provide adequate matching the matching networks (input and output transmission lines) must then be implemented with progressively higher characteristic impedances in order to compensate for the larger input and output parasitic device capacitances. Subsequently, the design of the input and output matching networks becomes increasingly difficult as design tolerances makes the physical realization of these high impedance values impractical. In an IC implementation of the DA the tolerances of high characteristic impedance distributed matching networks are made difficult to maintain through virtue of the unavoidable process variations present within any given fabrication technology. Another limiting feature of large-sized devices within the context of the distributed amplification is revealed when considering the Bragg cutoff frequency of the parasitically loaded transmission lines. The Bragg cutoff frequency of the transmission lines within a distributed matching network can be roughly computed by

$$\omega_c \approx 2/\sqrt{L_{TL}(C_{TL}+C_{device})} \qquad (2)$$

where C is the sum of the line segment capacitance and L is the total inductance of the line segment and the parasitic loading capacitance upon the line segment [11]. Therefore, it can be readily seen that increasing the device size in order to realize larger gains simultaneously lowers the cutoff frequency of the distributed matching network. Thus, by providing a means of achieving increased gain without substantially increasing device size the DA achieves a physically realizable wideband amplifier with performance greater than that possible through traditional amplifier designs.

3. SIMULATION RESULT

The HEMT Distributed Amplifier was simulated by Advanced Design System (ADS2010). Figure2 illustrates the schematic diagram of the proposed DA. To obtain appropriate power gain, four-stage conventional distributed amplifier was used. Figure 4 and Figure 5 show the S-parameters and the noise figure of the DA respectively. As seen in the Figure 3, gain (S21) is 15.5dB with ±0.5dB flatness cover from 3.1 GHz to 10.6 GHz. The input and output return losses are less than -10dB as shown in figure 4. The

reverse isolation S12 is -16dB or better over the whole bandwidth. The noise figure is between 2.5dB and 4.2dB. Power consumption of the DA is only 49mW. Figure 6 shows that the device is stable for wide range of input and output loads. Table 1 summarizes the performance of the DA.
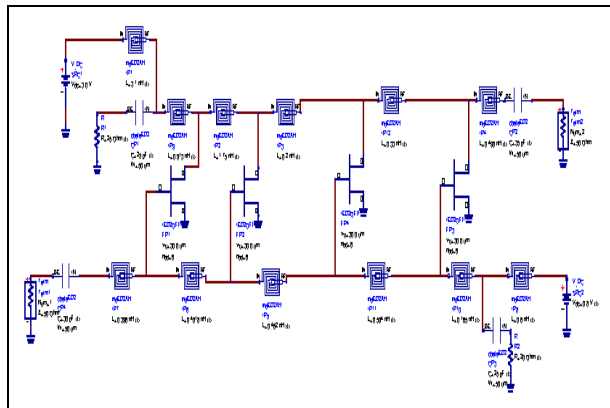

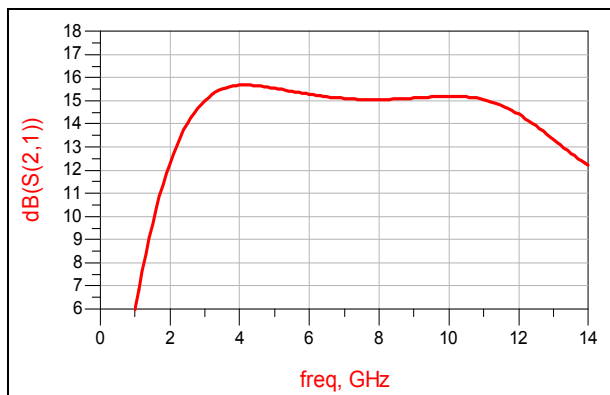**Fig. 2.** Proposed Schematic diagram of DA for Ultra-Wideband application

Fig. 3. Gain (S21) of Proposed DA for Ultra-Wideband application
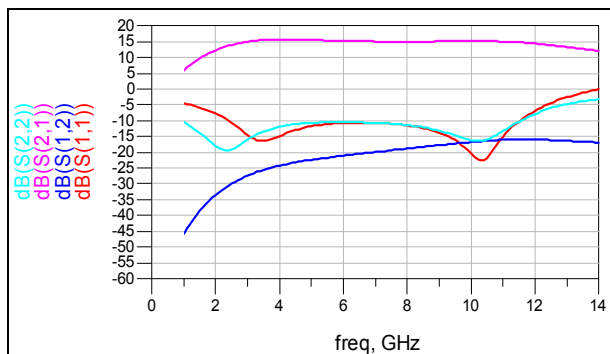

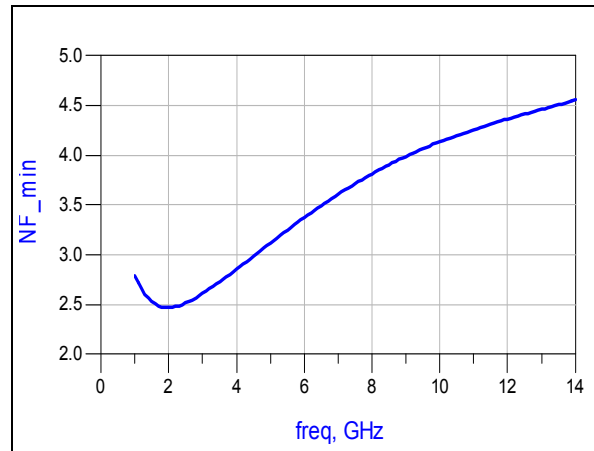**Fig. 4.** S-parameter of proposed DA for Ultra-Wideband application

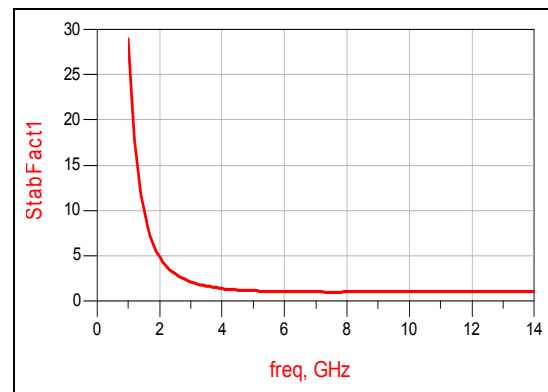**Fig. 5.** Noise Figure of proposed DA for Ultra-Wideband application

Fig. 6. Stability Factor of proposed DA for Ultra-Wideband application

Table 1. Performance summary of DA

	Simulation Results
Technology	HEMT(ED02AH)
Frequency(GHz)	3.1-10.6
Power Supply(V)	3
Gain(S21)	15
Input Return loss(S11)	< -10
Noise Figure	< 4.2
Output Return loss(S22)	<-10
Isolation(Sl2)	<-16
Power Consumption(mW)	49

The recently reported performances of distributed amplifiers compared with this work are summarized in Table 2.

Table 2. Recently Reported Performances of DA

reference	[12]	[13]	[14]	[15]	This work
process	0.6μm CMOS	0.35μm CMOS	0.18μm CMOS	0.35μm BiCMOS	HEMT
BW(GHz)	4	5	14	10.5	7.5
Gain(dB)	6.5	21	10.6	12	15.5
S11(dB)	-7	-10	-11	-8	-10
S22(dB)	-10	-10	-12	-8	-10
VDD(V)	3	2.2	1.3	1	3
Power Consumption (mW)	83.4	132	52	40	49

4. CONCLUSION

In this paper, a HEMT distributed amplifiers has been proposed. We have successfully applied these results to implement a wideband distributed amplifier with respectable gain, noise, input match and output match characteristics. Four-stage conventional distributed amplifier was used to achieve 15.5 dB with ±0.5dB flatness cover from 3.1 GHz to 10.6 GHz. Reflected power at the input and output from loads matched to 50 Ohm are all below –10 dB over the bandwidth of the device. The device is stable for broad range of input and output loads.

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