Analysis of a New Quasi Parallel Resonant DC Link (QPRDCLI)

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ABSTRACT:
Soft switching techniques have recently been used for the design of DC-AC converters, in order to achieve better performance, higher efficiency and power density. One of the soft switching techniques applied in inverters is resonant DC links. These topologies have some disadvantage such as irregular current peak, large voltage peaks, uncontrollable pulse width, etc. Another soft switching method in inverters is using quasi resonant links, which have PWM modulation capability. In this paper, an inverter with a new quasi resonant parallel DC link with capability EDPWM (Enhanced Double PWM) which uses of single-phase soft switching technique (SPSS) is introduced. This circuit provides the inverter with two to three ranges of PWM control capability, which increases the switching time control is the larger range. Various operational stages of this new quasi resonant DC link and designing process are analyzed. Finally, simulation results of new QPRDCLI and some other samples by PSPICE software are presented to justify the circuit operation.

KEYWORDS: Inverter, Soft switching, QRDCL, PWM, Losses, EDPWM, SPSS.

1. INTRODUCTION

Inverters extensively used in industrial usage such as uninterruptible power supplies (UPS), emergency power supplies, AC & DC drives, frequency converters, etc. From view of switching situation, inverters can be divided into two categories: Hard switching inverters & Soft switching inverters. Hard switching inverters included Voltage Source Inverters (VSI) and Current Source Inverters (CSI). Voltage source inverters and current with pulse width modulation, considering to the simple structure of power circuit and capabilities of the pulse width modulation, apply widely in power supply and drive motors. Hard switching inverters have some problems such as high stress on circuit switches (Voltage & current), large SOA, high switching losses, high di/dt & dv/dt (which causes EMI) which limits the inverter's work frequency, so soft switching inverters used for decreasing the switching losses and increasing the inverter work frequency in zero voltage situation (ZVS) and / or zero current situation (ZCS). Furthermore, soft switching causes decreasing of EMI and noise sonic. Topologies of soft switching can be described in figure (1).

Inverters with resonant DC & AC link are suitable choices for soft switching. Resonant AC link because of complexity to the power circuit and control and also utilizing of bidirectional switches which are so expensive, is less useable [2].

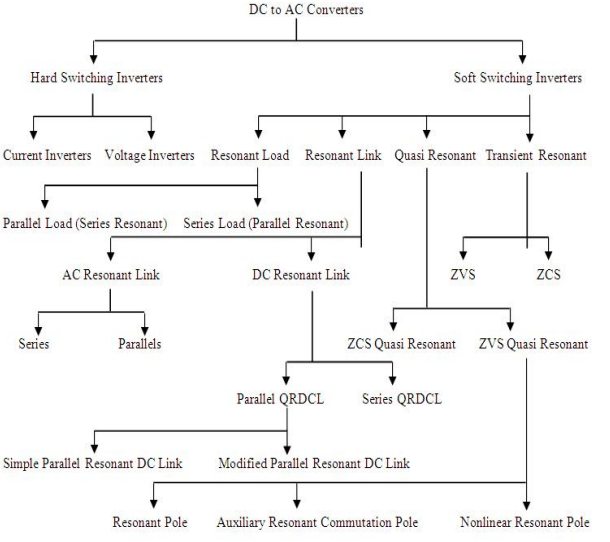


Fig. 1. DC/AC Topologies

In resonant DC link, the link voltage is pulse and this causes changing of inverter's main switches when voltage is zero. Defects of these inverters are high peak of the link voltage and unused PWM modulation. That

for removing the first defect can use of passive clamp circuits or active clamp circuits or an auxiliary quasi circuit in which link voltage peak in the sequent will be limited about 2.5, 1.8 and 1.5 against of input source DC voltage [3-4]. For removing the second defect can use of inverters with modified resonant DC link or inverters with resonant auxiliary commutation pole [5] or inverters with quasi resonant DC link [6 to 16] which from them, inverters with quasi resonant DC link are more suitable. The main characteristic of these inverters is that resonant circuit operates only when the link voltage reaches to zero and back to its prime situation and in other times, the resonant circuit will be completely out of control. By controlling the resonant circuit switches, when the link voltage reaches to zero can be adjusted based on the necessity of PWM modulation, also the voltage peak in these inverters should be equal to input source DC voltage.

In this paper, with doing some changes to the source circuit [6], the capability of width pulse modulation on both up and down edges of the link voltage up to three areas and also possibility of turning off the switches carrier current when the link voltage is not zero has been provided. Then, while studying the circuit behavior, the mathematics equations for the circuit will be exploited and also the procedure of designing the circuit will be studied. Finally, the results of simulation will be compared with some other quasi resonant DC link.

2. THE NEW CIRCUIT OFFER AND ITS WORK

One suitable criterion for selecting the quasi resonant DC link is the capability of PWM modulation on circuit. By using the technique of Enhanced Double PWM modulation (EDPWM) can use PWM at both two edges up and down link voltage which causes increasing the capability of circuit's time control. With adding one switch to the resonant circuit source [6] in figure (2), can add the EDPWM capability to the circuit and increase PWM modulation on both two up & down edges of link voltage. Also with distributing the link capacitors on main switches in inverter in figure (3), can use of single phase soft switching (SPSS) to turn off the main switches in circuit when link voltage is not zero.

The procedure of SPSS technique has been shown in figure (4). If assumed that S1 carries current so by turning it off, the circuit will transmit to its parallel Cr capacitor and after charging that capacitor and discharging the bottom Cr capacitor at that phase, the current will be transmit to the Dp1 diode. In this case the current's main switch can be turned off under the soft switching situation.

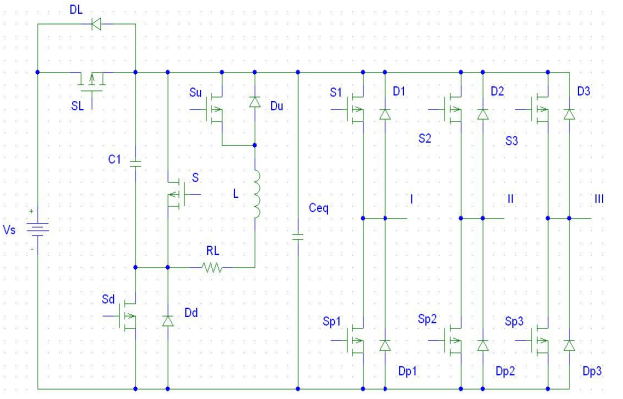


Fig. 2. New parallel quasi DC link inverter with EDPWM capability

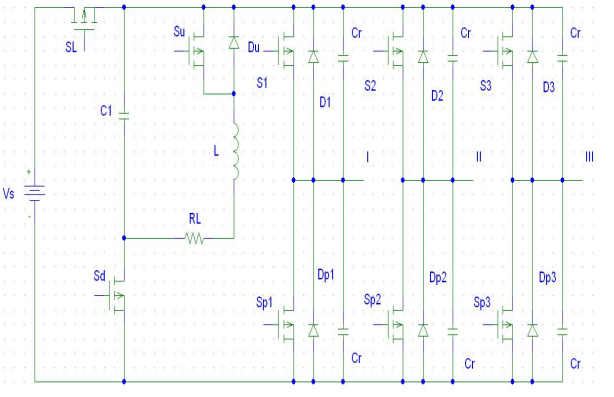


Fig. 3. New quasi DC Link inverter parallel with distributed link capacitor on the main switches

In the offered inverter circuit, the link voltage control system made of small Cr, small L, small C1 and four auxiliary switches.

With timely OFF and ON the auxiliary switches, the link voltage can be zero when needed and after changing the inverter's main switches in ZVS, the link voltage can be returned to the normal condition. The added S switch can be bidirectional; in this case the circuit has the PWM capability in three areas.

In this paper for simplifying the analysis, the S switch has been assumed to be unidirectional.

For analyzing the procedure of this system, the equaled circuit in figure (5) has been described.

Cr capacitors with a Ceq have been equaled. The value of Ceq during each switching frequency period will be equal to 3Cr because there is an ON switch by in each phase which made its parallel capacitor inactive. Do is equal to anti parallel diodes of inverter's main switches and prevents the link voltage to be negative. The Io current source is output current, and be assumed stable during a switching frequency period with consider to the filters inductance or load. So is equal to two switches on one phase of inverter or the total switches.

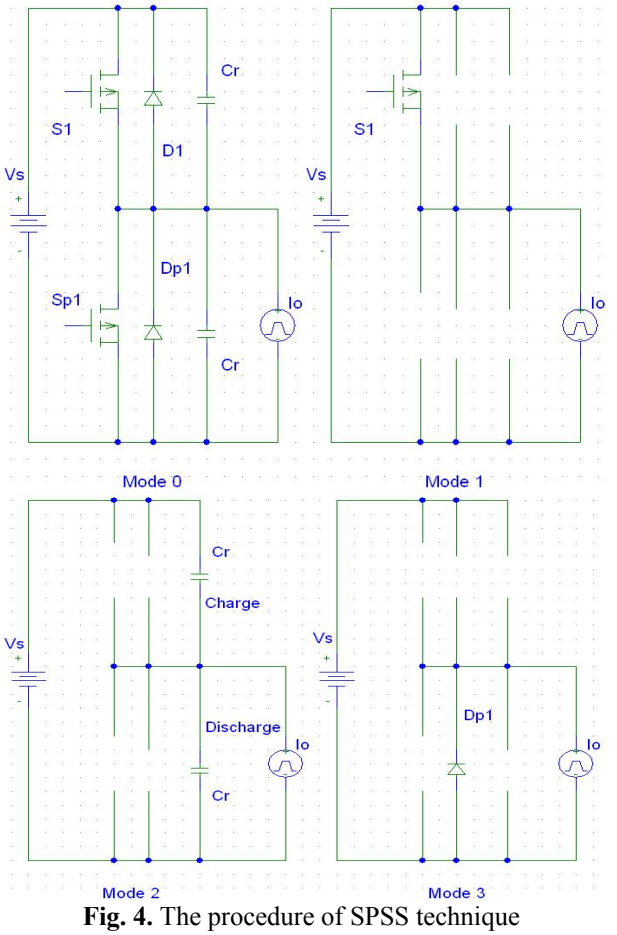


Fig. 4. The procedure of SPSS technique

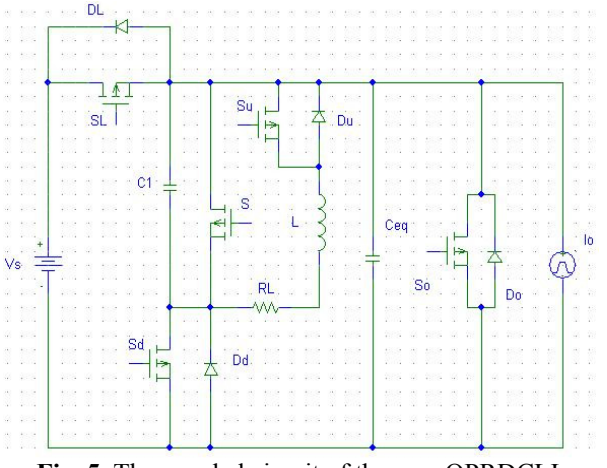


Fig. 5. The equaled circuit of the new QPRDCLI.

The circuit has seven stages of procedure as follows:

2.1. Stage zero (t0-t1): The stable condition status

In this stage SL and Sd are ON and the other auxiliary switches are OFF. The time of this stage TPWM1 is completely under controlled and independent from the circuit's parameters. In figure (6) the equaled circuit has been shown.

The equations on circuit are as follows:

$$V_{C1}(t) = V_{Ceq}(t) = V_S \quad (1)$$

$$i_L(t) = 0 \quad (2)$$

$$T_0 = T_{pwm1} = ControllableTime \quad (3)$$

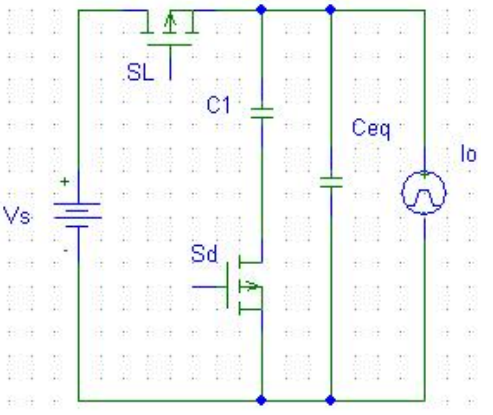


Fig. 6. The inverter's equal circuit in stage zero

2.2. Stage one (t1-t2): Induction current linear increase status

In this stage Su in ZCS is ON. Induction current will be increased linearly to Ip. In figure (7) the equal circuit of this stage has been shown.

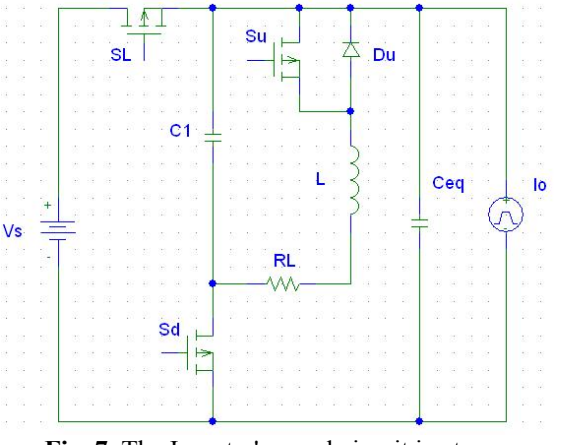


Fig. 7. The Inverter's equal circuit in stage one.

The equations on circuit are as follows:

$$V_{C1}(t) = V_{Ceq}(t) = V_S \quad (4)$$

$$i_L(t) = \frac{V_S}{L}(t - t_1) \quad (5)$$

$$T_1 = t_2 - t_1 = \frac{I_p}{V_S}L \quad (6)$$

$$i_L(t) = I_p \quad (7)$$

T1 considered as the stage one time and will increase by enhancing the Io value.

2.3. Stage two (t2-t3): The resonant status between L and Ceq and C1

In this stage, SL under ZVS is off. Induction L and capacitors (Cr and C1) in this stage are resonations and decreased of capacitor's voltage to zero and increased the induction current to the maximum value. In figure (8) the equal circuit in this stage has been shown.

The equations on circuit are as follows:

$$i_L(t) = (I_p + I_o)Cos\omega_1(t-t_2) + \frac{V_S}{Z_o}Sin\omega_1(t-t_2) - I_O \quad (8)$$

$$V_{C1}(t) = V_{Ceq}(t) = -(I_p + I_o)Z_o Sin\omega_1(t-t_2) + V_S Cos\omega_1(t-t_2) \quad (9)$$

$$i_L(t_2) = I_p = \frac{V_S}{Z_O}Cos(\omega_1 T_2) - I_O \quad (10)$$

$$i_L(t_3) = I_{L\max} \quad (11)$$

$$V_{C1}(t_3) = V_{Ceq}(t_3) \quad (12)$$

$$T_2 = t_3 - t_2 = \frac{1}{\omega_1}Sin^{-1}\left(\frac{V_S}{V_S + 2Z_O I_O}\right) \quad (13)$$

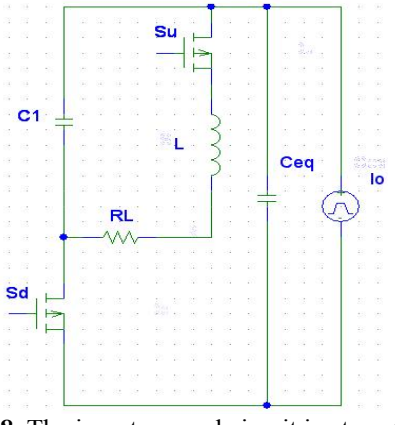


Fig. 8. The inverter equal circuit in stage two

In which ILmax ≈ (Vo/Zo) + Io, ω1 = 1 / (LC)½, C= Ceq+C1, Zo = (L/C)½. T2 (the time of this stage) decrease with increasing of the Io.

2.4. Stage three (t3-t4): The resonant status between C1 and L.

The start of this stage will be when the link voltage reaches to zero. In this status the Sd in soft mood is Off and So under ZVS becomes ON. C1 and L so keep to the resonation till capacitor C1 voltage reach to negative peak and back to zero again. As far as the induction current is positive, the Su conduct and when the induction current becomes negative, Du start to conduct and the Su in completely soft status is off. Mean time the output current Io continues from So or Do. In figure (9) the equal circuit of this stage has been shown.

The equations on circuit are as follows:

$$i_L(t) = I_{L\max}Cos\omega_2(t-t_3) \quad (14)$$

$$V_{C1}(t) = V_{Cl_{\max}}Sin\omega_2(t-t_3) \quad (15)$$

$$V_{Ceq}(t) = 0 \quad (16)$$

$$V_{C1}(t_4) = V_{Ceq}(t_4) = 0 \quad (17)$$

$$i_L(t_4) = -I_{L\max} \quad (18)$$

$$T_3 = t_4 - t_3 = \frac{\pi}{\omega_2} \quad (19)$$

In which ω2 = 1 / (LC1)½, VC1max = ω2.L.Imax and T3 considers as the time of this stage and is independent from the output current and only depend on the value of C1 and L.

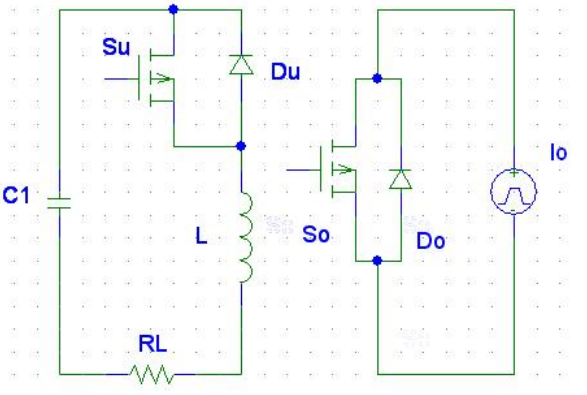


Fig. 9. The inverter equal circuit in stage three

2.5. Stage four (t4-t5): The stable situation status

In this stage the S under ZVS is ON. The induction current via Du and S, plugs its path. The time in this stage (TPWM2) will be completely under controlled. In figure (10) the equal circuit of this stage has been shown.

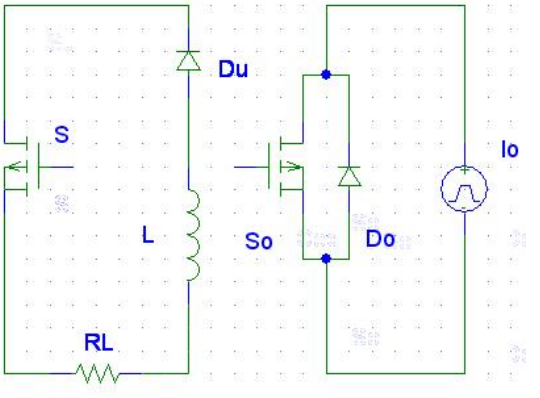


Fig. 10. The inverter equal circuit in stage four

The equations on the circuit are as follows:

$$i_L(t) \approx -I_{L\max} \quad (20)$$

$$V_{C1}(t)=V_{Ceq}(t)=0 \quad (21)$$

$$T_4 = T_{pwm_2} = Controllab\ \ leTime \quad (22)$$

2.6. Stage five (t5-t6): The resonant status between L and C1 and Ceq

In this stage the S and So in soft mood are OFF and the Sd in ZVS becomes ON and Du keeps to be ON. The resonant occurs between L and Ceq and C1 which causes the increase of capacitor's voltage to Vs value and induction current reaches to Io value. In figure (11) the equal circuit of this stage has been shown.

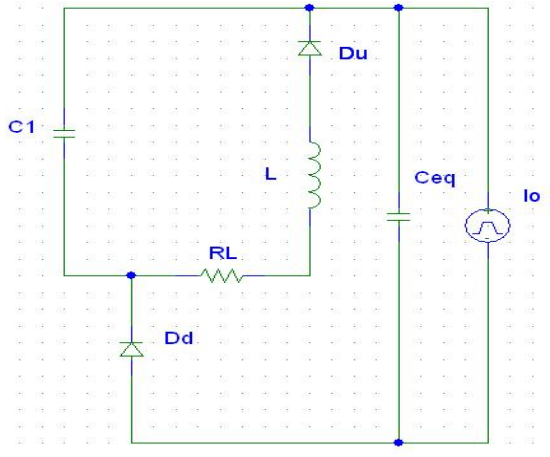


Fig. 11. The inverter equal circuit in stage 5

The equations on the circuit are:

$$V_{C1}(t)=V_{Ceq}(t)=(I_{L_{\max}}-I_O)Z_O Sin\omega_1(t-t_5) \quad (23)$$

$$i_L(t)=(I_O-I_{L\max})Cos\omega_1(t-t_5)-I_O \quad (24)$$

$$V_{C1}(t_6)=V_{Ceq}(t_6)=V_S \quad (25)$$

$$i_L(t_6)=-I_O \quad (26)$$

$$T_5=t_6-t_5=\frac{\pi}{2\omega_1} \quad (27)$$

The time of this stage T5 is independent from the output current and only depends on the Ceq and C1 and L values.

2.7. Stage six (t6-t7): L current linear decrease status.

When voltage of C1 and Ceq reaches to Vs value, this stage starts. In this stage the SL is ON under ZVS and causes the excess discharge of induction current and control circuit restoration the link voltage to its prime status. In figure (12) the equal circuit of this stage has been shown.

The equations on the circuit are:

$$i_L(t)=\frac{V_S}{L}(t-t_6)-I_O \quad (28)$$

$$V_{C1}(t)=V_{Ceq}(t)=V_S \quad (29)$$

$$i_L(t_7)=0 \quad (30)$$

$$V_{C1}(t_7)=V_{Ceq}(t_7)=V_S \quad (31)$$

$$T_6=t_7-t_6=\frac{I_O}{V_S}L \quad (32)$$

The time of this stage T6 increase with enhancing the output current.

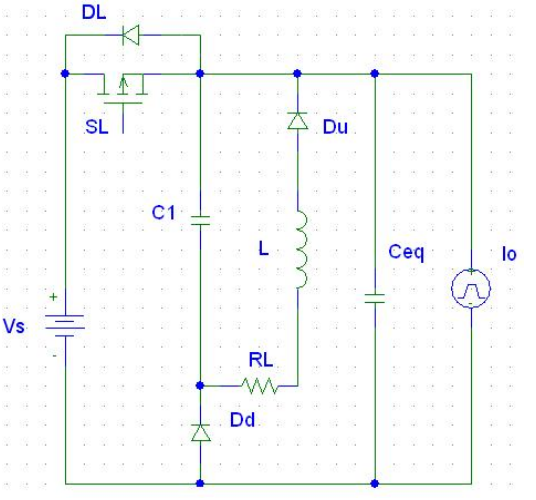


Fig.12. The inverter equal circuit in stage six.

When induction current becomes zero the process of making the link voltage zero and reversing it to the normal status completes. The time takes for this process calculated via the following equation which consider to the TPWM2 is completely under controlled.

$$T=\frac{1}{\omega_1}Sin^{-1}\left(\frac{V_S}{V_S+2Z_O I_O}\right)+\frac{\pi}{\omega_2}+T_{pwm2}+\frac{\pi}{2\omega_1} \quad (33)$$

If S is bidirectional between the status 2 and status 3 a situation will be added which causes the increase of PWM area. In figures (13) to (18) the changes of T based on the different parameters of the circuit has been shown.

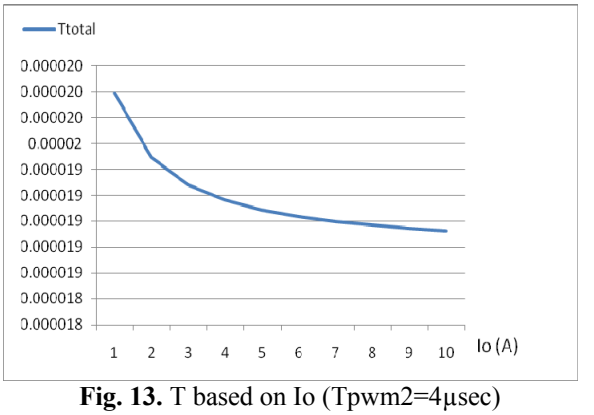
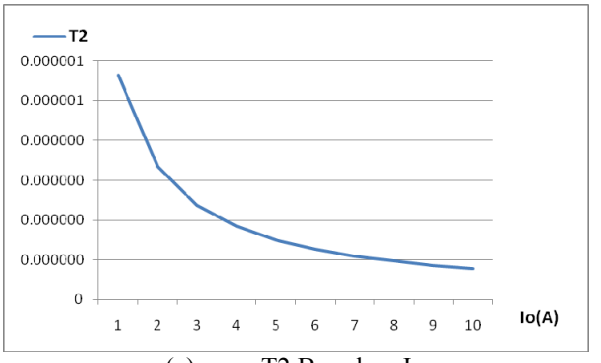
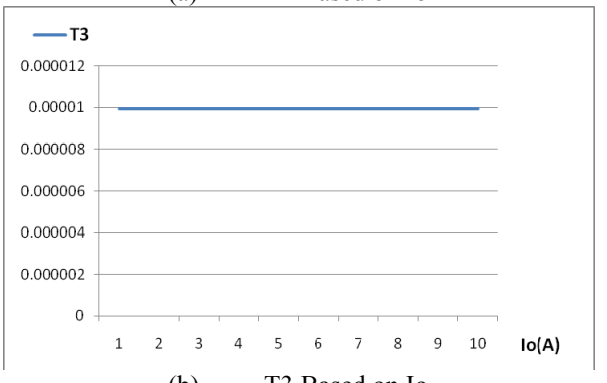


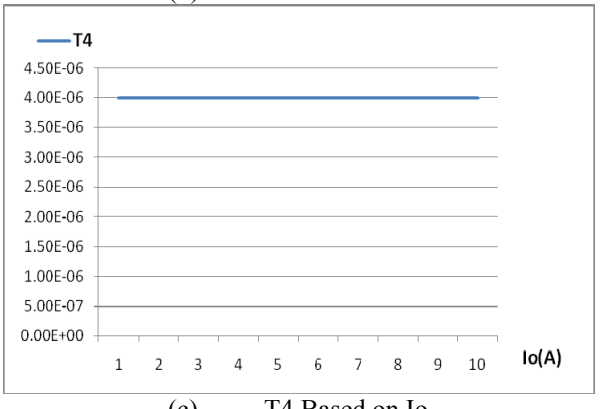
Fig. 13. T based on Io (Tpwm2=4µsec)



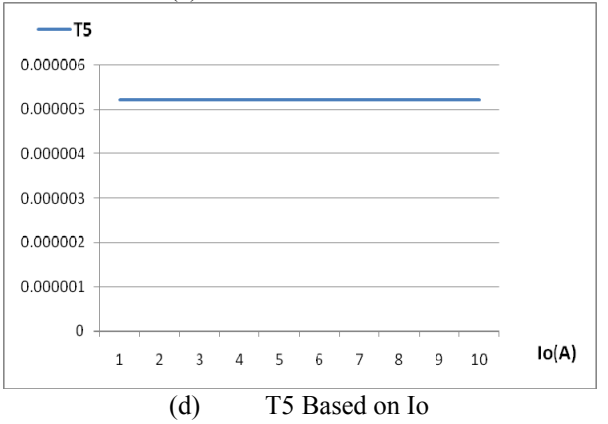
(a) T2 Based on Io



(b) T3 Based on Io



(c) T4 Based on Io



(d) T5 Based on Io

Fig. 14. The changes of T2,T3,T4,T5 based on Io

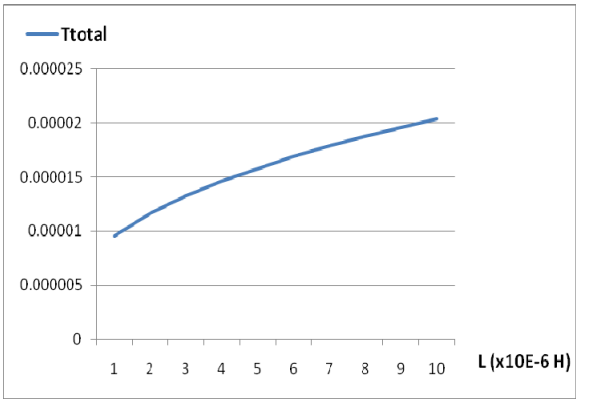


Fig. 15. The changes of T based on L

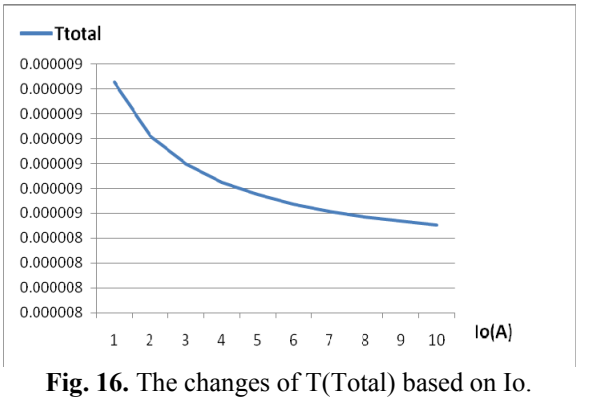


Fig. 16. The changes of T(Total) based on Io.

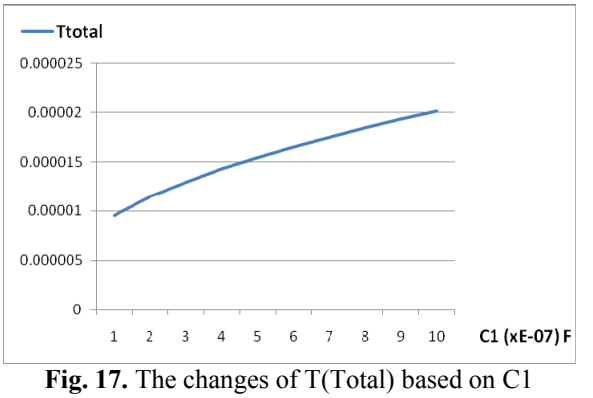


Fig. 17. The changes of T(Total) based on C1

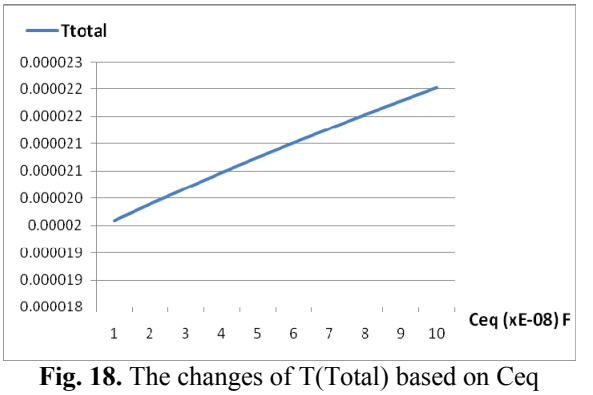


Fig. 18. The changes of T(Total) based on Ceq

Table 1. The various stages of the new QPRDCLI

Stages / Switches	0 t0-t1	1 t1-t2	2 t2-t3	3 t3-t4	4 t4-t5	5 t5-t6	6 t6-t7
S_L	ON	ON	OFF	OFF	OFF	OFF	OFF
D_L	OFF	OFF	OFF	OFF	OFF	OFF	ON
S_D	ON	ON	ON	OFF	OFF	OFF	OFF
D_D	OFF	OFF	OFF	OFF	OFF	ON	ON
S_u	OFF	ON	ON	ON	OFF	OFF	OFF
D_u	OFF	OFF	OFF	ON	ON	ON	ON
S	OFF	OFF	OFF	OFF	ON	OFF	OFF

3. DESIGNING ELEMENTS OF THE OFFERED INVERTER

For designing the elements of the offered inverter based on decreasing the total losses can act as per the following method. The first selected element is Cr. The criterion for selecting this capacitor calculated based on the time of the circuit's commutation from the switch carrier the current to its reversed paralleled diode in one phase which is not more than a standard limit. If load current assumed stable during the commutation operation the following equation can be considered by using of figure (19).

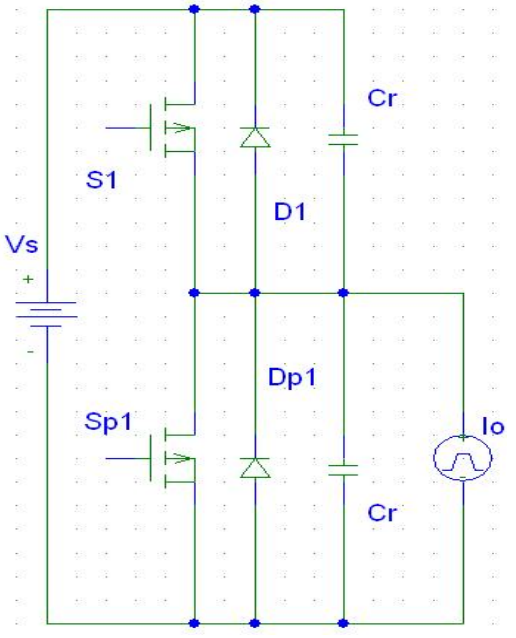


Fig. 19. Current commutation in new inverter's single phase switches.

$$I_{out} = 2C_r \frac{dv_O}{dt} \tag{34}$$

By using of (34) equation and having the minimum output current, Cr capacitor value can be selected so that the time takes for changing Vo output voltage from zero to Vs vice versa doesn't excess from a standard limit. This standard limit can be considered about %1.5 to %10 of the time takes in a frequency switching period.

It needs to be mentioned that capacitance of Cr should not be very small because it causes the increase of switches switching losses. From that the amount of switching losses in a quasi resonant link circuit depends on the capacitance of resonant capacitor and link frequency and must be in the least amount, the switching frequency can be gotten from the following equation [17]:

$$P_{SW_{\min}} = \frac{K_{LOSS} \cdot f}{C} \tag{35}$$

In which Kloss is a stable value and obtain from the following equation [17]:

$$K_{LOSS} = \frac{I_a^2 . t_f^2}{24} \tag{36}$$

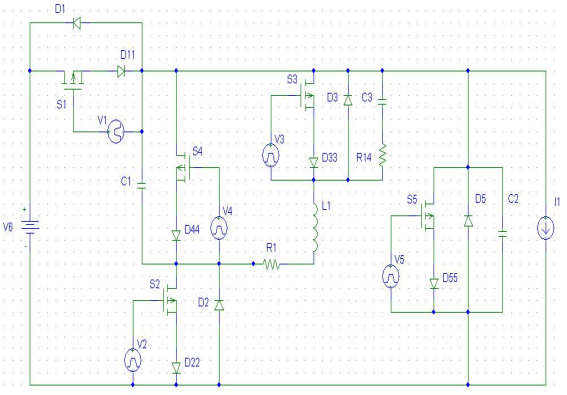
In which Ia is the transmitted current from switch when the switch is Off and tf is time when the switch is Off. For calculating L the following equation can be used [17]:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{37}$$

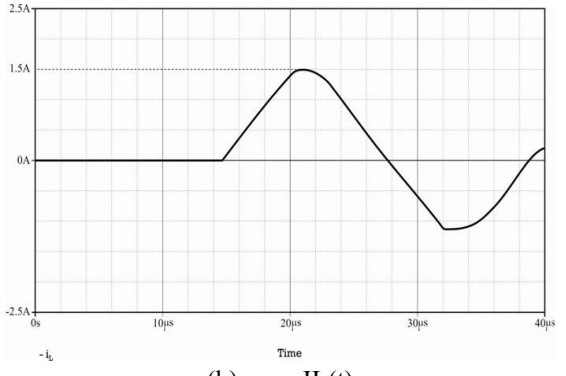
It needs to be mentioned that the L value should not be less than a standard limit for two reasons. The first reason is that if the resonant induction value be less than the leakage induction value due to the circuit the L has an undesirable affect on the resonant frequency. Finally the L value must be major than the total values of leakage inductions. The second reason is that with consider to the reference of the link voltage at the end of switching frequency period to its prime value induction L should save a definite value of energy in order that the restoration operation of link voltage to the prime status occurs exactly.

4. THE SIMULATION OF INVERTER WITH A NEW PARALLEL QUASI RESONANT DC LINK

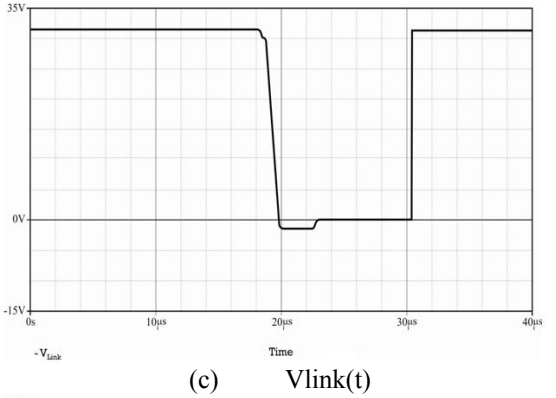
The equal circuit of inverter with new parallel quasi resonant DC link has been analyzed for 25 KHz frequency with Ceq and C1 capacitance with values 0.1µF and 0.01µF, L with 100µH value and 10Ω resistance, 35Vdc input voltage and 1.5A output current and by using of power-mosfet IRF640 and MR876 diodes, by PSPICE software. The wave of induction current and the voltage of the resonant capacitor and the losses energy in new parallel quasi resonant DC link and the references [6], [7] and [8] obtained from analyzing the software have been shown in figures (20) to (23) in sequent.



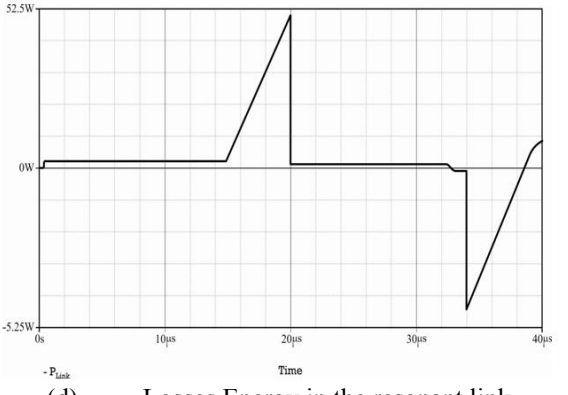
(a) Simulation new QPRDCLI.



(b) IL(t)

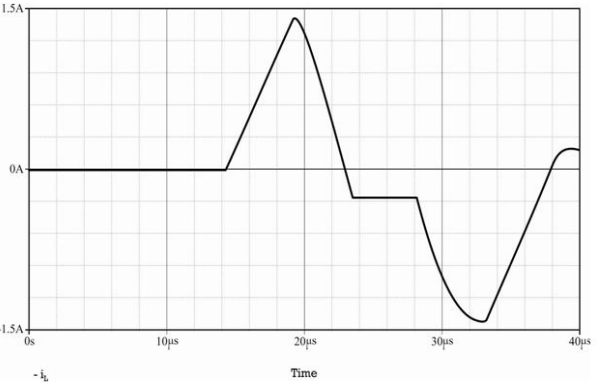


(c) Vlink(t)

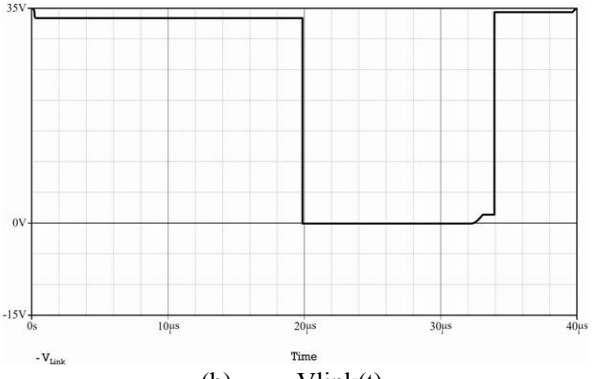


(d) Losses Energy in the resonant link.

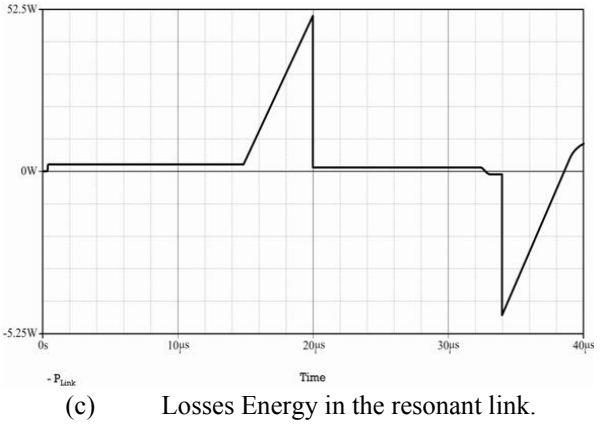
Fig. 20. Waves of reference [6]



(a) IL(t)

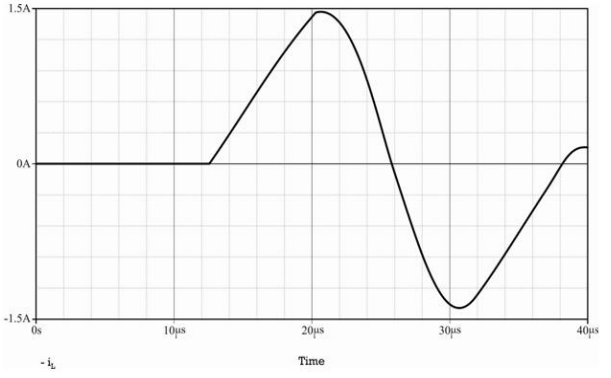


(b) Vlink(t)

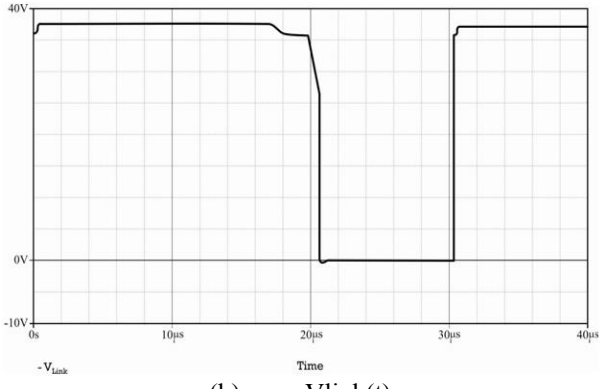


(c) Losses Energy in the resonant link.

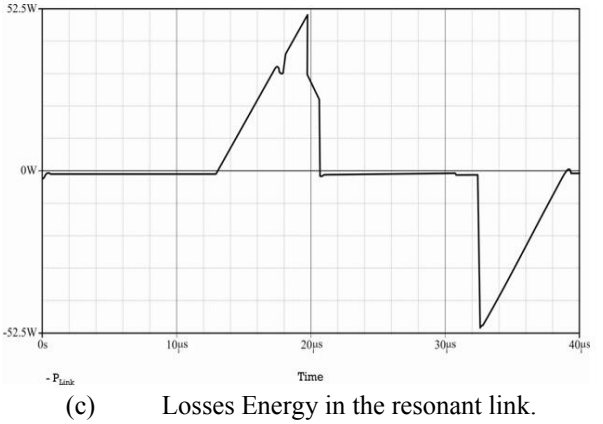
Fig. 21. Waves of reference [7]



(a) IL(t)

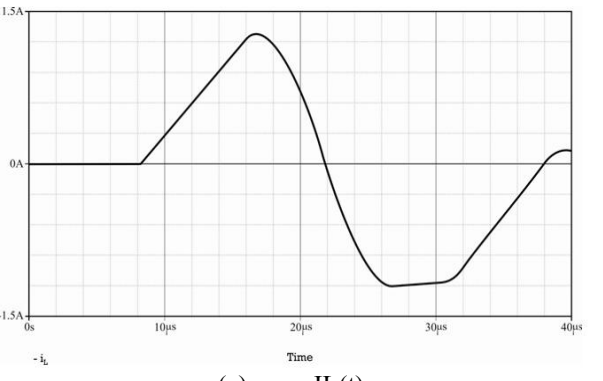


(b) Vlink(t)

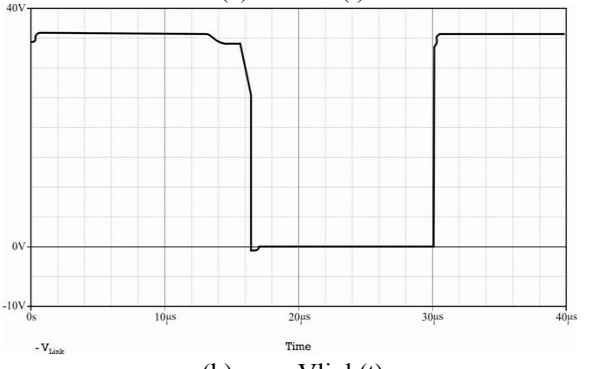


(c) Losses Energy in the resonant link.

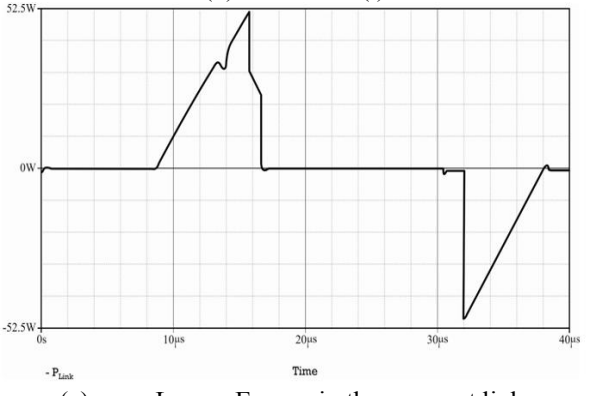
Fig. 22. Waves of reference [8]



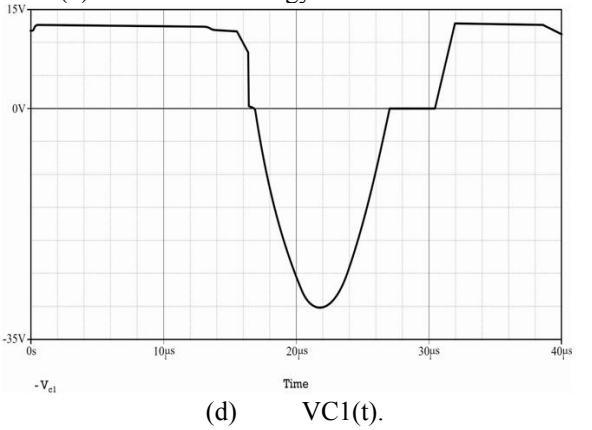
(a) IL(t)



(b) Vlink(t)



(c) Losses Energy in the resonant link.



(d) VC1(t).

(e)

Fig. 23. Waves of new quasi resonant DC link

Table (2) compares the total results of losses in the link obtained from analyzing the new parallel quasi resonant DC link and references [6], [7] and [8] at two simulation status and equations on circuits which shows the results conform to each others.

Table 2. Comparison of link's losses results the references [6], [7], [8] with new QRDCLI

Circuit	P(link) Simulation	P(link) Mathematical relations
[6]	2.36W	2.40W
[7]	2.14W	2.16W
[8]	2.29W	2.35W
New	2.75W	2.78W
L=100μH, RL=10mΩ, Ceq=0.01μF, C1=0.1μF, VDC=35V, Io=1.5A, fs=25KHz, Diode:MR876, Switch: IRF640		

5. COMPARISON OF NEW QRDCLI WITH SOME OTHER CIRCUITS

In this chapter, references [6], [7], [8] have been compared with new QPRDCL view points of the used number of elements, the PWM capability, benefit of SPSS technique and maximum of voltages on auxiliary and main switches which these shown in Table-2. The numeral values of maximum of the auxiliary and main switches voltage has been normalized based on DC voltage.

As you see, the maximum voltage of the offered inverter's main switches will limit on bias voltage which causes the decrease of voltage stress on switches, so the more energy transmitted by using switches which have lower voltage maximum. Also the capability of PWM implementation on both two up and low edges of link voltages causes the increase of controlling the switching time in a wider area. In Table-3 the offered circuit has been compared with some other quasi resonant dc link view point of the number of elements, capability of PWM implementation, using of single-phase soft switching technique and elements' voltage.

Table 3. Comparison of new QPRDCLI with some other circuits

Circuit	Switches	PWM Capability	SPSS Capability	Max Voltage Switches
[6]	4	1 range	Yes	1
[7]	3	1 range	No	1
[8]	4	2 range	No	1
New	4	3 range	Yes	1

6. CONCLUSION

In this paper, an inverter with new parallel quasi resonant DC Link has been offered. The offered circuit view point of complexity and the number of elements employed in compare of the existent parallel quasi resonant DC links is acceptable. In addition, in this offered inverter the capability of pulse width modulation in two areas exists and uses of single phase soft switching technique. The maximum voltage of the offered circuit main switches limits in input voltage which causes the decrease of voltage stress on switches.

The results of the offered circuit's simulation and the comparison with other circuits are explanatory of the following subjects:

- With using of SPSS technique, stress of the switches and switching losses decrease. Meantime consider to the distributed capacitors on circuit main switches, the switches have been conserved and doesn't need to the snubber external circuit.
- EDPWM capability in offered inverter causes increase the time control of switching in a wider area.
- In the offered inverter because of EDPWM capability, if output current peak changes due to the change of input voltage or change of load. TPWM2 can be adjusted arbitrary instead of changing the values of resonant elements. The decreasing of the induction energy limits is this time.

With consider that in the offered inverter has been used from quasi resonant DC link circuit the total time of switching depends on the input voltage's and output circuit's values, the decreased time can be modified in 1 & 6 stages with controlling TPWM2 & TPWM1, otherwise time stages with each other and resonant occurs speedy and inverter operatively voids from soft switching situation and circuit losses increase.

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