Designing Low Dropout Regulator with Low Settling Time, High Power Supply Rejection and Low Line and Load Regulation

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ABSTRACT:
Low dropout regulators are one of the most important factures of many portable devices. Thus, consider to the complexity of the circuits and increasing request for portable devices, for increasing battery life and minimizing supply noise, regulators with high efficiency, low output noise and small size is required. In this paper, two methods to improve the efficiency of LDO regulators is proposed. First method is increasing gain of the error amplifier by using cascode technique, to improve steady-state specification. Second method is using a simple subtractor circuit between error amplifier and pass transistor of LDO regulator to improve power supply rejection, slew-rate and steady-state specification. In addition, both methods are used to achieve area efficiency replacing MIM capacitors with MOS transistor. These low dropout regulators have been simulated in TSMC 0.18 µm CMOS process. Simulation results show enhancement settling time, good line and load regulation and power supply in compare with others LDO regulators.

KEYWORDS: Load regulation, Low dropout regulator, Line regulation, Power supply rejection, Slew-rate enhancement.

INTRODUCTION

Low-dropout regulator is widely used in many portable devices such as cellar phone, notebooks and MP3 players, for generating a stable and accurate supply voltage [1], [2]. Fig. 1 presents the topology of conventional LDO. A LDO regulator is usually composed by a pass element (power transistor), an error amplifier, a driver, a voltage reference, and a resistive feedback network. The topology of a LDO is connected as a closed loop. The feedback type is a series-shunt negative feedback to dynamically control the pass element. The pass element is usually a power PMOS transistor to reduce dropout voltage. Dropout voltage, Line, and load regulation are steady-state specifications of linear voltage regulation. These parameters in Fig. 1 are presented in the following relation [3]:

$$V_{dropout} = V_{in} - V_{out} = V_{DSSat(p)} \quad (1)$$

$$Line\ Regulation = \frac{\Delta V_{out}}{\Delta V_{in}}|_{DC} = \frac{g_{mp} r_{dsp}}{1 + A_{V0}\beta} + \frac{1}{\beta}.\frac{\Delta V_{ref}}{\Delta V_{in}} \quad (2)$$

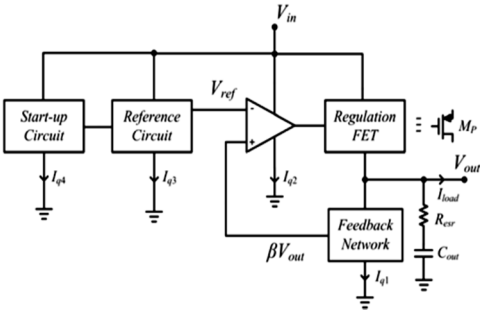

Fig. 1 .Topology of conventional LDO

where ΔV_{in} , ΔV_{out} and ΔV_{ref} are the variation of input, output, and reference voltage, respectively. Furthermore, $r_{dsp}, g_{mp}, A_{V0}\beta$, and β are output resistance and transcondactance of pass transistor, regulation loop gain, and feedback factor in DC position and therefore:

$$R_{out} = \frac{\Delta V_{out}}{\Delta I_{load}} = \frac{r_{dsp}}{1 + A_{V0}\beta} \quad (3)$$

where ΔI_{load} is variation of load current.

Power supply rejection is sensitive to the circuit to power supply noise in different conditions. This parameter is presented in the following relation [4]:

$$PSR = \frac{\Delta V_{out}}{\Delta V_{in}}|_{AC} \quad (4)$$

So far, many methods have been proposed to reduce the PSR, including RC filter in series with a power supply is used in reference [5]. Refrence [6] suggests the NMOS transistor, in which the gate of the transistor is free from noise by the RC filter and then, is applied to feed the gate of the pass transistor. Reference [7] has added a processing block in the regulation loop to reduce the PSR in the intermediate frequency and in the structure of reference [8] two transistors with cascode arragement is used to supply load current and more separation of V_{out} and V_{dd} , synchronistically.

In section II, the structure of LDO regulator by using MOSFET capacitors, that have considered as a base regulator has been studied. In section III, a method for reduce power supply rejection is discussed. Proposed LDO regulators are presented in section IV. Simulation results have been illustrated in section V, and finally, section VI is dedicated to the conclusion.

SCRUTINY OF THE LDO REGULATOR WITH MOS CAPACITORS

In reference [9] integrated MOS transistor capacitor instead of metal-isolator-metal (MIM) capacitor has been suggested. In addition, area efficiency has been achieved by replacing these capacitors with MOS capacitors, and location of the pole and zero of the implanted transfer function are adaptively changed according to the value of load current. Figure 2 shows structure of proposed LDO regulator along with frequency MOSFET compensation capacitors. Figure 3 shows the corresponding small-signal equivalent circuit. Assuming R_{c1} to be large, the effect of C_{c1} on the first stage output via i_c is negligible because of the relatively output low induced ac current. The transfer function is thus obtained as follows:

$$\frac{V_{fb}}{V_{in}} \approx \cdots \approx \frac{LG_0\left(1+{}^{S}/_{Z_1}\right).\left(1+{}^{S}/_{Z_2}\right)}{\left(1+{}^{S}/_{p_1}\right).\left(1+{}^{S}/_{p_2}\right).\left(1+{}^{S}/_{p_3}\right).\left(1+{}^{S}/_{p_4}\right)} \quad (5)$$

$$LG_0 = \cdots = g_{mi}g_{ms}g_{mn}g_{ml}R_iR_sR_n\left(R_L \parallel (R_{F1}+R_{F2})\right)\frac{R_{F2}}{R_{F1}+R_{F2}} \quad (6)$$

$$Z_1 = 1/R_{c1}\,C_{c1} \quad (7)$$

$$Z_2 = 1/\left(R_{c2} - 1/g_{mp}\right) \quad (8)$$

$$P_1 = 1/R_s(C_s + C_{c2}\left(1 + g_{mp}\left(R_L \parallel (R_{F1}+R_{F2})\right)\right)\Big) \quad (9)$$

$$P_2 = 1/\Big((R_L \parallel (R_{F1}+R_{F2}) \parallel R_S)(C_S + C_L)\Big) \quad (10)$$

$$P_3 = 1/R_iC_i \quad (11)$$

$$P_4 = 1/(C_S + C_{c2})(R_{c1} \parallel R_S) \quad (12)$$

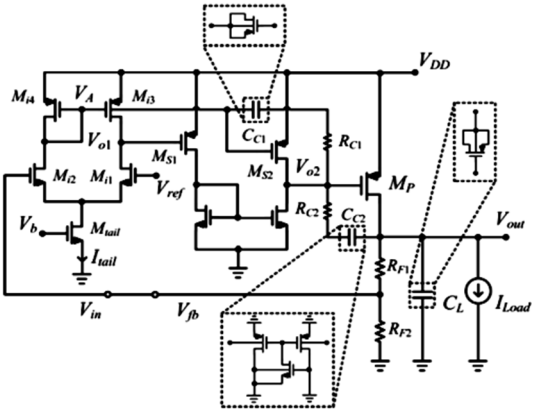

Fig. 2 . Detailed schematic of MOSCAP-compensated LDO[9]

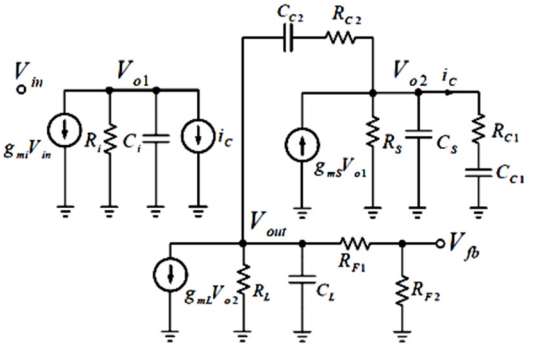

Fig. 3 . The equivalent small-signal circuit of the loop [9]

C_{C2} dominates the pole at the input of pass device (i.e. p_1) and pushes output pole (p_2) to relatively higher frequencies (well known pole-splitting action in Miller compensation [3]). R_{c2} in series with C_{C2} creates a LHP zero (z_2), which cancels out the undesirable effect of high frequency poles (P_3, P_4). As C_{C2} is SCDM and R_{c2} is constant, the magnitude of Z_2 is not affected by the ripples of output due to load current changes. This is not however true for C_{C1}, which is an uncompensated MOSCAP. As a result, z_1 which is produced by this capacitor becomes a function of the load current. The LHP pole located at the output of LDO increases

linearly with the load current according to the following well-known expression:

$$P_2 \approx 1/r_{DSP}C_L = \lambda_p I_{Load}/C_L \quad (13)$$

where r_{DSP} and λ_p are the output resistance and channel length modulation of pass device, respectively. The zero introduced by C_{C1} is intended to counteract the phase lag introduced by this pole. Based on the well-known *I-V* relation of a MOSFET, the DC component of V_{o2} and V_A are respectively given by:

$$V_{o2} = V_{DD} - |V_{Tp}| - \sqrt{\frac{2I_{load}}{\mu_p C_{ox}(W/L)_p}} \quad (14)$$

$$V_A = V_{DD} - V_{SG,i3} = \cdots = V_{DD} - |V_{Tp}| - \sqrt{\frac{I_{tail}}{\mu_{p(W/L)_{i4}}}} \quad (15)$$

μ_p, C_{ox}, $(W/L)_p$, and $(W/L)_{i4}$are the hole mobility, gate capacitance per unit area, and aspect ratio of pass device and M_{i4}, respectively. Therefore, the gate-bulk voltage of C_{c1} (V_{gb}) is expressed as:

$$V_{gb} = V_{o2} - V_A = \sqrt{\frac{I_{tail}}{\mu_p C_{ox}(W/L)_{i4}}} \cdots - \sqrt{\frac{2I_{load}}{\mu_p C_{ox}(W/L)_p}} \quad (16)$$

This equation shows that V_{gb} is proportional to the square root of I_{load}. To force C_{c1} working in depletion for the entire range of the load current, V_A can be properly set. If this is done, the capacitor value can be approximated as $a(V_{gb}+b)^2 + c$ where *a*, *b* and *c* are constant. Hence:

$$C_{c1} = \cdots a\left(\sqrt{\frac{I_{tail}}{\mu_p C_{ox}(W/L)_{i4}}} - \sqrt{\frac{2I_{load}}{\mu_p C_{ox}(W/L)_p}} + b\right)^2 + c \quad (17)$$

When I_{load}increases, to account for the variations of P_2, (17) shows that C_{c1} decreases to push Z_1into higher frequencies. The decrease in C_{C1} however is limited by the difference between minimum and maximum values of C_{C1} in depletion.

It is also important to investigate the effect of power supply on the location of poles and zeros because stability must be independent of V_{DD}. For a particular load current, the source-gate voltage of pass device is constant. Hence, V_{o2} follows the variations of V_{DD}. C_{c2}, as an SCDM, is not indeed affected by this phenomenon because its absolute value is almost independent of the operating point (Fig. 4). This is the reason why an SCDM with minor variations is employed for realizing this capacitor. C_{c1}, on the other hand, is dependent on its operating point. Nevertheless, the terminal voltage of this capacitor is as well independent of V_{DD}because the input stage of error amplifier is biased with constant current, I_{tail}. Therefore, nodes V_A and V_{o2} are both V_{SG} lower than the V_{DD} in which V_{SG} is independent of power supply.

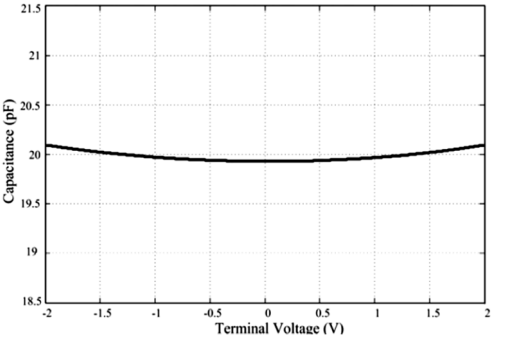

Fig. 4 . The *C-V* charastristic of Fig. 2 (*W/L* = 1180µ/20µ) [9]

Almost all state-of-the-art LDOs require an on-chip capacitor at the output (C_L in Fig. 2) for enhancing ac and transient responses. MIMs are conventionally employed to implement this capacitor. As an alternative approach, C_L can be an uncompensated MOSCAP with higher density. Fig. 6 shows the C-V diagram of the 100pF integrated output capacitor used in the proposed LDO. Output voltage is large enough to maintain the operating point in accumulation or perhaps inversion. Furthermore, the output is always under regulation to have minor variations in magnitude. This guarantees the fact that C_L is mostly remained in voltage-independent regions under different transient conditions. Employing such a capacitor at the output is very important to significantly reduce silicon area and overall cost. No change in circuit performance of the circuit is observed when 100pF MIM capacitor of initial design is replaced with its equivalent uncompensated MOSCAP. However, the area efficiency is considerable (100000 µm2 vs. 18000 µm2 in our technology).

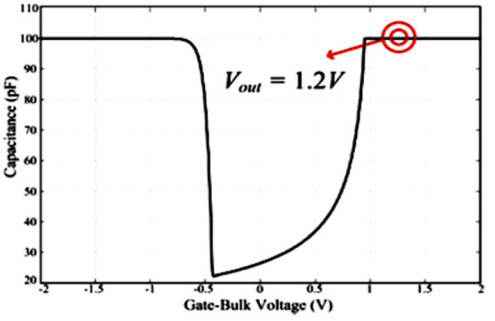

Fig. 5. C-V diagram of the load capacitance (W/L = 590µ /20µ) [9]

Table I summarizes the performance of the circuit for $C_L = 100pF$.

Table 1. Performance summary with *CL* = 100PF

Technology		0.18µm Digital Cmos Technology
Output voltage		1.2v
Dropout voltage		0.2v
Maximum I_{Load}		100mA
Quiescent current		83 µA
Dc Load Regulation (V_{DD}=1.4v,I_{Load}=0.01-100mA)		16µv/mA
Dc Line Regulation (V_{DD}=1.4v-3.4v)	I_{Load}=100µA	0.8mv/v
	I_{Load}=100mA	1mv/v
Transient settling time		850ns$^+$
		1500ns$^-$
PSR for 100mA		-62dB for 0-10KHz

SCRUTINY METHODE TO ACHIVED HIGH POWER SUPPLY REJECTION

To achieve high power supply rejection interesting method has been used in reference [10]. According to Figure 6 a stage with unity gain is used after error amplifier. Such that drain and gate of M_n connected to each other. So impedance from M_n drain's to V_{dd} is much smaller than impedance from M_n drain's to ground. So M_p tracks changes of V_{dd} and source-gate of this transistor remain constant. As a result, noise in main supply don't affected pass transistor current and reduced in V_{out} node.

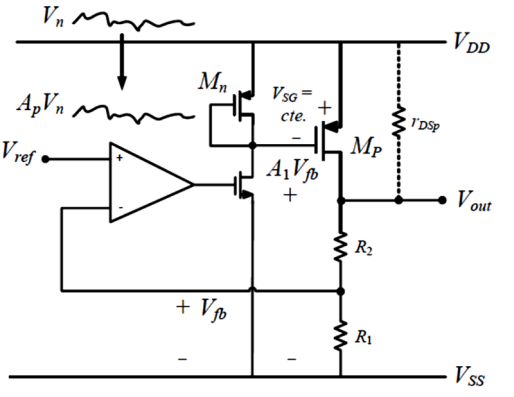

Fig. 6 .Soloution of reference [10] to reduce PSR

PROPOSED LDO REGULATORS

In both proposed methods, regulator in reference [8] has been used as a base regulator.

4.1. LDO regulator with enhancement steady-state specification

This method has been presented to improve steady-state specifications. As it was observed in first part, according to relations (2) and (3), the DC gain of regulation loop should be increased to achieve that goal. Therefore, cascode technique is applied to second stage of error amplifier of base regulator. Figure 7 shows structure of proposed LDO. The DC gain of proposed LDO regulator is according to equation (6), but R_s has increased from $r_{os1} \parallel r_{os3}$ to $r_{os1} \parallel r_{os3}(1 + g_{ms3}r_{os5})$.

Another parameter that affected by gain is Power Supply Rejection (PSR). Increased gain improved PSR at low frequency. Output is given by:

$$\begin{aligned} V_{out} = {} & \frac{R_{F1}+R_{F2}}{R_{F1}+R_{F2}+r_{dsp}}V_n + g_{mp}r_{dsp}V_n - \cdots \\ & -A_1\beta g_{mp}r_{dsp}V_{out} - A_p g_{mp}r_{dsp}V_n + \cdots \\ & + \frac{2r_{otail}+r_{oi1}}{2r_{otail}+r_{oi1}+\frac{1}{gmi3}}A_{12}g_{mp}r_{dsp}V_n + \cdots \\ & + \frac{\frac{1}{gms3}+\frac{1}{gms5}}{\frac{1}{gms3}+\frac{1}{gms5}+r_{os1}}A_{22}g_{mp}r_{dsp}V_n \end{aligned} \quad (18)$$

where A_{12} is the gain of the second stage in the error amplifier and A_{22} is gain from M_{s3} to M_p gate. We increase the A_1, A_{12} and $A_{22}$by using the cascode technique for the second stage. β is the feedback factor $\frac{R_1}{R_1+R_2}$, r_{dsp}, and g_{mp} are the output impedance and transconductance of the pass transistor, respectively. Assuming $r_{dsp} \ll R_1 + R_2$, we have:

$$V_{out} = (\frac{1-A_p}{A_1\beta} + \frac{1}{g_{mp}r_{dsp}}.\frac{1}{A_1\beta} + \cdots + \frac{2r_{otail}+r_{oi1}}{2r_{otail}+r_{oi1}+\frac{1}{gmi3}}\frac{A_{12}}{A_1\beta} + \cdots + \frac{\frac{1}{gms3}+\frac{1}{gms5}}{\frac{1}{gms3}+\frac{1}{gms5}+r_{os1}}\frac{A_{22}}{A_1\beta})V_n \quad (19)$$

According to (19), the increase of the gain in low frequencies, causes increase of the PSR. As a result, PSR is almost constant. When R_S is increased, poles P_1, P_2 and P_4 become small and bandwidth is reduced. Therefore, transient settling time will be increase.

4.2. A High Power Supply Rejection (PSR), Slew-Rate Enhancement and good line and load regulation Low-Dropout Regulator

Proposed LDO in part A has good line and load regulation, but it has not significent improvement in PSR.

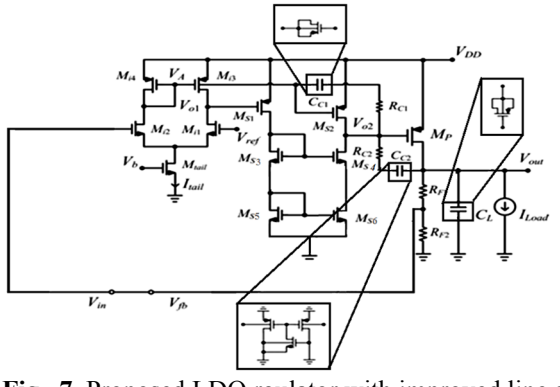

Fig . 7. Proposed LDO rgulator with improved line and load regulation

To achieve LDO with improvement steady–state, transient, and high frequncy specification, LDO regulator shown in figure 8 is proposed.

It is important to investigate the effect of power supply on the location of poles and zeros, because stability must be independent of *VDD*. For a particular load current, the source-gate voltage of pass device is constant. Hence, V_{o2} follows the variations of V_{dd}. C_{c2}, as an SCDM, is not indeed affected by this phenomenon because its absolute is almost independent of operating point. This is the reason why an SCDM with minor variations is employed for realizing this capacitor. Also, the terminal voltage of C_{c1} is depended of V_{dd}, because the input stage of error amplifier is biased with constant current, I_{tail}. Therefore, V_A and V_{SG} nodes is lower than the V_{dd}, and V_{o2} is V_{GSn2}. Then, SCDM is suitable for C_{c1}. Output voltage is large enough to maintain the operating point in accumulation or perhaps inversion. Furthermore, the output is always under regulation to have minor variations in magnitude. This guarantees the fact that C_L is mostly remained in voltage-independent regions under different transient conditions.

In this proposed LDO, the additional voltage subtractor stage, which presented in [10], is used between error amplifier and pass transistor of LDO circuit, which is presented in [9], but NMOS size is three times the size of PMOS. Thus, DC gain of LDO has increased, and as a result line and load regulation has reduced. Figure 9 shows the corresponding small-signal equivalent circuit for proposed LDO. In small signal analysis, with adding subtractor stage, poles P_1, P_2 and P_4 become large and bandwidth is increased, thus, slew-rate is improved. . In this structure, one pole is added in V_1 node, but whereas C_s is large and R_s is small, it does not affect on circuit bandwidth.

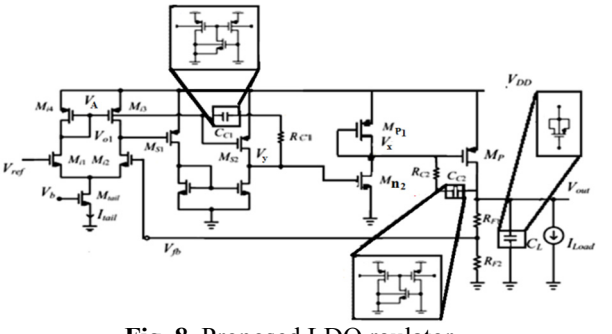

Fig. 8 .Proposed LDO rgulator

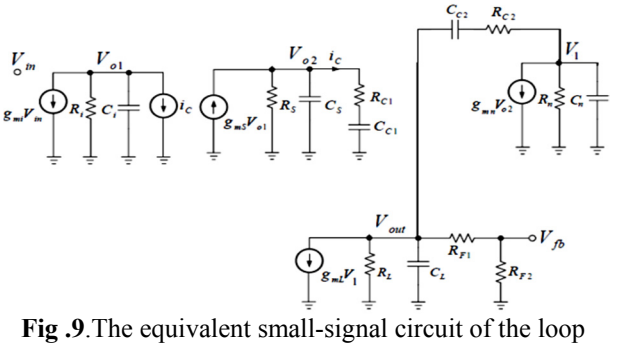

Fig .9.The equivalent small-signal circuit of the loop

SIMULATIOIN RESULTS

Proposed regulators and regulator suggested in [9] have been simulated in TSMC 0.18µm CMOS process. Line regulation, load regulation and PSR for both proposed LDO and LDO in [9] are shown in figures 10 to 12, respectively. Simulation results show the second proposed regulator has good efficiency.

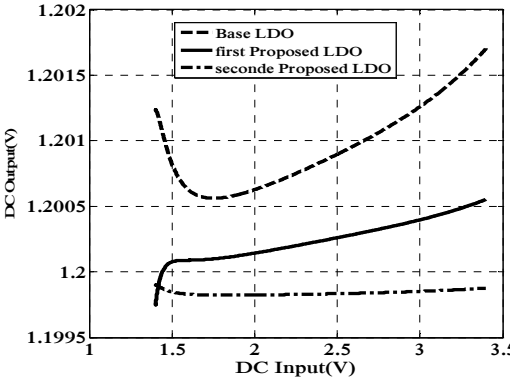

Fig . 10.Line regulaton for proposed regulators and regulator in[9] for $I_{Load} = 100mA$

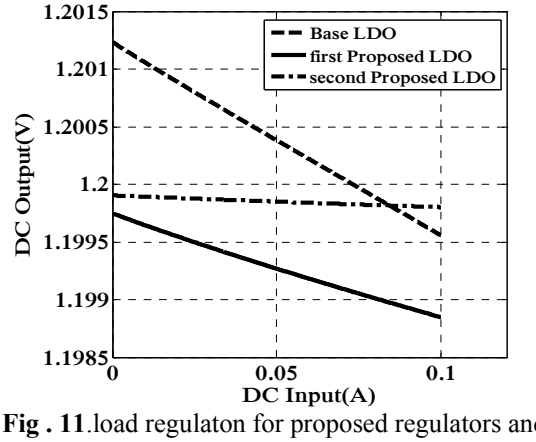

Fig . 11.load regulaton for proposed regulators and regulator in[9]

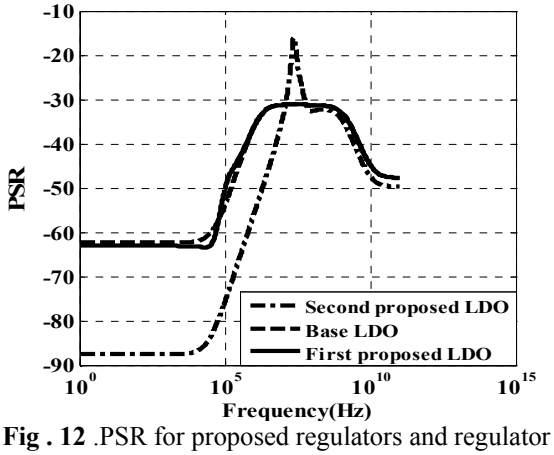

Fig . 12 .PSR for proposed regulators and regulator in[9]

The transient response for proposed LDOs and LDO presented in [9] for a 100 mA current step shows in figures 13 to 15, respectively. Setteling time for first proposed LDO is longer than LDO in [9], but seconde proposed LDO has significent improvement .

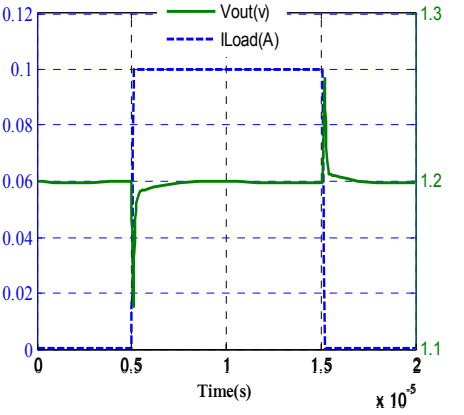

Fig . 13. Load transient response for first proposed LDO, for 0-100mA load current change

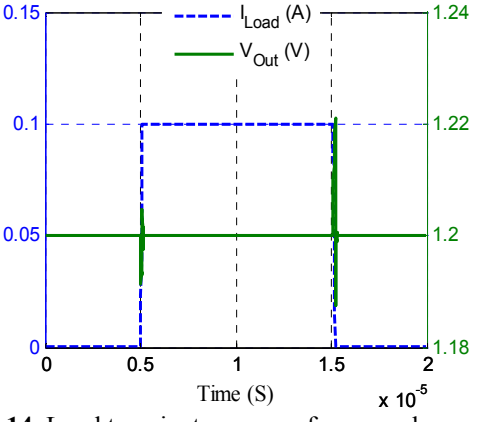

Fig . 14 .Load transient response for second proposed LDO, for 0-100mA load current change

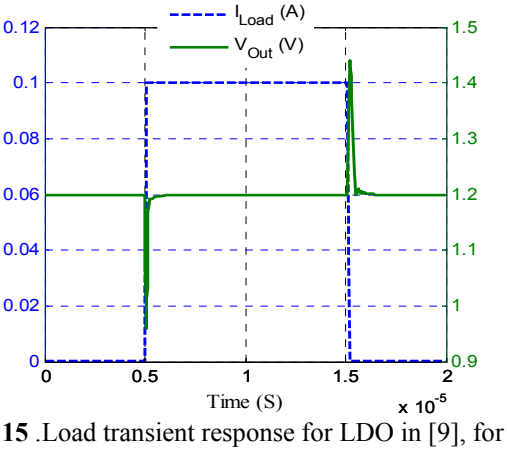

Fig . 15 .Load transient response for LDO in [9], for 0-100mA load current change

Table 2, tabulates all the important parameters of the proposed regulator in comparison with those of [1], [9], and [11].

CONCLUSION

In this paper, two LDO regulators with high performance was proposed. By using MOS transistor for load capacitor and compensation capacitors, both proposed LDO can be integrated, completely. First method increased gain of error amplifier by using cascade technique and improved line and load regulation. Line regulation has been reduced from $1mv/v$ to $0.8\,mv/v$ and from $0.8\,mv/v$ to $0.4\,mv/v$ for $I_{Load} = 100mA$ and $I_{Load} = 100\mu A$, respectively. Furthermore, load regulation has been reduced from $16\,\mu V/mA$ to $9\,\mu V/mA$. Second method by adding a stage between error amplifier and pass transistor has improved steady state specification, transient response, and PSR. Line regulation has been reduced from $1\,mv/v$ to $0.025\,mv/v$ and from $0.8\,mv/v$ to $0.026\,mv/v$ for $I_{Load} = 100mA$ and $I_{Load} = 100\mu A$, respectively. Load regulation has also been reduced from $16\,\mu V/mA$ to $1.05\,\mu V/mA$. Power supply rejection was -78dB at 0-10KHz. Finally, settling time for a 100 mA current step was improved from 850 ns to 350ns and 1500 ns to 600 ns for positive and negative edges.

Table 2. Important parameters of the proposed LDO regulators in comparison with other LDO regulators

	[12]	[9]	[11]	Proposed 1	Proposed 2
Technology	0.35	0.18	0.5	0.18	0.18
Minimum V_{DD} (µm)	2	1.4	1.4	1.4	1.4
Peresent output voltage (V)	1.8	1.2	1.2	1.2	1.2
Dropout voltage (V)	0.2	0.2	0.2	0.2	0.2
Maximum load current (mA)	100	100	50	100	100
Line regulation (mV/V)	0.057	1 for I_{Load}=100mA	2.4	0.5 for I_{Load}=100mA	0.024 for I_{Load}=100mA
		0.8 for I_{Load}=100µA		0.4 for I_{Load}=100µA	0.026 for I_{Load}=100µA
Load regulation (µV/mA)	109	16	160	9	1.05
PSR (dB)	N.A	-62 At (0-10KHz)	-70 At 1KHZ	-63 At (0-10KHz)	-78dB At(0-10KHz)
Quiescent current (µA)	20	83	62	83	98
T_r= Transient settling time (ns)	9000 ns^+	850 ns^+	1330ns^+	2500 ns^+	350 ns^+
	N.A	1500 ns^-	N.A	1800 ns^-	600 ns^-
FOM (ns)*	1.8	0.7	1.7	2	0.34
Year	2010	2008	2011	2012	2012

*$FOM = T_r * I_Q/I_{Load}$

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