A Novel Silicon on Diamond Structure to Improve Drain Induced Barrier Lowering

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ABSTRACT:
Silicon on diamond structure to improve DIBL is presented. The electrical field penetration through the buried insulator of diamond degrades the DIBL. In the new structure, a second, double insulating material, e.g. SiO_2 is added on top of the buried insulator and partially covers the diamond. The second insulating material has lower electrical permittivity. Therefore, the fringing field capacitance is smaller. Simulation results of 22 nm silicon-on-diamond transistor shows 18% improvement in DIBL comparing with conventional SOD structure. Lattice temperature increase of 5% is observed in the new structure compared with the conventional SOD.

KEYWORDS:
Drain Induced Barrier Lowering, Ultra Thin Body, Silicon on Diamond, MOSFET, Hydrodynamic Model

1. INTRODUCTION

Silicon on insulator technology is a solution to scaling problems mostly faced by Bulk technology as it moves deep into the nano-scale regime. Superior short channel effects and reduced parasitic elements are among the functionality improvements obtained using fully depleted SOI technology. FinFETs and planar Ultra-Thin Body SOI are two good examples of such solutions [1, 2]. A thin insulating layer, i.e. SiO_2, is used to separate the active ultra-thin body region from the substrate (Fig. 1). As a result of the thin body, the leakage current which normally flows far from the gate in the silicon body reduces, and consequently, higher speed and lower leakage are obtained.

However, limiting the device body thickness to the channel depth increases the source/drain resistance [3, 4]. In addition, the buried insulator electrical non-idealities can inversely affect the device electrostatics due to the extreme proximity of the body to the insulator [1].

Due to the low thermal conductivity of buried oxide under the silicon film in silicon-on-insulator technology, self-heating effects are observed. The presence of silicon dioxide layer under the top silicon causes self-heating due to about 1000 times lower thermal conductivity of silicon dioxide relative to diamond layer. The self-heating can degrade the device performance such as drive current and mobility reduction and decreased trans-conductance and speed of the transistor. As the chip power density level has increased, new methods to dissipate the generated heats in the channel are required. Silicon on diamond technology in which diamond like carbon (DLC) is used as buried insulator benefits from high thermal conductivity of diamond comparing with silicon dioxide (κ_{SOI}=1.48$Wm^{-1}K^{-1}$, $\kappa_{Diamond}$=1400$Wm^{-1}K^{-1}$). As such, SOD MOSFETs can operate at much higher power levels relative to SOI MOSFETs at the same junction temperature. Therefore, DIBL increases as drain-body fringing field capacitance penetrates into the DLC layer. SOD Power density levels of one order of magnitude higher than SOI has been reported [5].

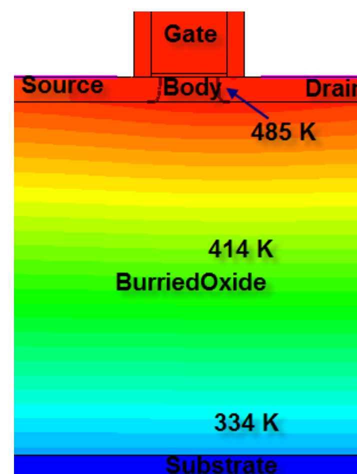

Fig. 1. Self heating effects in Ultra-Thin Body SOI MOSFET

However, integration of ultra-thin body processes on silicon on diamond substrates suffers from increased leakage current. The electrical permittivity of diamond is roughly 2.5 times than that of silicon dioxide. As a result of drain electrical field penetration through the diamond, the device drain induced barrier lowering increases.

In this paper, novel silicon on diamond structure is presented. A second insulating layer of silicon dioxide is inserted between the DLC layer and the device body such that the insulating layer has no impact on the device thermal behavior. The paper is organized as follows: In section 2, the new SOD structure is presented, simulation results of a 22nm UTB SOI MOSFET is shown in section 3, followed a conclusion part in section 4.

2. THE NEW SRUCTURE

In order to reduce the junction temperature in SOI devices, diamond as buried insulator can be used [5,-8]. Using diamond as buried insulator increases the device off-state leakage current. We developed a new structure that cancels the excessive impact of drain on the device body due to the higher electrical permittivity of diamond. Fig. 1 shows the new structure. The top insulator has electrical permittivity greater than the buried insulator. One example is silicon dioxide. The top insulator length is smaller than the total device length. As a result, the generated heat in the active device region can escape to the substrate.

The heat removal can also be implemented by thinning the silicon dioxide as buried insulator. Fig. 2 shows the parasitic capacitances of an ultra-thin body and BOX SOI MOSFET. The substrate-body/source/drain capacitance can be modeled by:

$$C_{BOX} = \frac{\varepsilon_{Box}}{t_{Box}} \qquad (1)$$

where t_{BOX} denotes the BOX thickness and electrical permittivity of the silicon dioxide is shown by ε_{BOX}.

As buried oxide thickness is reduced, the parasitic $C_{Sub\text{-}B}$, $C_{Sub\text{-}S}$, and $C_{Sub\text{-}D}$ increase. Therefore, the device speed is degraded.

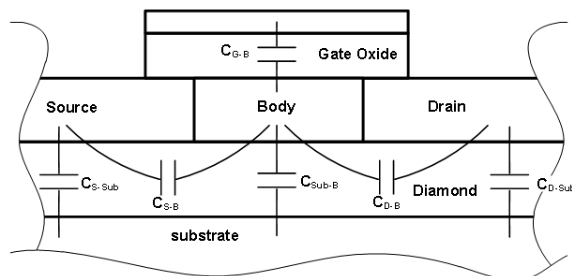

Fig. 2. Parasitic capacitances of an Ultra-Thin Body BOX SOI

However, the drain-body and source-body capacitances are also affected by BOX thinning. The relation that describes the variation of C_{BD} and C_{BS} is:

$$C_{BD(x)} = \frac{C_{BOX}}{\exp(\frac{\pi \times x}{t_{BOX}}) - 1} \qquad (2)$$

where x denotes the body distance to the drain junction. From the Eq. (2), as the BOX thickness reduces, the body to drain/source capacitance diminishes resulting in the better drain induced barrier lowering. Therefore, from Eq. (1) and (2), a trade-off in BOX thickness and an optimum value for BOX thickness are chosen [1].

Diamond can be used as an alternative to silicon dioxide to enhance the heat removal from the silicon top layer. However, As a result of higher diamond electrical permittivity in Eq. (2), the drain induced barrier lowering increases leading to increased short channel effects. Fig. 3 in which the top insulator layer is chosen as silicon dioxide is one solution to the current problem. This structure is different from the structure proposed in [3] to reduce the source/drain resistance. In this paper silicon on diamond device is considered for which the drain induced barrier lowering is enhanced.

The device structure is as follows: silicon film thickness, t_{si}=8 nm; gate oxide thickness, t_{SiO2}=1.8 nm; Top insulator thickness=60 nm; Buried insulator thickness=200 nm; body doping $N_A=10^{19}$ cm^{-3}; The source and substrate are at zero volt. The substrate is considered as thermal contact at 300 k. The non-isothermal drift-diffusion is used to model the carrier transport in the active device regions [9].

3. SIMULATION RESULTS

The structure of the device in Fig. 3 is considered. A thick diamond buried insulator is considered to reduce the effect of $C_{Sub\text{-}D}$ and $C_{Sub\text{-}S}$. The top insulator

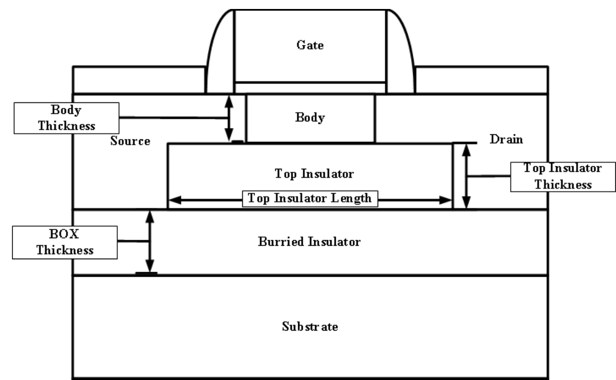

Fig. 3. The new silicon on diamond structure

layer is considered as silicon dioxide for its low electrical permittivity to reduce the impact of drain/source in the device body.

The ratio of Ion/Ioff is shown in Fig. 4. As it can be seen, the double insulating silicon on diamond device (DISOD) starts close to SOD, as top insulator length increases. As device leakage current reduces, the Ion/Ioff increases to the values close to SOI device. For the top insulator length between 50 nm and 90 nm, the ratio of on to off current is even higher than SOI transistor as a result of drain to body capacitance reduction.

Fig. 5 shows the DIBL variations versus the top insulator length. As it can be seen, as top insulator length increases from 20 nm to 100 nm, the DIBL starts from values higher than SOD to the best value close to SOI.

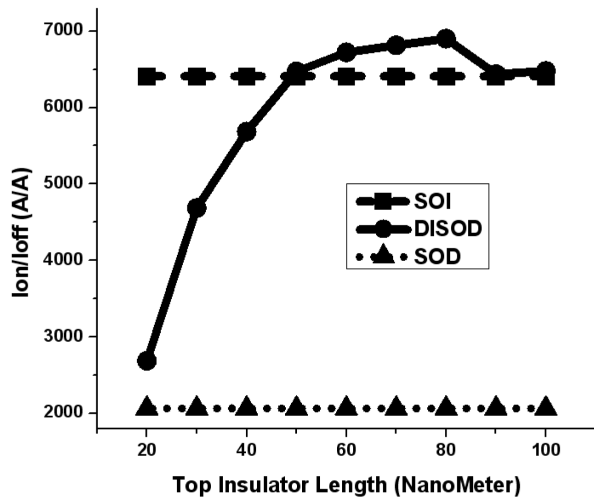

Fig. 4. The ratio of transistor on to off currents, L=22 nm, W= 1 μm

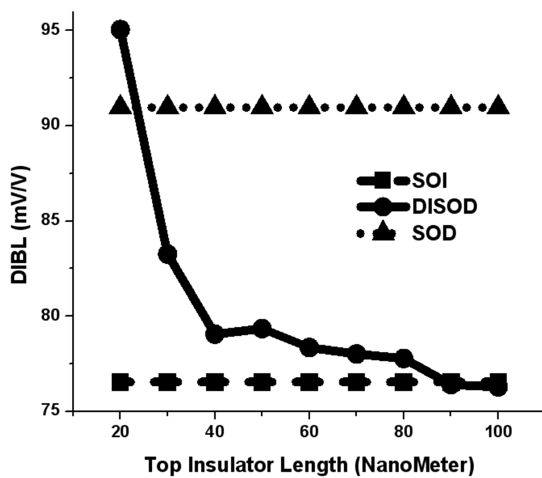

Fig. 5. Drain induced barrier lowering as top insulator length varies

This shows the effectiveness of the new structure in controlling the leakage and DIBL value. This is the direct result from lowering $C_{D\text{-}B}$ in the new structure.

The drain-source resistance is computed based on the method mentioned in [10]. The total drain to source resistance (R_t) is written as the addition of drain/source series resistance ($R_{ds}(V_{gs})$) and the channel resistance (R_{ch}). The total resistance is computed by dividing the drain-source voltage to the current. Then:

$$R_t = R_{ds} + \frac{L}{\mu_0 C_{ox} W}((V_{gs} - V_{th})^{-1} + \theta) \quad (3)$$

where L and W denote the channel length and width, C_{ox} the gate oxide capacitance in cm^{-2}, μ_0 the electron mobility, V_{th} the threshold voltage, and θ the normal electric field induced mobility reduction. The Eq. (3) is divided in two and can be written as:

$$R_t = a(V_{gs} - V_{th})^{-1} + b \quad (4)$$

$$a = \frac{L}{\mu_0 C_{ox} W}, b = a\theta + R_{ds} \quad (5)$$

In this paper, R_t is computed from the drain-source current versus drain-source voltage curves for various $(V_{gs}\text{-}V_t)^{-1}$ values. Then, using the least square methods, *a* and *b* coefficients and finally, R_{ds} are computed.

Shown in Fig. 6, the Rds versus top insulator length is presented and compared with the identical values for SOI and SOD. As it can be seen, Rds increases as the top insulator length increases. As the top insulator length increases from 22 nm, the body thickness expands from just under the gate to the values higher. Therefore, the drain and source regions get thinner. Consequently, the total resistance increases. The maximum value the source-drain resistance gets is the same as SOI.

One should notice that the value of R_{ds} is significantly lower than SOI, if the top insulator length thickness is near the channel length, i.e. 22nm. Although R_{ds} is small in this region, the DIBL curve shows very high values in this range. Therefore, other structures may be required to keep the DIBL low, while the source-drain resistance is significantly reduced.

While the substrate was kept constant at 300k, the top insulator length was allowed to vary from 20 nm to 100 nm and the maximum body temperature is recorded. Fig. 7 shows the novel device maximum temperature. As it can be seen, the device temperature is roughly 5% increased. Insertion of the top insulator in the active device region has a very little impact on the device temperature and the structure of silicon on diamond is still functional. Therefore, by inserting the new top insulting layer in this paper, the drain induced barrier lowering is reduced to the levels close to silicon on insulator technology. In addition, the thermal characteristics of the devise is still un-affected by the

new structure and maximum temperatures close to silicon on diamond is obtained.

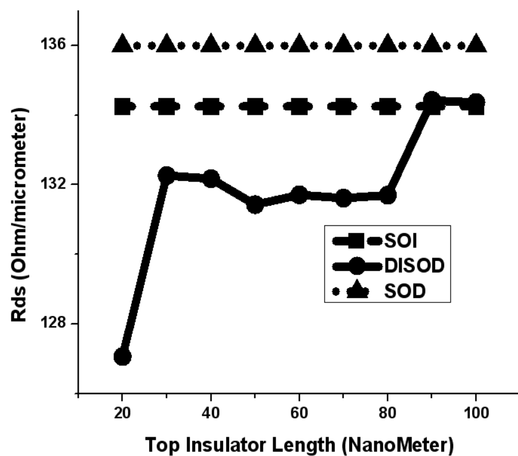

Fig. 6. Total drain-source resistance

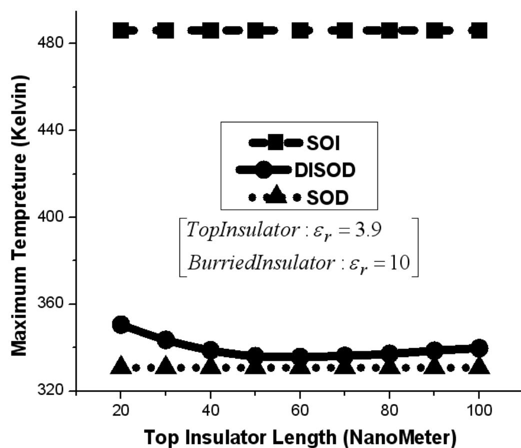

Fig. 7. Maximum body temperature as top insulator length varies, T(Substrate)=300 k

4. CONCLUSION

A second insulting layer is added to the top of diamond in silicon on diamond transistor. The length of top layer is varied from 20 nm to 100 nm. It is shown that the DIBL of SOD is improved incorporated the second insulating layer. The final DIBL is identical to silicon on insulator. The source-drain resistance is almost un-affected by the new structure. In addition, the insertion of the top insulating layer has no/little impact on the device temperature, and maximum body temperature is raised 5 %. While the new structure enhances the DIBL, it keeps the device thermal characteristics almost identical as silicon on diamond substrates.

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