An Investigation in the I-gate Body Contact for Partially Depleted SOI MOSFET

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ABSTRACT:
In this paper for the first time, a circuit model for multi-finger I-gate body-contacted silicon-on-insulator MOSFET is presented. The model parameters are adjusted using simulation of a 45 nm SOI nMOSFET. Using the model, typical body voltage for a 35 finger device is obtained and applied to the transistor. The threshold voltage and drain current are obtained for the first transistor and center ones in the multi-finger structure. The drain induced barrier lowering of the center transistor is increased by 30% and off-current 40 times than that of the first transistor. Simulation results verified the I-gate body contact model in lack of controlling the body voltage comparing with the conventional body contacts e.g. H-gate.

KEYWORDS: Silicon-on-Insulator MOSFET, I-gate Body Contact, Two-Dimensional Device Simulation, Body Resistance, Drain Induced Barrier Lowering.

1. INTRODUCTION

In recent years MOSFET plays an imperative role among various silicon technologies. Incorporating this technology, building numerous digital functions, memory blocks and analog integrated circuits are possible. Therefore, MOSFET is used widely in digital and analog applications. Simplicity of the fabrication process, reliability and scalability has made MOSFET as building block of the todays integrated circuits [1].

MOSFETs are usually made on silicon substrate which is known as bulk technology. As the technology moves into the nano-scale regime, high performance and low power integrated circuits, hence transistors with improved short channel effects are required.

Silicon-on-Insulator MOSFET is a viable technology to substitute the bulk technology [2]. The only structural difference is the buried oxide (BOX) in the silicon substrate [3]. The BOX layer prohibits the most of parasitic effects which are inherent to the bulk technology. In addition, well formation is not required in SOI technology, hence lower wafer area is occupied by the transistors in comparison with bulk. As a result, the die cost reduces. In general, elimination of the latch-up transistor, improved short channel effects, reduction of the source/drain parasitic capacitances, are the three main superior reasons of SOI than bulk. Furthermore, reduction of cross-talk, higher switching speed, isolation of the transistors, lower power in digital circuits, improved trans-conductance and steeper sub-threshold slope are among the benefits [4], [5].

However, SOI technology suffers from self-heating effects (SHEs). As a result of low thermal conductivity of silicon dioxide, the generated heat in the channel of the transistor does not find a way to the substrate and the underlying heat sink. Therefore, the lattice temperature rises in the active silicon film over the buried oxide. This is named self-heating effects and is the main reason for degradation of device performance. As the technology moves into the nano-scale regime, the number of transistors and electric field density increase per unit wafer area. Therefore, self-heating effects pronounces. Consequently, the carrier mobility, device trans-conductance, drain current and device switching speed reduce [6].

Furthermore, partially-depleted silicon-on-insulator MOSFET shows floating body effects (FBEs). Part of the device body over the buried oxide which is not depleted is electrically isolated and forms the floating body. The generated holes in impact ionization process move away from drain positive voltage and accumulate in the floating body. Since there is no way for the holes to escape to a contact, the floating body voltage increases. Therefore, the device threshold voltage reduces and nonlinear behavior is observed in the output characteristic of the device. Activation of the bipolar transistors and elevated drain current are two

effects associated to the FBEs. In addition, kink effect, transient drain current, hysteresis, threshold voltage reduction, and drain breakdown voltage are among the FBEs. There are several methods to eliminate the holes build up in the neutral body region. Making a path for the generated holes to escape to an electrical contact is one solution. Using this method and grounding the contact, the body of the device is ideally grounded. As a result, the floating body effects are eliminated or minimized [7].

In this paper, we analyzed an I-gate body contacted 45 nm PD SOI MOSFET. Two transistors with equal length and width are considered. Using two-dimensional hydrodynamic model simulation, the body voltages and output characteristics are derived. Analysis of output characteristics of the two transistors is an indication of how good the body contact controls the body voltage. The paper is organized as follows: The I-gate body structure is explained in section 2, the simulation model and results are discussed in section 3 followed by a conclusion in section 4.

2. I-GATE BODY-CONTACTED SOI MOSFET

The transistor we considered for analysis is an n-channel I-gate body contacted SOI MOSFET with substrate as standard doping. The body contacted structure was proposed to suppress the floating body effects [7]. The MOSFET structure is shown in Fig. 1.

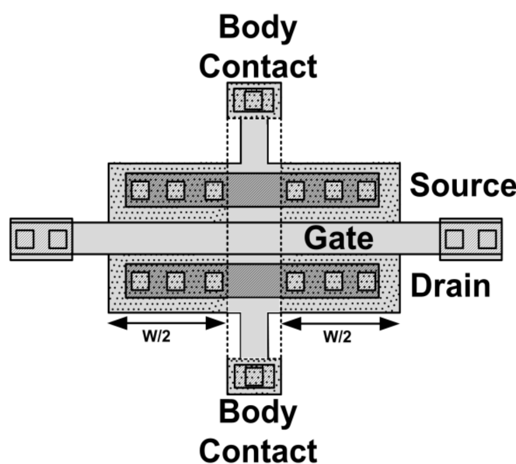

Fig. 1. The n-channel I-gate PD SOI MOSFET with the body contacts

An implant stop block for source and drain is used to extend the p body and place body contacts at the sides of the gate. The p region width is not count in the total effective device width. When the body contacts are connected to the ground, the generated holes can escape to the body contacts through the p region in the middle of the device. In the H-gate structure, the p+ extensions are along the device width and the gate is used to separate the p+ implantation from the source/drain regions. For this reason, the extra gate to p- body capacitance is formed. The parasitic extra gate capacitance is partly eliminated in the I-gate structure and only portion of the gate in the middle of the device forms the parasitic capacitance. It is shown that the parasitic gate capacitance in the I-gate structure is several times smaller than the H-gate. Therefore, I-gate body contacted device shows improved high frequency behavior [8].

However, the P- body extension in the multi finger I-gate structure adds to the body resistance. Fig. 2 shows the I-gate multi-finger layout structure.

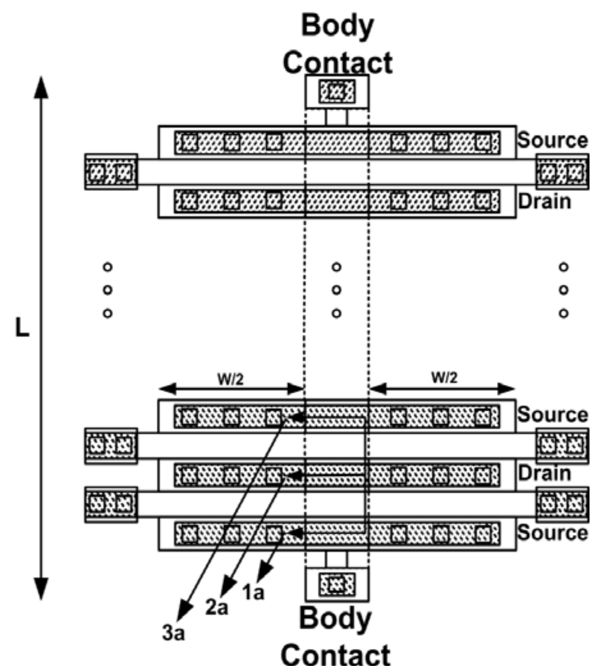

Fig. 2. Multi-finger layout structure of an I-gate body contacted device

In this structure, the impact ionization currents which pass through the body and the body extension face body resistance. The extension resistance is higher in the layout center than the devices at the sides. In addition, part of the body strip under the gate has higher resistance due to the partial depletion of the p-strip from mobile carriers. The higher resistance under the gate contributes to the total body resistance and it is the most in the center of the layout structure. As a result, the body voltage is higher for the gated devices in the center than the devices in the layout sides. Therefore, the terminal characteristics of the devices in center and at the sides are different.

Hydrodynamic model is used to describe the semiconductor physics. In this model, the carrier temperatures T_e and T_h are not equal to the lattice

temperature T_L [9]. The physical models include mobility dependence on doping, lattice temperature and band-gap narrowing. Shockley-Reed-Hall recombination, Auger recombination, saturation velocity dependence on lattice temperature and impact ionization coefficients. The substrate is an electrical contact at 0 V and thermal contact at 300 k. The transistor parameters are: channel length 45 nm, gate oxide thickness 1.2 nm, silicon film thickness 75 nm, and gate pitch 270 nm.

3. DEVICE SIMULATION RESULTS

The higher resistance under the gate contributes to the total body resistance and the body voltage in the center is the highest. The effect of p- body strip on the device characteristics is further investigated using hydrodynamic device simulation. For this reason, the 1a-2a and 1a-3a cut lines in Fig. 2 are considered. The views for the cut lines are shown in Fig. 3. By simulation of the devices as shown in the cut lines, the body strip resistance under the gate is computed. Since there is no current in the channel of the devices, there is a negligible temperature rise in the body. As a result the impact of self-heating effects is considered.

In a multi-finger device, as the number of gates increases, gate and source/drain regions area added to the layout structure as it is seen in Fig. 3B. By computing and subtracting the body-contact resistance seen in Fig. 3A (R2) and Fig. 3B (R1), the resistance associated to a single gate and source-drain is computed. In order to compute the resistance, one terminal voltage was set to ground and the second one to 0.01 V:

$$R = R_1 - R_2 = 1430 - 380 = 1050\Omega \quad (1)$$

The simulated value for the resistance is 1050 Ω. using the value of R, the circuit model for the body in a multi-finger device structure is developed. The circuit model is shown in Fig. 4. R is the body strip resistance obtained from Eq. 1 and V_{Bn} is the body voltage under the nth gate number. In Fig. 4, I_B is the impact ionization body current of a single gate transistor. In addition, m is the total number of fingers.

In order to compute I_B, 45 nm PD SOI MOSFET at terminal voltages V_{DS}=V_{GS}=1.5 V is simulated and the body current is recorded. The resultant current is obtained as I_B=6×10-7 A. Using the body strip model in Fig. 4, the body voltage at each node n is obtained:

$$\begin{aligned} V_B(n+1) &= RI_B((m-(2n-1))/2) + V_B(n) \\ V_B(0) &= 0 \end{aligned} \quad (2)$$

Where n is the node number and m denotes the total number of fingers. Using Eq. (2), the body voltage variations along the length of the multi-finger layout device structure is obtained. Fig. 5 shows the body voltage variation along the layout structure when m varies from 5 to 40.

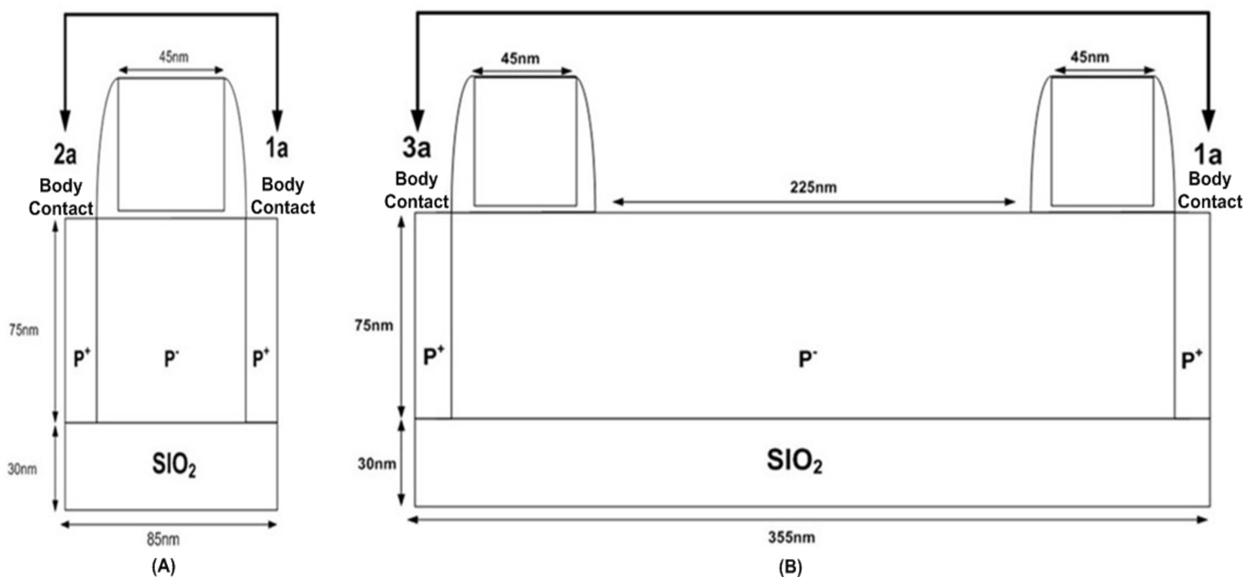

Fig. 3. A) View of the cut plane along 1a-2a, B) View of the cut plane along 1a-3a

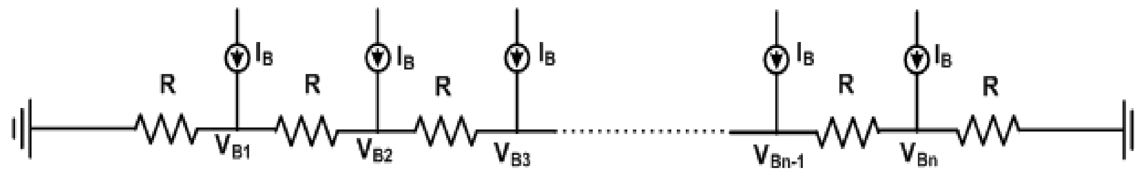

Fig. 4. The p- body strip resistance model in I-gate structure

It's clear that as the number of fingers increases, the layout length and the body voltage in the center of the layout structure increases. Using Fig. 5, maximum body voltages in each layout structure for various numbers of gates are extracted. The number of fingers as 40 is common in RF and analog circuit design where large transistors are required to amplify low power signals [9].

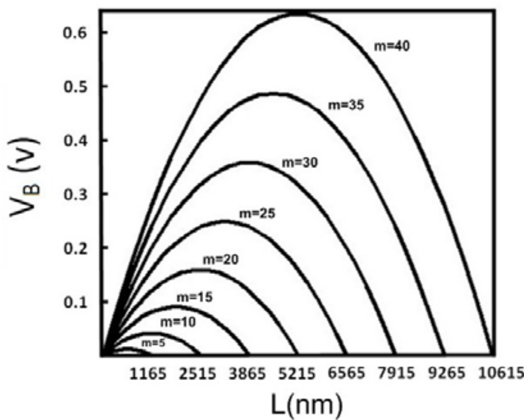

Fig. 5. The body strip voltage variation along the length of the multi-finger layout structure as number of fingers increases

The maximum body voltage as the number of fingers increases is shown in Fig. 6. At a typical m=35, the V_B(max) is obtained as 0.482 V.

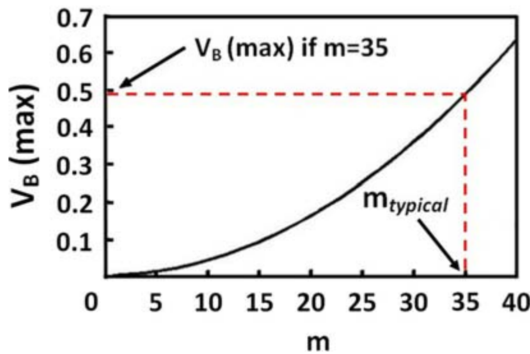

Fig. 6. Maximum Body voltage as the layout number of fingers increases

This is the body voltage at center of the layout structure for the number of fingers 35. Although the body voltage is almost 0 for the gates at the sides of the layout, the body of the transistor at the layout center is at elevated voltage.

Therefore, the transistor output characteristics are different than the one at the sides.

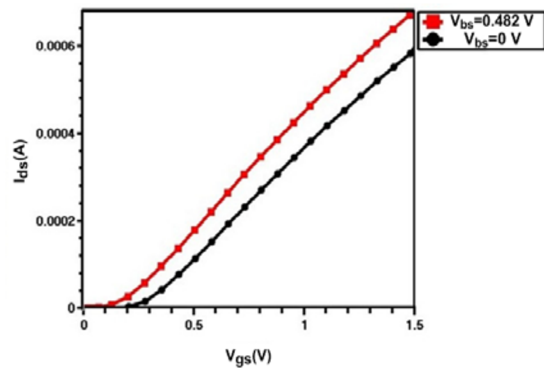

Fig. 7. Drain-source current vs. gate-source voltage

In order to fully analyze the device behavior, the input and output device characteristics are simulated. As it can be seen from Fig. 7 and Fig. 8, the transistor with the body voltage at 0.482 V has lower threshold voltage. Hence, current drive increases. Input and output terminal characteristic analysis raises our concern about the full comparison that needs to be made between the middle and side transistors in the layout structure.

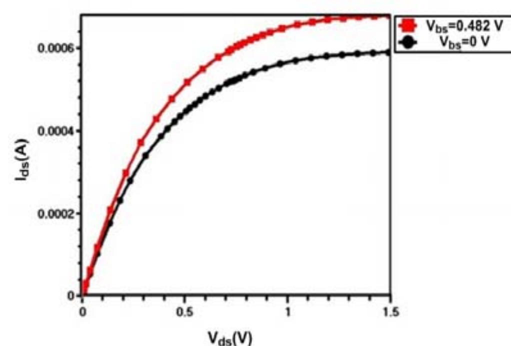

Fig. 8. Drain-source current vs. drain-source voltage

Table 1. The side and center transistors characteristics

	Side Transistor	Center Transistor
DIBL (mV/V)	20	30
Sub-threshold Slope (mV/decade)	85	135
I_{on} (mA)	0.59	0.68
I_{off} (mA)	10^{-8}	4×10^{-7}

Table 1 summarizes the device analysis results obtained. As it can be seen, the drain induced barrier lowering has increased by 30% comparing the side transistor with the center one. In addition, the off-current is increased by 40 times in the center transistor. The sub-threshold slope is increased by 58%, as well. The degradation in DIBL, I_{off} and sub-threshold slope of the center transistors is an indication of degradation of the transistor off-characteristic.
As a result, although the kink effect and gds variations using I-gate body contact is eliminated, the off-current increases. Therefore, comprehensive investigation on I-gate body contact structure and its performance requires analysis of the transistor off-characteristics.

4. CONCLUSION

A circuit model for the p- body strip in I-gate structure of PD SOI MOSFET is proposed. Using the circuit model, body voltage along the body strip for any number of fingers and any gate number is computed. For a typical finger number of 35, the corresponding maximum body voltage is computed. Applying the maximum body voltage, two typical transistors of side and center gates in the layout are compared. The simulation results verified substantial degradation of sub-threshold slope, off-current and drain induced barrier lowering. Although the kink effect and gds variations usually seen in floating body device is eliminated using I-gate body contact, the off-current increases. Therefore, comprehensive investigation on I-gate body contact structure and its performance requires analysis of the transistor off-characteristics.

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