Design of a Wide Tuning-Range, High Swing Fully Differential CMOS VCO with a Differential Tunable Active Inductor

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ABSTRACT:
In this paper, an inductor-less, high frequency tuning range and low power CMOS voltage controlled oscillator (VCO) is presented. The VCO can be implemented in 0.18 µm CMOS, with 1.8 V supply voltage. By using a novel structure, a high frequency tuning range, low phase noise and low power consumption VCO, is obtained. In order to increase the frequency tuning range, an active inductor is used. In addition, deep triode region transistors are employed to enhance the swing of the output voltage. By using the results of simulation with HSPISE software, the tuning range, phase noise and power consumption are 5.49-9.6 GHz, -146 dBc/Hz and 5.99 mW, respectively.

KEYWORDS: CMOS ring oscillator, voltage controlled oscillator, tuning range, active inductor.

1. INTRODUCTION

Adjustable oscillators, which their output frequency is controlled by a voltage, are needed in many applications such as active Radio Frequency Identification (RFID) transponders, OC-48 application, frequency synthesizer module and PLL [1]. In addition, the oscillator with high frequency tuning range is desirable in modern communication systems. Generally, the CMOS oscillators are implemented at two types of ring oscillator and LC oscillator. In fact, the LC oscillators have low phase noise, better frequency stability and low power consumption compared to the ring oscillators. However, the LC oscillators will occupy a lot of places in circuit. In addition, frequency tuning range of LC oscillators is limited [2]. In high symbol rate of Gbps serial links, the slope of the rising and falling edges of the clock should be maximized to achieve the minimum timing jitter. The timing jitter of VCOs is obtained by Eq. 1 [3]-[4].

$$\overline{\Delta\tau^2} = \frac{\overline{v_n}^2}{(\frac{dV}{dt})^2}$$

(1)

Where the timing jitter, the threshold-crossings noise injected, and the threshold-crossings slew rate of the signal, are $\Delta\tau^2$, v_n^2 and $\frac{dV}{dt}$ respectively. As shown in Equation 1, the enhancement in the threshold-crossings slew-rate will decrease the timing jitter. The delay is developed by *RC* time constant at the fundamental nodes. This limitation is a conventional drawback of VCO structures [5]. In order to considerably improve the slew rate of the output voltage, the spiral inductors are employed at fundamental nodes. However, several limitations exist in utilizing spiral inductors as a load, including a large component size, large area and a small inductance. The active inductor in replace of spiral inductor is used to remove these limitations. Therefore by using a differential active inductor, a very wide frequency tuning range is obtained [6]. The ring oscillators with differential delay stage show the greater immunity to the common mode noise. Also, low phase noise and low power dissipation must be considered to the integration of oscillators [7]. In this paper, the design and calculations of a new active inductor VCO are provided. In section (2), the circuit design is described. In section (3), simulation results and discussions are presented. Conclusions are expressed in section (4).

2. DESIGN OF PROPOSED RING VOLTAGE OSCILLATOR

A ring oscillator is formed by a number of gain stages in a loop. Generally, its oscillation frequency changes

by using a controllable voltage. In fact, the output frequency of an ideal VCO has a linear relation with its control voltage. The oscillation frequency of an N-stage ring oscillator is $2NT_d^{-1}$, where T_d refer to the delay of each stage [1]. By considering the resistance load of the differential delay stage at the output node as R_{eq}, the time constant will be equal to $R_{eq}C_L$ at the output node. Where, C_L is the capacitance of the differential delay stage at the output node [2]. Therefore, the oscillation frequency is equal to:

$$F_{osc} = \frac{1}{2NR_{eq}C_L}$$ (2)

The oscillation frequency, power, area and noise performance are the key roles of the ring VCO design [2]. Indeed, superior frequency tuning range, low power, low area and low noise performance are desirable. In this paper, a two-stage ring oscillator VCO is proposed. Its structure is shown in Figure 1. The circuit of each delay stage is illustrated in Figure 2 [8].

Each delay stage circuit (Figure 2) has two poles and one zero. The value of zero, neutralizes the small pole. Therefore the second pole that located at higher frequencies, remains and causes to increase the bandwidth. The active inductor is employed in this circuit to avoid a large chip area. In this circuit, M_1 and M_2, are used as input pair. In addition, an active inductor as is shown in Figure 3, is provided to increase the frequency range [9].
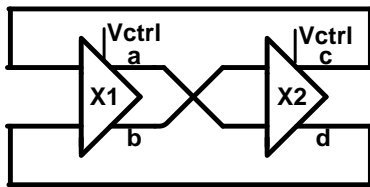

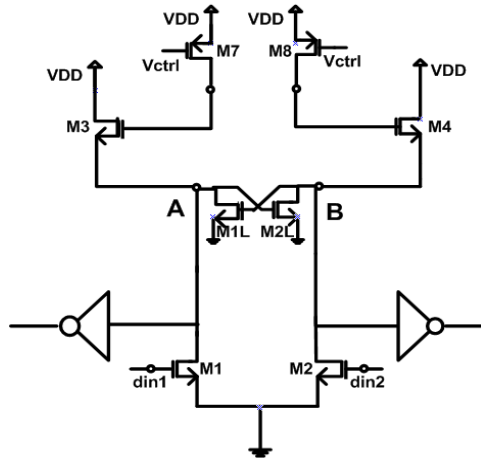**Fig. 1**. Architecture of the two-stage ring oscillator

Fig. 2. delay stage for ring oscillator [8]

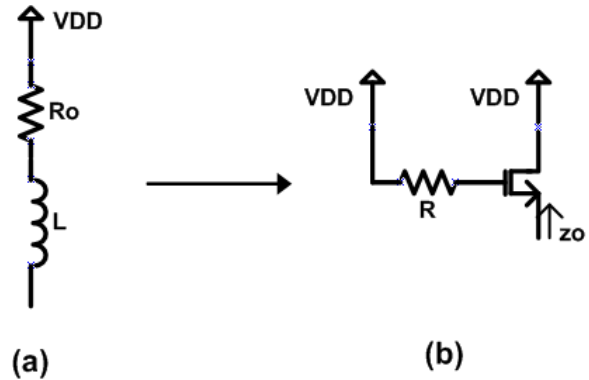The equivalent resistance of the active inductor circuit is obtained as follows [9]-[10];

Fig. 3. Active inductor load [9]-[10]

$$Z_o = \frac{S(C_{gd}+C_{gs})+\frac{1}{R}}{S^2 C_{gd}.C_{gs}+S(\frac{C_{gs}}{R}+C_{gd}.g_m)+\frac{g_m}{R}} \cong \frac{1}{g_m}+S\frac{RC_{gs}}{g_m}$$ (3)

By using the spiral inductor as a load, as it is shown in Figure 3(a), the transfer function of the delay stage is obtained by Equations 4 and 5:

$$A_v(jw) = -g_{m1}[\frac{-1}{g_{m1L}} \| \frac{1}{jwC} \| (R_o + jwL)]$$ (4)

$$A_v = \frac{-g_{m1}(R_o + jwL)}{(1-R_o g_{m1L} - w^2 LC) + jw(R_o C - g_{m1L})}$$ (5)

Where, C is the parasitic capacitance at the output node.

According to Barkhausen's criteria, at oscillation frequency of a ring oscillator, the total phase shift of a delay stage chain most be 180° in feedback system. Therefore, in a two stage ring oscillator, the phase shift of the transfer function will be equaled to 90°. It means that, the oscillation frequency will be obtained as follows:

$$F_{osc} = \frac{1}{2\pi}\sqrt{\frac{R_o(1-R_o g_{m1L})}{L.g_{m1L}}}$$ (6)

Therefore, if L is decreased, F_{osc} will be increased. According to Equation 3, R_o is equaled to $1/g_{m3,4}$. The size of $M_{1L,2L}$ and $M_{3,4}$ is chosen to have the value of $R_o g_{m1L,2L}$ lower than one.

As can be seen in Figure 2, the loads of delay stage are consisted of controllable transistors M_7 and M_8. By using a variable load through varying the gate voltage of M_7 and M_8, the oscillation frequency can be tuned. If M_7 and M_8 transistors are biased in deep triode region, the resistance values of M_7 and M_8, are obtained as follows:

$$R_{M7,8} = \frac{1}{\mu_p C_{ox}(\frac{W}{L})_{7,8}(V_{DD}-V_{ctrl}-|V_{thp}|)}$$ (7)

According to the above equation, by decreasing V_{ctrl}, $R_{M7,8}$ will be decreased. It means that, the inductance will be decreased according to the following relation:

$$L = \frac{R_{M\,7,8}C_{gs\,3,4}}{g_{m3,4}} \qquad (8)$$

Therefore, according to Equation 6, the oscillation frequency will be increased.

By using crossover transistor pair, M_{1L} and M_{2L}, 90° delay will be obtained by each delay cell. It means that, the Barkhausen's criteria will be satisfied by this oscillator. In addition, these transistors are used to charge and discharge of output node capacitor faster. The action of the delay stage can be characterized as follows:

1. If the input node of din1 becomes lower than another input node of din2 , then M_2 will be on, while M_1 will be off. Consequently, M_{2L} will be on and M_{1L} will be off. It means that, the output node (B) capacitor will be discharged through M_{2L} transistor.

2. If the input node of din1 becomes larger than another input node of din2, then M_1 will be on, while M_2 will be off. Consequently, M_{1L} will be on and M_{2L} will be off. Therefore, the capacitance at the output node (B) doesn't discharge through M_{2L} transistor. This capacitor will be charged through M_4 and controllable $M_{7,8}$ transistor (near V_{DD}). In both actions of the full circuit, controllable PMOS transistors of M_7 and M_8, adjust the entire charging and discharging of capacitors at the output node of delay stage.

One of the most important problems of this circuit (Figure 2) is its limited frequency tuning range. Another problem of the circuit is its limited output voltage swing, which is caused by using the active inductor. Triode region transistors M_5, M_6, M_{77} and M_{88} are added to solve the above problems, which are shown in Figure 4.
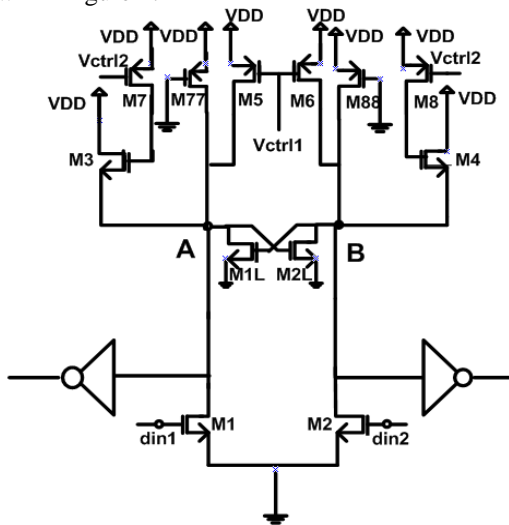

Fig. 4. Frequency range of the proposed ring oscillator

The dc equivalent resistance at the output node is given by Equation 9. It shows that R_{eq} has a small value, which cause to improve the oscillation frequency and frequency tuning range.

$$R_{eq} = (\frac{1}{g_{m3,4}} \| \frac{-1}{g_{m1L,2L}} \| R_L) = \frac{1}{g_{m3,4} - g_{m1L,2L} + \frac{1}{R_L}} \qquad (9)$$

The value of R_L in Equation 9 is obtained as follow;

$$R_L = R_{M\,5,6} \| R_{M\,77,88} \qquad (10)$$

$R_{M5,6}$ are biased in deep triode region. Therefore they have a small output resistance. As mentioned before, if the value of V_{ctrl} becomes low, $R_{M5,6}$ and therefore R_L will be decreased, while the values of $g_{m3,4}$ and $g_{m1L,2L}$ are constant. According to Eq. 9, if R_L is decreased, R_{eq} will be decreased. It means that, the oscillation frequency will be increased. Indeed, according to the Equation 2, conclusion can be obtained as follows:

$$V_{ctrl} \downarrow \;\rightarrow\; R_L \downarrow \;\rightarrow\; R_{eq} \downarrow \;\rightarrow F_{osc} \uparrow \qquad (11)$$

3. SIMULATION RESULTS

The proposed voltage controlled ring oscillator circuit is simulated based on TSMS 0.18μm CMOS process model using HSPICE. The tuning range of Figure 2 and proposed VCO are shown in Figure 5 and Figure 6, respectively, where V_{crtl1} and V_{ctrl2} are connected together and considered as a single V_{ctrl} in the proposed VCO. As can be seen, the frequency tuning range is higher in the proposed VCO. Furthermore, the performance of its linearity is much better. In the proposed VCO circuit, the control voltage value is varied between 0 to 1.3V, which cause in a frequency range of 9.6 GHz to 5.49 GHz (Figure 6). Otherwise, if V_{ctrl1} is changed between 0 to 1.3V and V_{ctrl2} is fixed at 0V, the frequency tuning range will be changed between 9.6 GHz to 8.43 GHz, as is shown in Figure 7. Also, if V_{ctrl2} is changed between 0 to 1.3V and V_{ctrl1} is fixed at 0V, the frequency tuning range will be changed between 9.6 to 7.36 GHz (Figure 8). As can be seen, by integrating the Figures 7 and 8 together, Figure 6 will be obtained, which is a more linear function of V_{ctrl}. The differential waveforms of the VCO at a frequency of 7.64 GHz are illustrated in Figure 9. The output spectrum which is simulated at 7.64 GHz is shown in Figure 10. The simulation result illustrates a maximum peak at 7.64 GHz of oscillation frequency, with the spectrum of complementary skirting spurs. Eye diagram and jitter histogram at 7.64 GHz working frequency are illustrated in Figures 11 and 12. These figures exhibit about 2.58ps and 3.3 ps RMS and peak-to-peak jitters, respectively. By using Equation 12, the phase noise is obtained as follows [3]:

$$S_\phi = \frac{f_0}{f^2} \times (\frac{\Delta t_{vco-rms}}{T_0})^2 \qquad (12)$$

Where, f_0 is center frequency, f is certain frequency offset, $\Delta t_{vco-rms}$ is rms jitter, and T_0 is period of signal. The phase noise of the VCO at the working frequency in different frequency offset is presented in Figure 13. The output phase noise is -146 dBc/Hz at a 1MHz frequency offset. The value of merit of the proposed VCO according to Equatin 13 [11], is -208 dBc/Hz.

$$FOM = L\{\Delta f\} - 20\log\{\frac{f_0}{\Delta f}\} + 10\log\{\frac{P_{diss}}{1mW}\} \quad (13)$$

Where, $L\{\Delta f\}$, Δf, f_0 and P_{diss} are phase noise, certain frequency offset, center frequency and power dissipation, respectively. A comparison between proposed work with previous ring oscillators is performed in Table 1. The proposed oscillator obtained a FOM of -208 dBc/Hz. In the proposed ring oscillator the frequency tuning range is increased and the value of phase noise is almost improved while the power consumption of the ring oscillator is minimum.
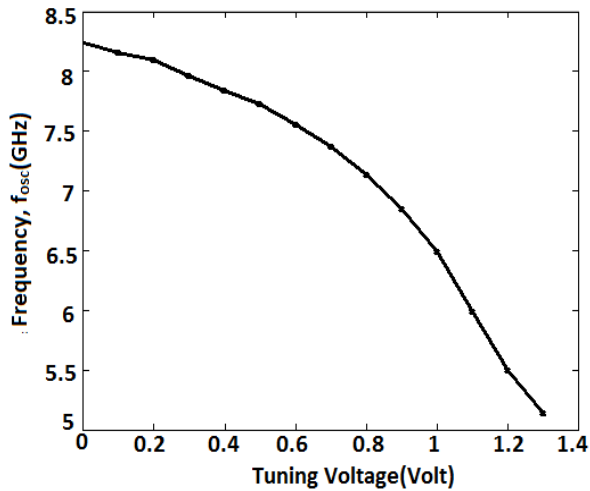

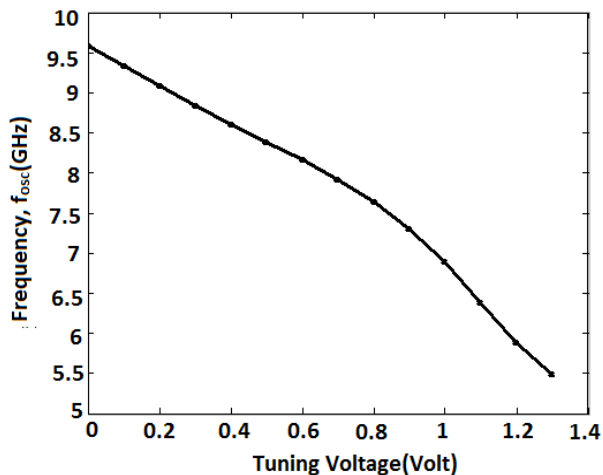**Fig. 5**. Frequency range of the Fig. 2

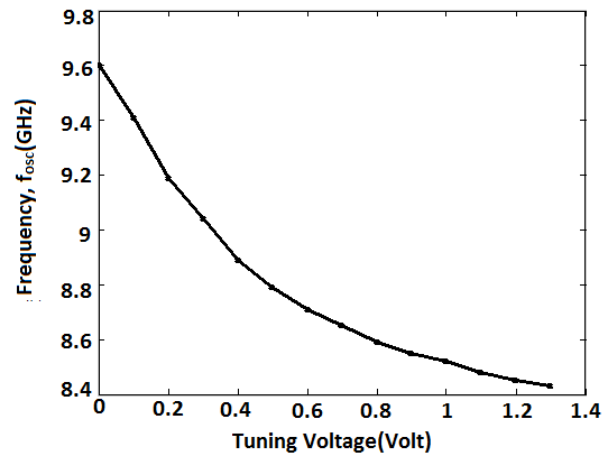**Fig. 6**. Frequency range of the proposed ring oscillator

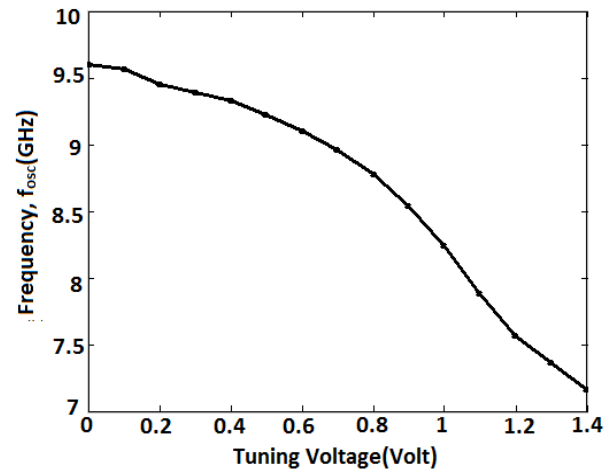**Fig. 7**. Frequency range of the proposed ring oscillator for Vctrl1 variations and constant Vctrl2

Fig. 8. Frequency range of the proposed ring oscillator for Vctrl2 variations and constant Vctrl1
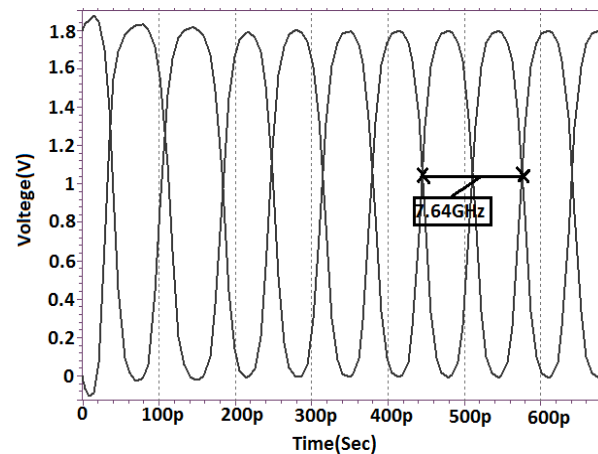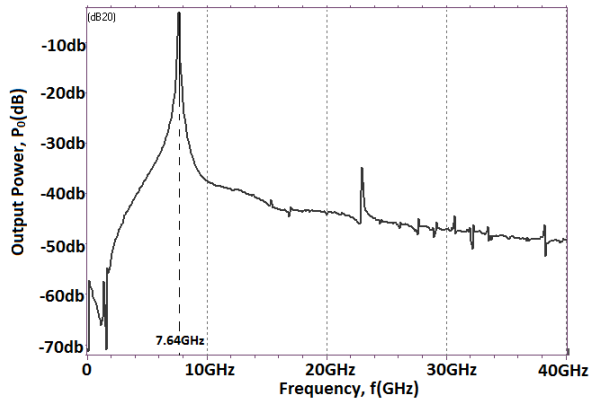

Fig. 9. Transient response of VCO at 7.64 GHz

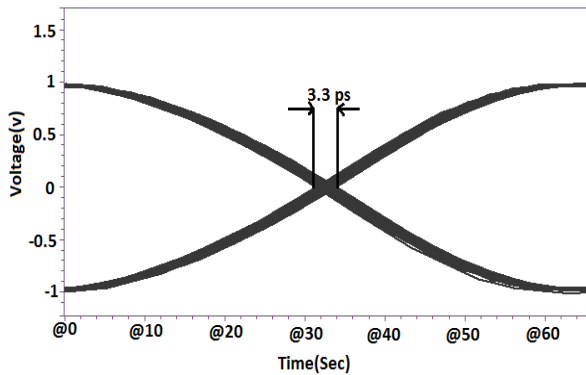**Fig. 10**. Output spectrum of the VCO at center frequency

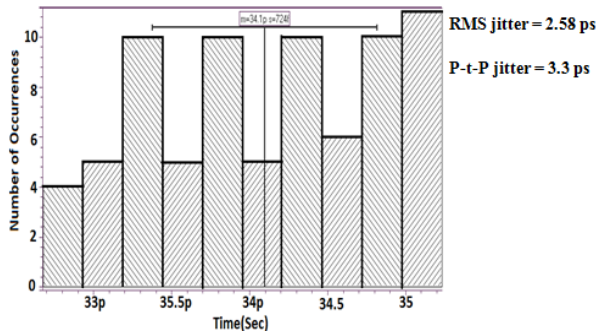**Fig. 11**. Output jitter eye diagram at 7.64 GHz

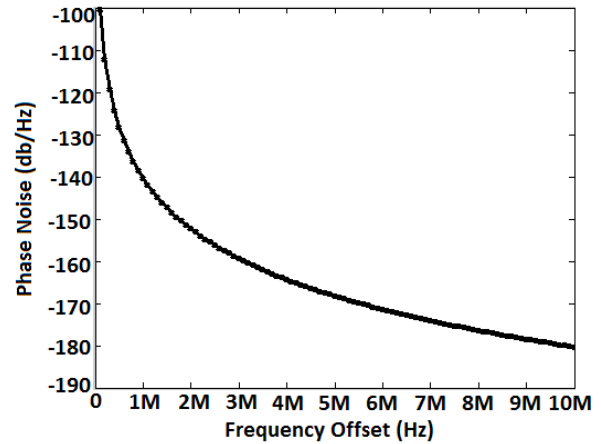**Fig. 12**. Output jitter histogram at 7.64 GHz

Fig. 13. Simulated phase noise at 7.64 GHz for different frequency offsets

4. CONCLUSIONS

In this paper, a two-stage differential ring oscillator is presented. By using an active inductor in each delay stage, a wide tuning range is obtained. In addition, the deep triode region transistors are used to increase the swing of the output voltage. The results show that maximum tuning range, phase noise and power consumption are 5.49-9.6 GHz, -146 dBc/Hz and 5.99 mW, respectively. This circuit illustrates a high FOM performance compared to the previous works. Thus this VCO can be expressed as one of the high tuning range VCO, which is suitable for PLL applications.

Table 1. The performance comparisons of ring oscillators

Ring Oscillator	CenterFreq (GHz)	Tuning Range (GHz)	Phase Noise (dbc/Hz)	SupplyVoltage (V)	FOM (dbc/Hz)	Power (mW)	Technology (μm)	No. of stages
Proposed	7.64	5.49-9.6	-146@1MHz	1.8	-208	5.99	0.18	2
[2]	0.9225	0.92-0.925	-116@10MHz	3.3	-138.97	42.9	0.35	3
[7]	2.4	1.6-2.6	-141@1MHz	1.8	-208	1.09	0.18	3
[12]	2.45	2.36-2.85	-112@10MHz	1.8	-151.34	6.99	0.18	3
[15]	_	1.72-1.92	-123.4@10MHz	1.8	_	13	0.18	4
[16]	0.886	0.381-1.15	-126@10MHz	3.3	-156	7.48	0.35	3
[17]	_	1.57-3.57	-90.31@0.6MHz	1.8	_	16.8	0.09	2
[18]	1.35	0.62-1.5	-126@1MHz	1.8	-172.5	41	0.18	4

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