

GBW Enhancement of a Two Stage Amplifier Using Dual Approach of Feed-Forward and Passive Compensation

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ABSTRACT

Design of a very compact two stage amplifier is proposed by merging passive frequency compensation with a feed forward compensation technique, which achieves significant improvement in gain-bandwidth product (GBW), slew rate and phase margin with lower supply voltage requirement. The mathematical analysis given in this paper justify that the proposed technique offers the advantage of locating poles and zeros at higher frequencies than with the conventional method. The workability of the proposed amplifier has been verified by using Mentor Graphics Eldo simulation tool with TSMC CMOS 0.18 μm process parameters. The simulated results show a GBW of 150 MHz and average slew rate of 98 V/ μs with a power consumption of 3.2 mW.

KEYWORDS: Analog Signal Processing, CMOS, Multistage Amplifier, Passive Compensation, Feed-forward Network.

1. INTRODUCTION

An amplifier is widely used as a basic building block in analog signal processing circuits. The four basic types of amplifiers are voltage amplifiers, current amplifiers, trans-conductance amplifiers and trans-resistance amplifiers. In a multistage or cascaded amplifier, a number of amplifier stages are connected in succession. A Multistage amplifier is required to achieve higher gain, however each stage introduces a pole in the transfer function which causes several design challenges to offset performance, slew rate, gain bandwidth product, phase margin and power consumption tradeoffs. A frequency compensation technique can help to attain better gain frequency response curve under low power constraints. Many compensation techniques proposed are variants of Miller [1] and nested Miller [2] methods. It is a common practice to employ a relatively low value compensation capacitor between input and output of final stage in Miller's method which causes pole splitting and leads to stability at the cost of bandwidth reduction as the performance is deteriorated by right half plane (RHP) zero which needs to be eliminated. Some methods have been advised by the designers to counteract the presence of RHP zero for both two and three stage CMOS amplifiers [3]. One different approach to break the forward path and optimize the performance of the system was exploited using a

voltage buffer [4], current buffer [5] and current amplifier [6-7].

The proposed bandwidth extension technique in this paper is the improved version of passive frequency compensation method [3] where a compensation network was placed across the first stage. The circuit presented here places that compensation network between first and last stage, which counteracts RHP zero while consuming low power and a low supply voltage (V_{DD}) of 1.5volts. The compensation capacitor and load capacitor used in new circuit are of very small value. The circuit is designed and simulated using 0.18 μm technology parameters. The paper is organized as follows. The proposed amplifier using feed-forward and passive compensation technique has been suggested and compared with a prevalent technique [3] in section 2. This section also presents transistor level circuit implementation and block diagram of the proposed and conventional designs. The transfer function is evaluated and location of poles and zero have been determined. Section 3 contains results of various simulation processes for both compensation and without compensation conditions. It is very clear from the output result that compensation helps to improve phase margin and extend bandwidth. Table 1 and Table 2 are included to list of the all circuit parameters and performance summary of corner analysis, respectively. Section 4 defines two well-

known figure of merits (FOMs), which are used to compare performance of various designs. Table 3 is also given here to compare performance of proposed work and circuit with existing techniques. Section 5 concludes the proposed methodology and future work.

2. CIRCUIT TOPOLOGY

The transfer function and stability issue of a prevalent technique [3] is compared with a proposed technique. Different parameters such as location of poles and zeros, bandwidth and low power requirement are also discussed.

2.1. Existing compensation technique

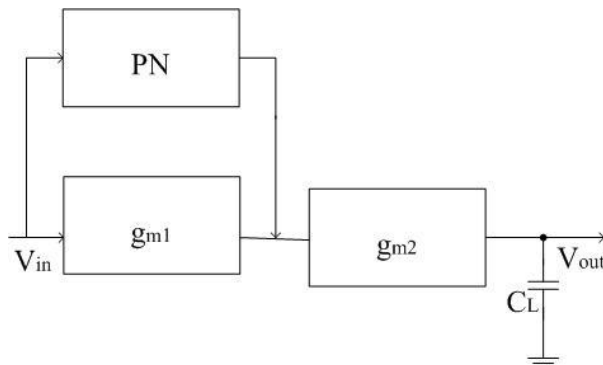


Fig. 1. The Block diagram of conventional amplifier [3]

Passive frequency compensation for high gain-bandwidth and high slew rate is one of the recently-proposed effective solutions [3] for bandwidth extension of amplifier circuits. The block diagram of two stage amplifier is conventional design, shown in Fig.1. It uses only one frequency compensation network [3], which is employed across first stage. The second stage is a common source amplifier to provide large voltage gain. The conventional compensation technique of amplifier circuit is designed and simulated in 0.18µm process.

The transfer function of the two stage amplifier [3] is given as:

$$\frac{V_{out}}{V_{in}} = \frac{A_{dc}(1+sR_cC_c)}{(1+sR_LC_L)(1+sC_c(\alpha+R_c))} \quad (1)$$

Where $A_{dc} = g_{m1}g_{m2}R_1R_L$ and R_c is compensation resistor, R_1 is output resistance of the first stage, R_L is load resistor, C_c is compensation capacitor, C_L is load capacitance and g_{mi} is transconductance of i^{th} MOSFET (where $i=1,2,3,\dots$).

From the transfer function given in equation (1), the locations of poles are as follows

$$p_1 \approx \frac{1}{(C_c(\alpha+R_c))} \quad (2)$$

where

$$\alpha = \frac{1+2R_1g_{m3}}{g_{m3}} \quad (3)$$

and

$$p_2 \approx \frac{1}{R_LC_L} \quad (4)$$

The LHP zero is calculated as

$$z_1 \approx \frac{1}{R_cC_c} \quad (5)$$

As described in passive compensation technique [3], the first non-dominant pole will be cancelled by zero if an inequality $R_LC_L=R_cC_c$ holds true. Also to see the effect of RHP zero, $C_c > C_E$ inequality should be met, these two inequalities should be true according to the conventional method and thus the required compensation capacitor value is quite high.

2.2. Proposed compensation technique

There is requirement of a suitable technique which can place these poles farther from origin and where a smaller value of compensation capacitor can be used. The topology of proposed dual compensation using feed-forward and passive R-C network is shown in Fig. 2(a). It shows changes in the conventional circuit [3]. The transistor level implementation is illustrated in Fig. 2(b).

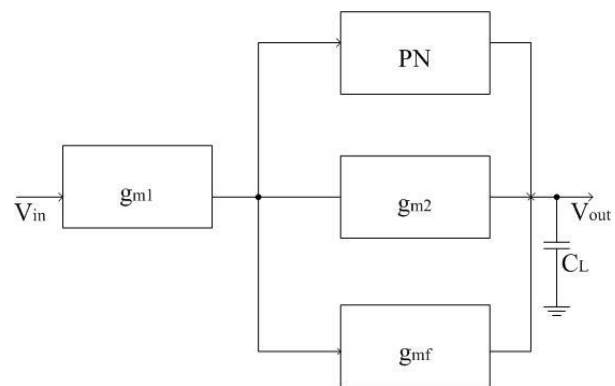


Fig. 2(a). The Block diagram of proposed amplifier

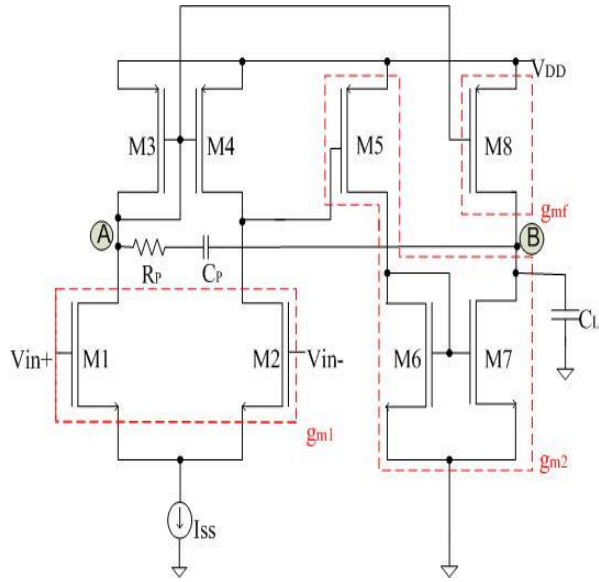


Fig. 2(b). Transistor level implementation

The first stage of this amplifier circuit consists of NMOS transistors M1 and M2 in differential manner, together with PMOS transistors M3 and M4 as an active load forming current mirror. The second stage provides output and is composed of NMOS transistors M6 and M7 as the current amplifier and PMOS M5 transistor to amplify incoming signal. In Fig. 2(b), I_{SS} is the bias current, C_L is the load capacitance and V_{DD} is the supply voltage. In this amplifier a feed-forward path is also added using PMOS transistor M8 to form a push pull output stage, which can improve slewing performance. Hence when a dual compensation method of feed-forward plus R-C network is added to the two stage amplifier design, it can lead to high phase margin and lower capacitance requirement. The frequency compensation is realized using series combination of R_p and C_p . The presence of resistor R_p in series with C_p increases impedance of capacitive path and thereby RHP zero can be eliminated and gain-bandwidth of the circuit is increased. An additional parallel path is provided between input and output path to compensate for the direct feed through effect.

Fig. 3 shows the basic structure of proposed two stage amplifier using small signal model. In this circuit, the input stage has an output resistance r_{o1} , trans-conductance g_{m1} and a total parasitic capacitance as C_1 . The R_p - C_p network is connected between two stages to implement frequency compensation. The output resistance r_{o2} , trans-conductance g_{m2} and a load capacitance C_L are related to second stage. The trans-conductance of feed-forward stage is represented by g_{mf} .

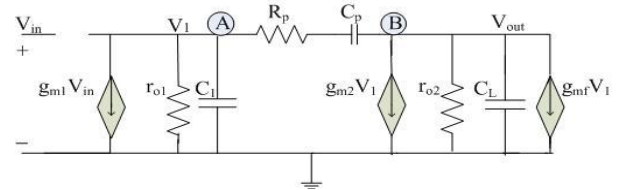


Fig. 3. Small signal equivalent of the proposed circuit

2.1.1 Transfer function

To analyze the stability of proposed circuit, the small signal transfer function needs to be derived. The dominant pole approach was used to calculate the transfer function. Here g_{mi} , r_{oi} and C_{oi} are trans-conductance, output resistance and parasitic capacitance respectively. The following assumptions are used to simplify the transfer function.

- The gain of each stage is higher than unity ($g_{mi}r_{oi} \gg 1$)
- The parasitic capacitor is negligible ($C_L, C_p \gg C_i$)
- Channel output resistance is very high ($R_L, R_p \ll r_{oi}$)

Application of KCL at nodes A and B gives:

$$g_{m1}v_{in} + v_1 \left(\frac{1}{r_{o1}} + sC_1 \right) + (v_1 - v_{out}) \left(\frac{1}{R_p} + sC_p \right) = 0 \quad (6)$$

$$g_{m2}v_1 + \frac{v_{out}(1+sC_Lr_{o2})}{r_{o2}} - g_{mf}v_1 + (v_{out} - v_1) \left(\frac{1}{R_p} + sC_p \right) = 0 \quad (7)$$

From equation (6) v_1 can be given as:

$$v_1 = \left(\frac{r_{o1}R_p}{R_p + r_{o1} + r_{o1}R_p(sC_1 + sC_p)} \right) \left(\frac{(1+sC_pR_p)V_{out}}{R_p} - g_{m1}v_{in} \right) \quad (8)$$

Substituting the value of v_1 from equation (8) into equation (7) leads to:

$$\frac{r_{o1}R_p}{R_p + r_{o1} + r_{o1}R_p(sC_1 + sC_p)} \left(\frac{(1+sC_pR_p)V_{out} - g_{m1}v_{in}R_p}{R_p} \right) (g_{m2}R_p - g_{mf}R_p - 1 - sC_pR_p) + V_{out} \left(\frac{R_p + sC_Lr_{o2}R_p + r_{o2} + sC_p r_{o2}R_p}{r_{o2}R_p} \right) = 0 \quad (9)$$

The complete transfer function can be written as:

$$A_v(s) = \frac{V_{out}}{V_{in}} = \frac{A_{dc}(1 + \frac{sg_{m1}C_p R_p^2 r_{o1} r_{o2}}{g_{m1}g_{mf}R_p^2 r_{o1} r_{o2} - g_{m1}g_{m2}R_p^2 r_{o1} r_{o2} + g_{m1}R_p r_{o1} r_{o2}})}{\left(1 + s \frac{C_p g_{m2} R_p r_{o1} r_{o2} - C_p g_{mf} R_p r_{o1} r_{o2} - 2C_p r_{o1} r_{o2} + r_{o1}(C_1 + C_p)(R_p + r_{o2}) + r_{o2}(r_{o1} + R_p)(C_p + C_L)}{r_{o1}(g_{m2} r_{o2} - g_{mf} r_{o2} + 1) + R_p + r_{o2}} + s^2 \frac{R_p r_{o1} r_{o2} \{(C_1 + C_p)(C_L + C_p) - C_p^2\}}{r_{o1}(g_{m2} r_{o2} - g_{mf} r_{o2} + 1) + R_p + r_{o2}}\right)} \quad (10)$$

Where

$$A_{dc} = \frac{g_{m1}g_{mf}R_p^2 r_{o1} r_{o2} - g_{m1}g_{m2}R_p^2 r_{o1} r_{o2} + g_{m1}R_p r_{o1} r_{o2}}{g_{m2}R_p r_{o1} r_{o2} - g_{mf}R_p r_{o1} r_{o2} + R_p r_{o1} + R_p^2 + r_{o2} R_p} \quad (11)$$

Let $(g_{m2} - g_{mf})R_p \gg 1$, and equation (11) gets simplified to:

$$A_{dc} \approx \frac{g_{m1} r_{o2} (g_{m2} - g_{mf}) R_p}{(g_{m2} - g_{mf}) r_{o2} + 1 + \frac{R_p + r_{o2}}{r_{o1}}} \quad (12)$$

$$p_1 = \frac{1 + (g_{m2} - g_{mf}) r_{o2} + \frac{R_p + r_{o2}}{r_{o1}}}{(g_{m2} - g_{mf}) r_{o2} R_p C_p - 2C_p r_{o2} + (C_1 + C_p) R_p + (C_L + C_p)(r_{o1} + R_p) \frac{r_{o2}}{r_{o1}}} \quad (14)$$

Assuming that $\frac{(R_p + r_{oi})}{r_{oi}} \approx 1$ and $(g_{m2} - g_{mf})r_{oi} \gg 1$, the equation (14) is simplified as

$$p_1 \approx \frac{g_{m2} - g_{mf}}{R_p((g_{m2} - g_{mf})C_p - \frac{2C_p}{R_p} + \frac{(C_1 + C_p)}{r_{o2}}) + (\frac{1}{R_p} + \frac{1}{r_{o1}})(C_L + C_p)} \quad (15)$$

Since $C_1 \ll C_p$, so equation (15) can be rewritten as:

$$p_1 \approx \frac{g_{m2} - g_{mf}}{R_p C_p} \frac{1}{((g_{m2} - g_{mf}) - \frac{2}{R_p} + \frac{1}{r_{o2}} + \frac{C_1}{C_p r_{o2}} + (\frac{1}{R_p} + \frac{1}{r_{o1}})(\frac{C_L}{C_p} + 1))} \quad (16)$$

If $(g_{m2} - g_{mf}) \gg \frac{2}{R_p} + \frac{1}{r_{o2}} + \frac{C_1}{C_p r_{o2}} + (\frac{1}{R_p} + \frac{1}{r_{o1}})(\frac{C_L}{C_p} + 1)$ then this will transform equation (16) into

$$p_2 = \frac{C_p g_{m2} R_p r_{o1} r_{o2} - C_p g_{mf} R_p r_{o1} r_{o2} - 2C_p r_{o1} r_{o2} + r_{o1}(C_1 + C_p)(R_p + r_{o2}) + r_{o2}(r_{o1} + R_p)(C_p + C_L)}{R_p r_{o1} r_{o2} \{(C_1 + C_p)(C_L + C_p) - C_p^2\}} \quad (18)$$

Further simplification of equation (18) gives:

$$p_2 = \frac{(g_{m2} - g_{mf}) + \frac{C_1 + C_p}{R_p C_p} - \frac{2}{R_p} + \frac{C_1 + C_p}{r_{o2} C_p} + \frac{(C_L + C_p)(r_{o1} + R_p)}{R_p C_p r_{o1}}}{(C_1 + C_L + \frac{C_1 C_L}{C_p})} \quad (19)$$

Since $C_1 \ll C_p$ so $(C_1 + C_L) \gg \frac{C_1 C_L}{C_p}$ and $(C_L + C_1) \approx C_L$,

This assumption reduces equation (19) into

$$p_2 \approx \frac{g_{m2} - g_{mf}}{C_L} \quad (20)$$

It can be seen from the equation (10) that there is only one zero. This can be given as:

Assuming that $\frac{(R_p + r_{oi})}{r_{oi}} \approx 1$ and $(g_{m2} - g_{mf})r_{oi} \gg 1$

The equation (12) will transform into:

$$A_{dc} \approx g_{m1} R_p \quad (13)$$

The poles and zeros of the equation (11) can be approximated as:

$$p_1 \approx \frac{1}{R_p C_p} \quad (17)$$

And the second pole can be estimated as:

$$z_1 \approx \frac{(g_{m2} - g_{mf})g_{m1}R_p^2 r_{o1} r_{o2} - g_{m1}R_p r_{o1} r_{o2}}{g_{m1}C_p R_p^2 r_{o1} r_{o2}} \quad (21)$$

and equation (21) can be rewritten as:

$$z_1 = \frac{(g_{m2} - g_{mf})}{C_p} - \frac{1}{C_p R_p} \approx \frac{1}{C_p} (g_{m2} - g_{mf}) \quad (22)$$

It is clear that if $(g_{m2} - g_{mf})R_p \gg 1$, then $z_1 \gg p_1$
Also if $\frac{C_L}{C_p} \gg 1$,

then $z_1 \gg p_2$

The single zero z_1 of transfer function will lie after pole p_1 and pole p_2 on satisfying above mentioned conditions. If equations (1) and (10) are compared, it is easily noticeable that poles (14-20) are at a higher

frequency in proposed circuit. The dual compensation method gives better results in terms of higher bandwidth and phase margin for amplifier.

2.1.2 Stability

To determine the stability condition of an amplifier, the zero of (10) is neglected and the amplifier is considered

in unity-gain configuration. The closed loop voltage gain results as in equation no. (23). According to Routh-Hurwitz criterion, a second order system is

$$A_{CL}(s) = \frac{1}{\left(1 + s \frac{C_p g_{m2} R_p r_{o1} r_{o2} - C_p g_{mf} R_p r_{o1} r_{o2} - 2 C_p r_{o1} r_{o2} + r_{o1} (C_1 + C_p) (R_p + r_{o2}) + r_{o2} (r_{o1} + R_p) (C_p + C_L)}{r_{o1} (g_{m2} r_{o2} - g_{mf} r_{o2} + 1) + R_p + r_{o2}} + s^2 \frac{R_p r_{o1} r_{o2} (C_1 + C_p) (C_L + C_p) - C_p^2}{r_{o1} (g_{m2} r_{o2} - g_{mf} r_{o2} + 1) + R_p + r_{o2}}\right)} \quad (23)$$

$$C_L < \frac{r_{o1} r_{o2} (C_1 - 2 C_p + (g_{m2} - g_{mf}) C_p R_p) + (r_{o1} - r_{o2}) C_p R_p + r_{o1} C_1 (R_p + r_{o2})}{r_{o2} (R_p + r_{o1})} \quad (24)$$

2.1.3 Slew rate

In a multistage amplifier, the slowest stage limits the slew rate. The slewing period further depends on the values of lumped capacitors at related nodes and the current available to drive these capacitors. In the proposed circuit the compensation capacitor C_p and the capacitor C_L at the final stage are responsible for the slew rate of circuit. If the currents driving C_p and C_L are denoted by I_1 and I_2 respectively, then slew rate SR of the amplifier is given by:

$$SR \approx \min\left(\frac{I_1}{C_p}, \frac{I_2}{C_L}\right) \approx \frac{I_2}{C_L} \quad (25)$$

$$SR \approx \frac{I_2}{C_L} \quad (26)$$

Since the value of compensation capacitor C_p is very small as compared to load capacitor C_L , so the slew rate is limited by rightmost expression in equation no. (25). The slew rate is a very important recital parameter which controls maximum frequency of the output signal as well as constraints of the settling time during the transient response.

2.1.4 Noise

The input referred noise is the equivalent noise that would be needed at the input source to generate the calculated output noise in a noiseless circuit. Hence it indicates that how much the input signal is corrupted by the circuit's noise. Since noise in a multistage amplifier is mostly dominated by the first stage so in the circuit topology shown in Fig. 2(b), the input noise spectral density is mostly by M_1 , M_2 , M_3 and M_4 . Flicker noise is ignored as it is significant only at lower frequencies. The total input-referred thermal noise ($v_{n,in}^2$) can be expressed as:

stable if all poles have non-positive real part. Using this criterion the necessary condition of stability for given circuit is expressed in equation no. (24). The circuit is unconditionally stable if and only if this equation is satisfied. It also sets a low limit to C_L depending on C_1 and C_p .

$$\overline{v_{n,in}^2} \approx 2 \overline{v_{n1}^2} + 2 \frac{g_{m3}^2}{g_{m1}^2} \overline{v_{n3}^2} = 8kT \left(\frac{2}{3g_{m1}} + \frac{2g_{m3}}{3g_{m1}^2} \right) \quad (27)$$

Where g_{mi} is the trans-conductance of i^{th} MOS (where $i=1,2,3,\dots$), k is Boltzmann constant and T is the absolute temperature. Noise is a random process and it trades with power dissipation, speed and linearity. Hence it is required to analyze the noise behavior of a circuit.

3. SIMULATION RESULTS

The work proposed here is gain-bandwidth product (GBW) enhancement of a two stage amplifier circuit using dual frequency compensation approach. The circuit shown in Fig. 2(b) is simulated using 0.18 μm process parameters and total bias current in circuit is 0.9 mA from a 1.5 V supply. Table 1 is included here to list all circuit parameter and their values. It can be seen from Table 1 that required compensation capacitor value is also minimized which can save chip area.

Table 1. Various circuit parameters for proposed circuit

Circuit parameter	Value
Technology	0.18 μm
Power supply	1.5V
DC bias current	900 μA
Aspect ratio	M1,M2,M3=70/1
	M4,M5,M6=40/1
	M7=20/1
	M8=50/1
Passive component R_p, C_p	3.3K, 1pF

The output voltage of the circuit presented in this paper changes at a faster rate with respect to time and slew rate (+/-) measured is 113.6/83.3 V/ μ s. Fig.4 shows the simulated transient response with a 10pf load which clearly exhibit that the circuit offers higher average slew rate of 98V/ μ s as compared to conventional circuit [3]'s 60V/ μ s. The gain bandwidth product is 150MHz and phase margin is 53° in the proposed circuit (Fig. 5) whereas for the conventional amplifier [3] GBW and PM are 100MHz and 55° respectively. The gain and phase response curves with proposed compensation technique and with no compensation technique are shown in Fig. 5 and 6 respectively. Fig. 5 makes it obvious that using dual compensation technique GBW and phase margin have been improved.

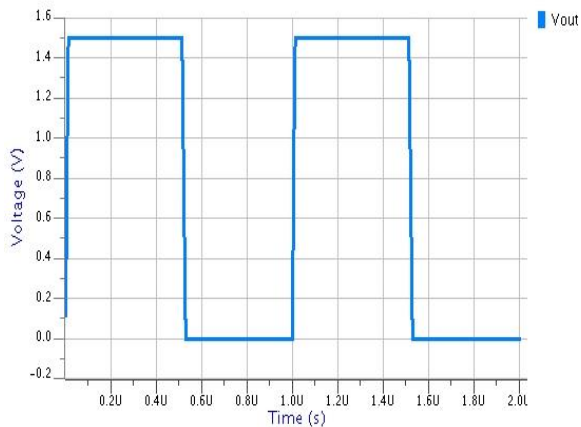


Fig. 4. Transient response with 500pF load

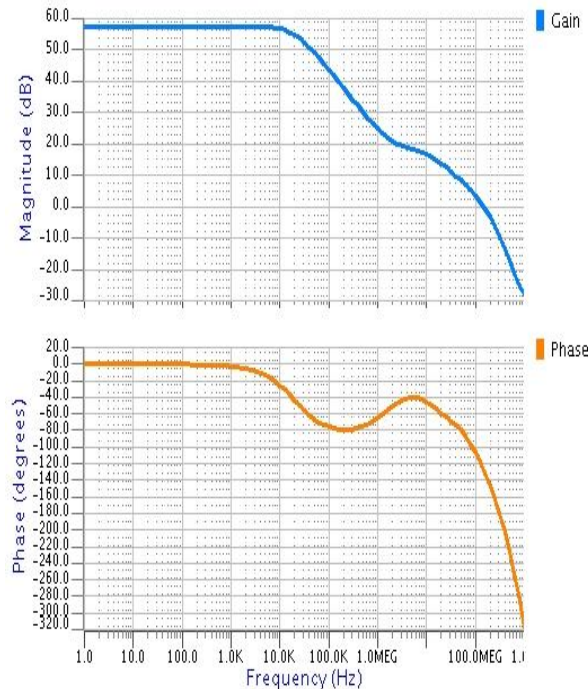


Fig. 5. Gain and phase response with proposed compensation technique

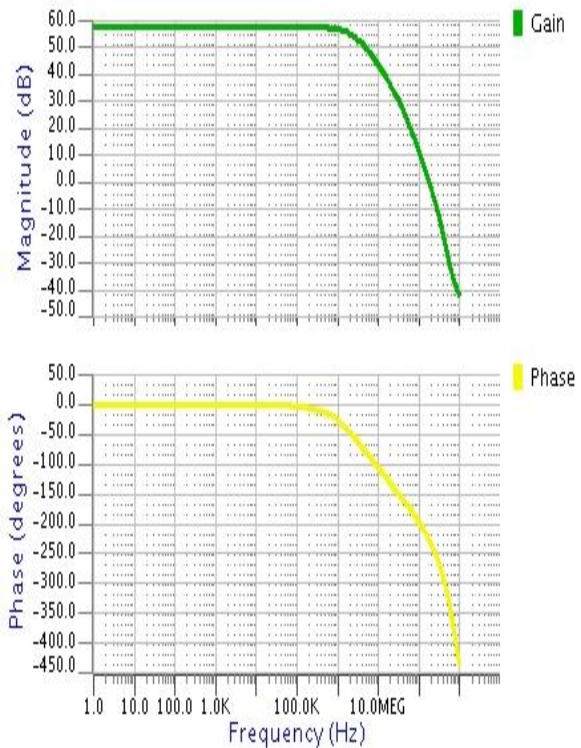


Fig. 6. Gain and phase response without any compensation technique

The DC response is shown in Fig. 7 which clearly exhibit enhanced stability of proposed circuit.

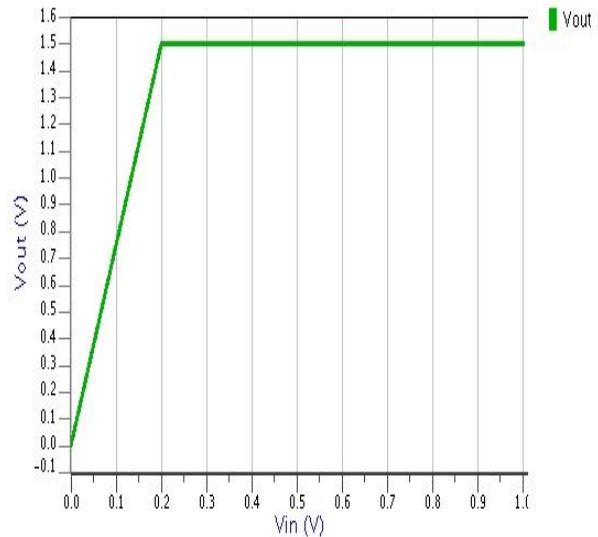


Fig.7. DC response of the proposed circuit

The proposed circuit has also been simulated for different values of load capacitor C_L . Fig. 8 illustrates the simulated frequency and phase response of the proposed amplifier with different load capacitors and it

can be seen that this technique performs well even for different value of load capacitors. The amplifier achieves a GBW of 149,150 and 151 MHz with a phase margin of 50° , 53° and 53.1° for $C_L=100\text{pF}$, 500pF and 1nF , respectively. The variation in output impedance versus frequency is plotted as Fig. 9. From Fig. 9, it can be verified that the output impedance (z_{out}) of the proposed circuit is constant till 10MHz frequency and equals to 115Ω , whereas at higher frequencies it decreases at a fast rate. This reduction results into larger current at the output and also validates that by using an impedance element between input and output the bandwidth of a circuit can be altered. The z_{out} of circuit is equal to 110Ω at 100 MHz and 100Ω at 200 MHz frequency.

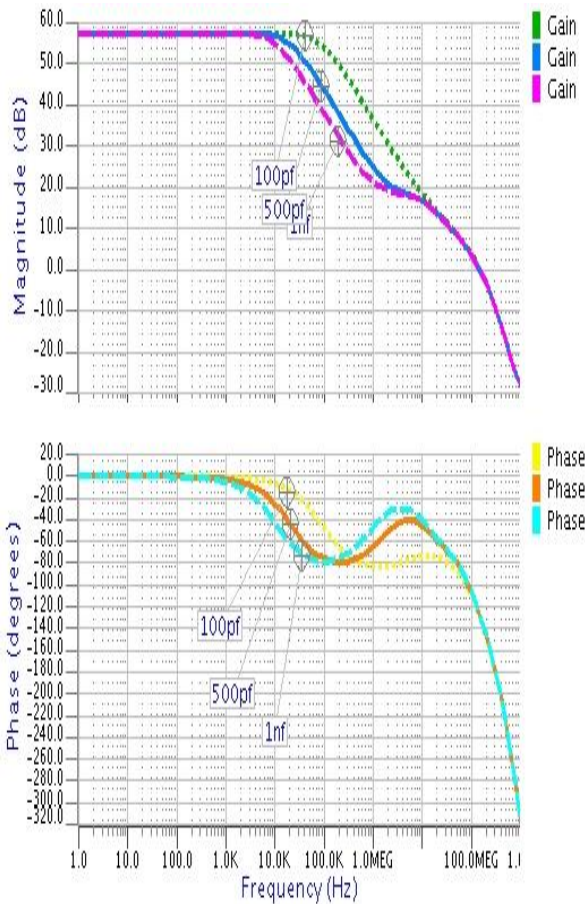


Fig.8. Gain and phase response of the proposed circuit for different values of load capacitance $C_L=100\text{pF}, 500\text{pF}, 1\text{nF}$

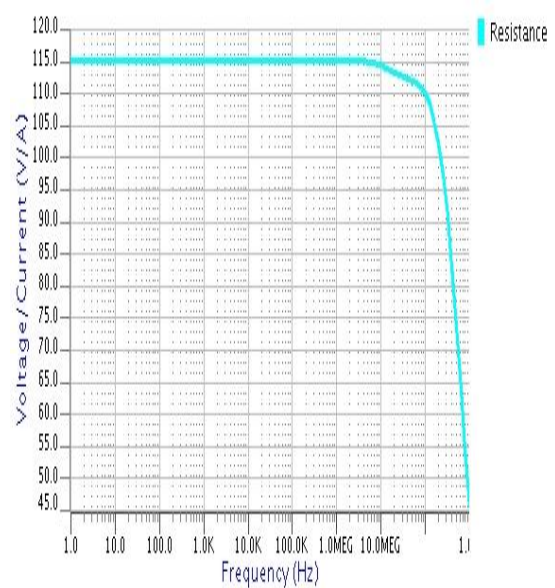


Fig.9. The output impedance of the proposed circuit

The Monte Carlo simulation of the proposed amplifier is performed to evaluate the effect of 5% mismatch in transistor's threshold voltage and aspect ratio with Gaussian distribution (200 runs) on transient response and shown in Fig. 10. The maximum and minimum transit time obtained in Monte Carlo simulation is $0.61 \mu\text{s}$ and $0.82 \mu\text{s}$, respectively. The mean and standard deviation are $0.665 \mu\text{s}$ and $0.07 \mu\text{s}$ respectively for the proposed circuit. The layout of the circuit is shown in Fig. 11. The total area utilized by the circuit including passive components R_p and C_p is 0.017mm^2 whereas the conventional amplifier [3] occupies more area using same technology. To examine the effect of process and temperature variations on GBW, phase margin and average slew rate of the amplifier for $C_L=500\text{pF}$, corner simulation is done and results are summarized in table 2. The simulated amplifier remains stable with minimum GBW of 129.42 MHz and phase margin of 52.18° . The deviation in GBW and phase margin over various corners is $\pm 15\%$ and $\pm 5\%$, respectively. The minimum average slew rate across the extreme temperature and process corners is $91 \text{ V}/\mu\text{s}$. Hence the proposed circuit shows high stability

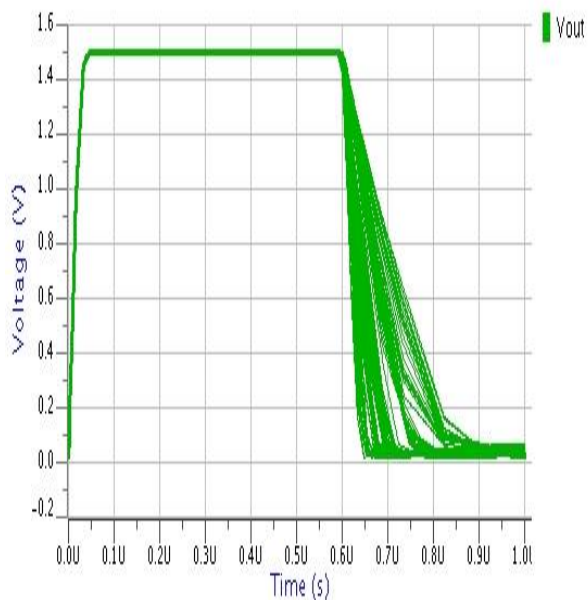


Fig.10. The Monte Carlo analysis (200 runs) on applying 5% mismatch in transistor’s threshold voltage and aspect ratio of transient response of the circuit

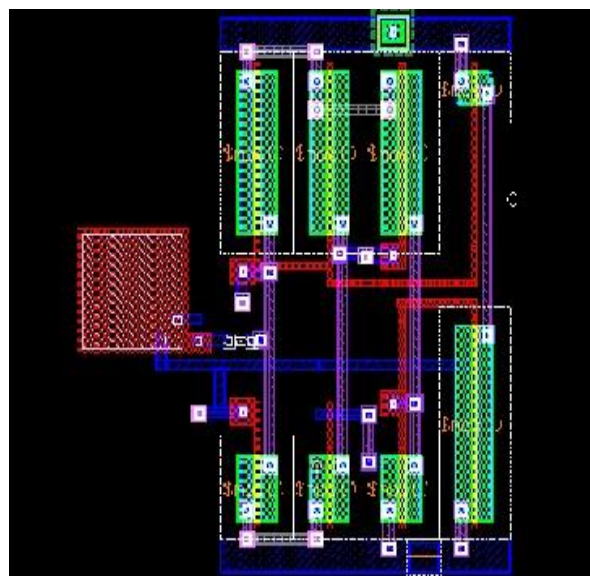


Fig. 11. Layout of the proposed circuit

Table 2. The performance of the proposed circuit at $C_L=100\text{pf}$ over process and temperature corners

+27°C					
Corner	TT	SS	FF	SNFP	FNSP
GBW(MHz)	150	141.22	156.32	143.13	145.06
PM(deg)	53	53.41	53.62	53.24	53.81
Average slew rate(V/μs)	98	94	103	96	97
-40°C					
Corner	TT	SS	FF	SNFP	FNSP
GBW(MHz)	162.24	158.81	170.86	163.45	163.64
PM(deg)	54.56	54.42	54.78	54.16	55.11
Average slew rate(V/μs)	100	95	105	97	99
+100°C					
Corner	TT	SS	FF	SNFP	FNSP
GBW(MHz)	132.56	129.42	142.80	130.91	132.61
PM(deg)	53.09	52.18	53.51	53.24	53.28
Average slew rate(V/μs)	96	91	102	94	96

4. FIGURE OF MERIT

In order to compare various techniques (independent of technology) used for the bandwidth extension of amplifiers, two figure of merits [8] are defined as;

$$FOM_1 = GBW[\text{MHz}] \cdot C_L[\text{pF}] / I(\text{mA})$$

and

$$FOM_2 = \text{slewrates} \cdot C_L[\text{pF}] / I(\text{mA})$$

There is always a tradeoff between high gain bandwidth product (GBW) and phase margin. Table 3 compares several high performance amplifier designs using compensation of last few years in terms of GBW, phase margin, supply requirement, power consumption, slew rate and size of compensation capacitor. A larger FOM implies a better frequency compensation

topology. From Table 3, it is clear that the proposed scheme achieve highest gain bandwidth product and FoMs. The value of load capacitor C_L is higher than frequency compensation [3], self-biased amplifier [4] and active feedback [10] and exhibit that this technique works well with high load capacitance. The other parameters such as slew rate and phase margin have also been improved when compared to self-biased amplifier [4] and hybrid cascade [8]. The value of compensation capacitor is comparable with all other techniques. The power consumption is higher in

proposed work but other it offers very high slew rate and good circuit stability. Hence it is clear that proposed dual compensation gives a significant improvement over other existing designs listed in Table 3. The Performance of an amplifier depends on many other important parameters such as for example: offset, power consumption, linearity, output resistance, area, etc. All necessary simulations to carry out these values are done and results are summarized in table 4.

Table 3. The Performance comparison of different compensated amplifiers

	This work	[2]	[3]	[4]	[8]	[10]
GBW(MHz)	150	1.73	100	35	2.41	4.5
Phase Margin(°)	53	53	55	>45	51	65
C_p (pf)	1	1.1	N.A.	N.A.	.80	>5
C_L(pf)	500	500	15	>5.5	500	120
Slew rate(V/μs)	98	.53	60	19.5	.74	1.5
FoM₁(MHz.pF/mA)	83,333	39,300	1578	2116	54,770	2700
FoM₂(pF.SR/mA)	54,440	12,045	948	1180	16,818	900
Power (mW)	3.2	.0204	1.7	N.A	N.A.	.4
Area (mm²)	.017	.0088	.25	.0123	.0069	.06
Technology(μm)	.18	.065	.18	.13	.09	.8

Table 4. The simulation results for typical conditions

Parameter	Simulated results	Unit
Gain	58	dBS
Gain bandwidth product	150	MHz
Phase Margin	50	degrees
Gain Margin	9.2	dB
Slew Rate(+/-)	113.6/83.3	V/ μ s
Input referred noise @150MHz	5.6	nV/ \sqrt{Hz}
Input linearity Range	200	mV
Output voltage swing	1.5	V
Input offset voltage	8.9	mV
Output resistance@150MHz	105	Ohms
Power consumption	3.2	mW

5. CONCLUSION AND FUTURE WORK

A dual compensation technique based on a direct feed-forward network from output of first stage to output of second stage together with a passive r-c compensation between input and final output of two stage amplifier circuit is presented here. The proposed design exhibits better performance compared to most others and is capable to achieve very high speed and stability over a vast frequency range. Furthermore, the value of compensation capacitor used here is very small which in turn significantly reduces die area.

Possible future work may include application of this compensation scheme to those amplifiers which have more number of cascaded stages. An active frequency compensation technique can also be tried to internally compensate amplifier as it will separate low-frequency high gain path and high frequency signal path and thereby it can improve performance.

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