A Low Noise Amplifier with Low Voltage, Low Power Consumption, and Improved Linearity at 5 GHz

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ABSTRACT
In this paper a low-noise amplifier with 0.6V supply voltage, low power consumption, and improved linearity at 5GHz is introduced in 0.18 µm CMOS technology. By using a feed-forward structure and a multi-gated configuration in the proposed circuit, linearity of the circuit is significantly improved, while only 122 µW more power is consumed compared to conventional folded cascode structure, and the other circuit parameters are similar. In addition, the Volterra series is used for nonlinear analysis and to evaluate the linearity improvement of the proposed circuit. There is also a noteworthy superiority over compared published works in the figure of merit. The suggested low-noise amplifier (LNA) at 1.28mW DC power consumption provides 9.6dB gain and a noise figure of 3.24dB. It is achieved whilst the third order interception point has been improved by 10dB and equals 0.0dBm. In the operating frequency the circuit displays satisfactory input and output impedance matching. Finally, throughout the whole circuit bandwidth input and output isolation is below −27dB.

KEYWORDS: Low Noise Amplifier (LNA), Folded Cascode Structure, Low Power Consumption, Low Supply Voltage, Improved Linearity.

1. INTRODUCTION

Increasing demand for mobile wireless systems has driven the development of radio frequency integrated circuits (RFICs). To prolong the battery life of these systems, power consumption is continuously being reduced. In applications like wireless medical telemetry, low power consumption plays a significant role. In such applications, the portable device should be able to operate from an ultra-low voltage supply or environmental energy such as solar cells. Therefore, optimization of power consumption and supply voltage are two key factors which should be considered by designers [1-2]. Advancement of technology in size reduction of MOSFETs, has facilitated designing high-gain, low-noise amplifiers, with low power consumption. However, linearity has, so far, not been improved [3]. Linearity is one of the key factors in RF circuits, considering that non-linearity causes a lot of issues like intermodulation and gain compression.

There are many different linearization methods for a CMOS LNA. To date, the most efficient ones reported have been the derivative superposition (DS) technique [4-5], modified DS [6-7], and complementary DS [8]. While linearity is improved, these methods struggle to control the quality factor (Q) of the input matching network, which has a lot of influence on the low noise optimization [3].

Moreover, improving linearity of the circuit is very challenging without detriment to other key factors, such as gain and noise, in voltage and power consumption restricted designs. This article attempts to significantly improve linearity by a slight increase in power and without influence to other parameters. It is performed by adding two auxiliary transistors to the conventional folded cascode structure and employing a multi-gated configuration in the first stage, and a feed-forward technique in second.

Organization of the article is as follows: In section 2 the folded cascode structure is briefly reviewed.

Section 3 contains an explanation about the proposed LNA and design related topics. Additionally, the Volterra series is used as a non-linear analysis method to evaluate the linear behavior of the circuit. In section 4, the simulation results of the suggested circuit are presented and compared with several similar works. Finally, section 5 concludes the paper.

2. LNA WITH FOLDED CASCODE STRUCTURE

One of the conventional structures for designing low noise, low voltage amplifiers is the folded cascode structure (Fig. 1), where transistors M_1 and M_2 form the structures first and second stage, respectively. Input impedance matching is handled by inductances L_g and L_s, while inductance capacitance network L_o, C_o controls the output impedance matching.

It is possible to reduce the supply voltage of the folded cascode structure down to the threshold voltage, due to the absence of stacking gain stages. When compared with other low voltage LNA topologies, the folded cascode displays remarkably superior amplifier linearity and noise figure [9].

Nonlinear behavior of MOSFETs has two main sources. One is the nonlinear transconductance g_m, which converts the linear input voltage to a nonlinear output drain current. The second is the nonlinear output transconductance g_{ds} [10]. g_{ds} effect is ignored in the equations in order to ease calculations. However, g_{ds} non-linearity is minimized by using the adopted cascode topology [10]. In the following, the proposed improved structure for compensating the nonlinear behavior is demonstrated.

3. PROPOSED LINEARITY IMPROVED FOLDED CASCODE LNA

Fig. 2 depicts a schematic of the proposed linearity improved LNA. This LNA is designed for 5GHz working frequency and 0.6V supply voltage. As it is depicted in Fig. 2, using multi-gated configuration, transistor M_4 is added to the first stage of the conventional folded cascode LNA structure. Also, using a feed-forward structure, transistor M_3 and inductor L_1 are added to the second stage. Capacitors C_1, C_2, and C_3 are coupling capacitors. By choosing proper gate voltage and proper scaling for transistor M_4 in the first stage, an appropriate value for inductor L_1, as well as, gate voltage and scaling for transistor M_3 in the second stage, the third order intermodulation factors produced by transistors M_1 and M_2 would be suppressed noticeably. Although adding inductor L_1 to the circuit will increase size of the chip, the abovementioned benefits justify it.

Considering the fact that transistor M_3 is added to the circuit in series, it does not increase the power consumption of the circuit, since it reuses the bias current of transistor M_2. Moreover, transistor M_4 is used to suppress the nonlinear components of transistor M_1. Since transistor M_4 is biased in the sub-threshold region, therefore, the power consumption of this transistor is insignificant compared with other transistors in the structure. To clarify the method used for improving the circuit linearity, and the effect of adding transistors M_3 and M_4, linear analysis of the circuit using the Volterra series is first performed in the absence of transistor M_4. Then, adding transistor M_4 to the circuit, the effect of this transistor on linearity and other parameters is evaluated.

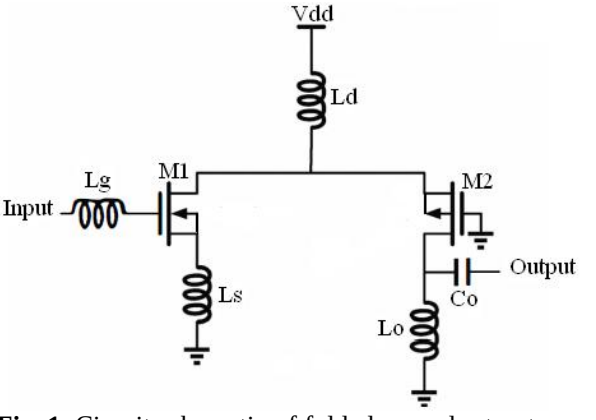


Fig. 1. Circuit schematic of folded cascode structure

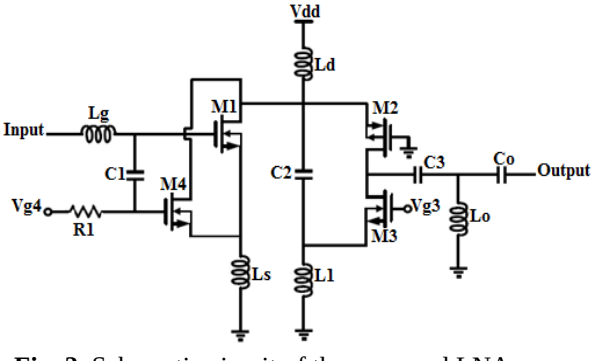


Fig. 2. Schematic circuit of the proposed LNA

3.1. NONLINEAR ANALYSIS USING VOLTERRA SERIES

The Volterra series, like the Taylor series, is used for modeling non-linear behavior. In Volterra series analysis, each significant nonlinear element is described by a power series in terms of its small signal control voltage [11]. Common nonlinear behavior of MOSFETs is due to the voltage to current conversion (V-I) in them. Fig. 3 shows the proposed LNA in the absence of transistor M_4. Capacitor C_x is added to the structure at the first stage for simultaneous input power and noise matching, under restricted power consumption, using PCSNIM technique [12].

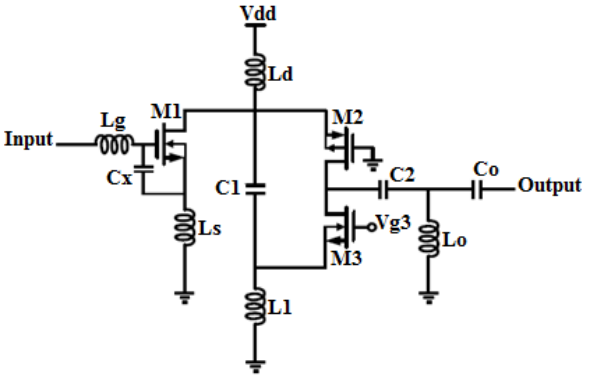


Fig. 3. Schematic of proposed LNA circuit in the absence of transistor M_4

Ignoring the effect of channel length modulation (CLM), the drain current in transistors M1, M2 and M3 versus their gate source voltages, can be approximated as follows:

$$i_1 = g_{11}V_{gs1} + g_{12}V_{gs1}^2 + g_{13}V_{gs1}^3 \quad (1)$$

$$i_2 = g_{21}V_{sg2} + g_{22}V_{sg2}^2 + g_{23}V_{sg2}^3 \quad (2)$$

$$i_3 = g_{31}V_{gs3} + g_{32}V_{gs3}^2 + g_{33}V_{gs3}^3 \quad (3)$$

In which the transconductance components of each transistor of order one to three can be described as follows:

$$g_{mi} = \frac{1}{i!}\frac{\partial^i I_D}{\partial V_{gs}^i} \quad (4)$$

The Vgs_1 and i_1 values can be expanded using Volterra series as follows:

$$V_{gs1} = A_1(s_1)\circ V_i + A_2(s_1,s_2)\circ V_i^2 + A_3(s_1,s_2,s_3)\circ V_i^3 \quad (5)$$

$$i_1 = B_1(s_1)\circ V_i + B_2(s_1,s_2)\circ V_i^2 + B_3(s_1,s_2,s_3)\circ V_i^3 \quad (6)$$

Where in (5) and (6), $X_1(s_1)$, $X_2(s_1; s_2)$ and $X_3(s_1; s_2; s_3)$ are first, second and third nonlinear coefficients, respectively. The operator "o" means that the magnitude and phase of each spectral component of V^n_i is to be changed by the magnitude and phase of $X_n(s_1; s_2; s_3)$, where the frequency of the component is $\omega_1 \neq \omega_2 \neq \cdots \neq \omega_n$ [6]. Using Kirchhoff's laws in the first stage, the following relations are derived:

$$sC_{t1}V_{gs1} + i_1 = \frac{V_{s1}}{sL_s} \quad (7)$$

$$V_{s1} = V_i - V_{gs1}(1 + s^2C_{t1}L_g) \quad (8)$$

Where V_{s1} represents the source voltage of transistor M_1, and C_{tl} is the addition of the gate-source capacitor of $M_1(C_{gs1})$ and capacitor C_x. Using (8) in (7) we would have:

$$i_1 = -V_{gs1}\left(sC_{t1} + \frac{1 + s^2C_{t1}L_g}{sL_s}\right) + \frac{V_i}{sL_s} \quad (9)$$

Considering (1) and (9) can be rewritten as:

$$x_1(s)V_{gs1} + g_{12}V_{gs1}^2 + g_{13}V_{gs1}^3 = \frac{V_i}{sL_s} \quad (10)$$

Where we define:

$$x_1(s) = g_{11} + sC_{t1} + \frac{1 + s^2C_{t1}L_g}{sL_s} \quad (11)$$

To derive the linear transfer function of $A_1(s_1)$ the voltage $Vi = e^{s1t}$ should be applied to the circuit. Equation (10) can be linearized as follows:

$$x_1(s)A_1(s_1).V_i = \frac{V_i}{sL_g} \quad (12)$$

Therefore, the linear transfer function of (5) would be,

$$A_1(s_1) = \frac{1}{s_1L_sx_1(s_1)} \quad (13)$$

To determine the second order nonlinear transfer functions, $V_i = e^{S_1t} + e^{S_2t}$ should be applied to the circuit. Using (5), by considering the nonlinear second-order terms of (10), the second order nonlinear transfer function is:

$$A_2(s_1,s_2) = \frac{-g_{12}}{s_1s_2L_s^2x_1(s_1+s_2)x_1(s_1)x_1(s_2)} \quad (14)$$

Then, defining $s_1 = s_2 = s_a$ and $s_3 = -s_b$ and assuming a very small distance between two frequency components, $s_a \approx s_b \approx s$, the third order transfer function is obtained:

$$A_3(s_a,s_a,-s_b) = \frac{g_{13}x_1(2s) - 2g_{12}^2}{3s^3L_s^3x_1^3(s)x_1(2s)x_1(-s)} \quad (15)$$

Considering the derived first to third order coefficients for V_{gs1}, (5), and (6), the coefficients of current i_1 are:

$$B_1(s_1) = \frac{g_{11}}{s_1L_sx_1(s_1)} \quad (16)$$

$$B_2(s_1,s_2) = \frac{g_{12}(x_1(s_1+s_2)-g_{11})}{s_1s_2L_s^2x_1(s_1+s_2)x_1(s_1)x_1(s_2)} \quad (17)$$

$$B_3(s_a,s_a,-s_b) = \frac{(g_{11} - x_1(s))(g_{13}x_1(2s) - 2g_{12}^2)}{3s^3L_s^3x_1^3(s)x_1(2s)x_1(-s)} \quad (18)$$

According to (2) and (3) the output current can be described as:

$$i_{out} = i_2 - i_3 = g_{21}V_{sg2} + g_{22}V_{sg2}^2 + g_{23}V_{sg2}^3 - g_{31}V_{gs3} - g_{32}V_{gs3}^2 - g_{33}V_{gs3}^3 \quad (19)$$

Since we can write $V_{sg2}=V_{sg3}=V_A$ (19) can be reformulated in the following way:

$$i_{out} = (g_{21} + g_{31})V_A + (g_{22} - g_{32})V_A^2 + (g_{23} + g_{33})V_A^3 \quad (20)$$

According to (20), it can be observed that by adding transistor M_3, the effective output transconductance increases and the second order nonlinear component (IM2) of the output decreases, since g_{22} and g_{32} are of

the opposite sign. Also, the third order nonlinear coefficient (IM3) of the output can be reduced because g_{23} and g_{33} can be different in sign. Choosing proper transistor size and gate voltage for M_3, we can design for $g_{22} = g_{32}$ and $g_{23} = -g_{33}$ and therefore, according to (20) achieve improved circuit linearity. With these conditions we would have:

$$i_{out} = (g_{21} + g_{31})V_A = C_1(s_1).V_i + C_2(s_1, s_2).V_i^2 + C_3(s_1, s_2, s_3).V_i^3 \quad (21)$$

Applying KCL at the node of the drain of transistor M_1, we have:

$$i_{out} = \frac{-(g_{21} + g_{31})i_1}{x_2(s)} \quad (22)$$

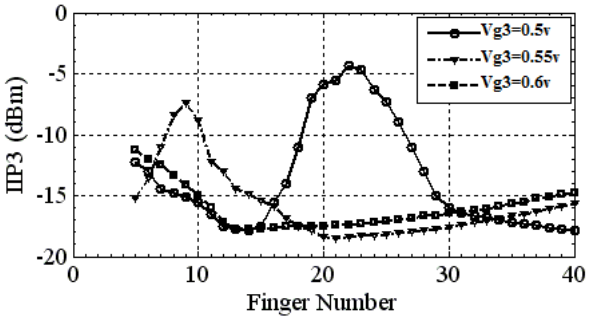


Fig. 4. Variations of IIP3 of the proposed circuit versus the finger number of transistor M_3, with different gate voltages in the absence of transistor M_4. (W=Finger Number×8µm)

Such that:

$$x_2(s) = g_{21} + g_{31} + \frac{1}{sL_d} + \frac{1}{sL_1} + sC_{tot} \quad (23)$$

In which $C_{tot} = C_{gs2} + C_{gs3}$ Using (6) and (22) the coefficients of the output current nonlinear Volterra series for n=1,2,3 can be derived as follows:

$$C_n(s_1, s_2, \dots, s_n) = \frac{-(g_{21}+g_{31})B_n(s_1,s_2,\dots,s_n)}{x_2(s_1+s_2+\cdots+s_n)} \quad (24)$$

It can be seen from (24) that the first to third order nonlinear coefficients of output current are only related to the first to third order nonlinear coefficients of the first stage current. Consequently, using this method, the effect of nonlinear behavior of transistor M_2 can be suppressed to an acceptable level. Next, considering the IIP3 formulation in (25) and $Z_s(s) = Z_{in}(-s)$, the IIP3 can be calculated using (26).

$$IIP_3 = \frac{1}{6Re(Z_s(s))}\left|\frac{C_1(s_a)}{C_3(s_a,s_a,-s_b)}\right| \quad (25)$$

$$IIP_{3Circuit} = \frac{1}{2}\left|\frac{s^2C_{t1}L_sx_1^2(s)x_1(2s)x_1(-s)}{(g_{11}-x_1(s))(g_{13}x_1(2s)-2g_{12}^2)}\right| \quad (26)$$

Variations of IIP3 versus variations of transistor M_3 width and gate voltage (V_{gs}), in the absence of the transistor M_4, are depicted in Fig. 4. The widths of transistors M_1 and M_2 are $W_1 = 9 \times 8$ µm and $W_2 = 18 \times 8$ µm. As can be observed in Fig. 4, the circuit gives the best linear results with a voltage of $V_{g3} = 0.5$V and 22 fingers for transistor M3. In this state, the IIP3 of the circuit is equal to −4.3dBm. Figures 5(a) and 5(b) illustrate the noise figure and gain in this state. Considering Fig. 5, it can be observed that the gain of the circuit at 5GHz is almost equal to that of the conventional folded cascode, although the noise figure suffers a slight increase. Subsequently, transistor M_4 is added to the structure to reduce the nonlinear behavior of the common source transistor, M_1 (Fig. 6). As can be seen in Fig. 6, transistor M_4 replaces capacitor C_x in the circuit illustrated in Fig. 3, using the multi-gated configuration to improve the nonlinear behavior of transistor M_1 in the first stage [13].

This transistor should operate in the weak inversion, or sub-threshold region, so it can compensate for the unwanted effects of the third order current component of M_1 [13].

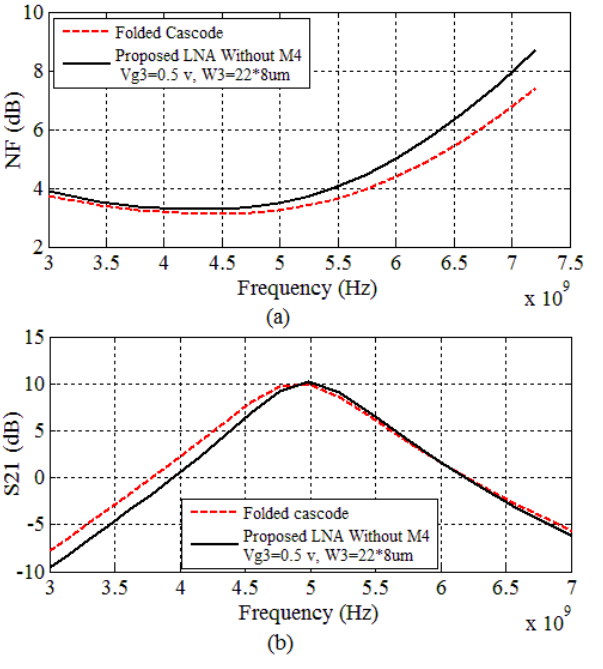


Fig. 5. The noise figure (a) and gain (b) of the proposed LNA in the absence of the transistor M_4 (solid lines) and the LNA with conventional folded cascode structure (dashed lines).

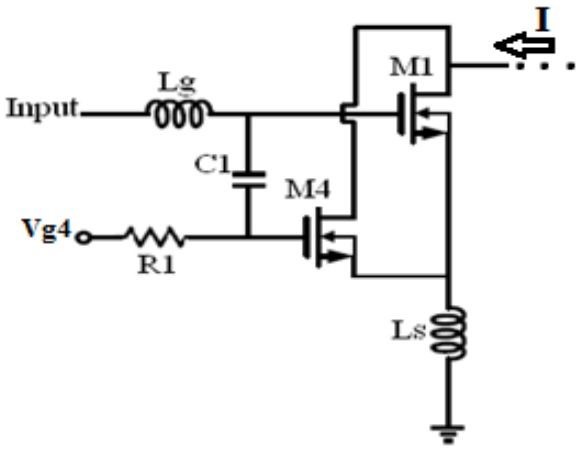


Fig. 6. Schematic of the first stage of the proposed circuit

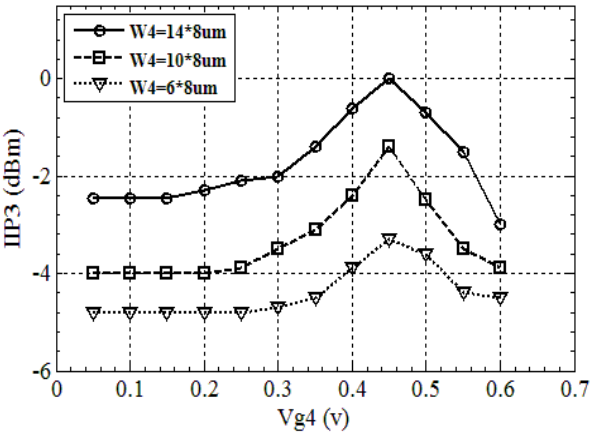


Fig. 7. Variations of IIP3 of the proposed LNA versus various gate voltages and widths of transistor M_4

be significantly lower compared to other transistors in the structure. In addition, the increase in the size of transistor M_1 results in an increased capacity of the gate-source capacitor. Since the output current in this stage is the result of adding the currents of transistors M_1 and M_4, the increased gate- source capacitance of M_4 results in a better matching of the input impedance with the optimum noise impedance, to reach the minimum noise in the circuit. Adding capacitor C_x in order to reach the minimum noise through reduction in gate- source voltage causes a decrease in the output current of the first stage, and consequently a decrease in gain. However, the increased gate-source capacitance of M_4 compensates the unwanted effects on the gain of the circuit caused by adding capacitor C_x.

The drain current of the two transistors M_1 and M_4 are defined as follows:

$$I_{d1} = I_{DC1}+g_{m11}V_{gs1}+g_{m12}V_{gs1}^2+g_{13}V_{gs1}^3 \quad (27)$$

$$I_{d4} = I_{DC4}+g_{m41}V_{gs4}+g_{m42}V_{gs4}^2+g_{43}V_{gs4}^3 \quad (28)$$

Considering that $V_{gs1} = V_{gs4}$ the output current of these two transistors is:

$$I = (I_{DC1}+I_{DC4}) + (g_{m11}+g_{m41})V_{gs1} + (g_{m12}+g_{m42})V_{gs1}^2 + (g_{m13} + g_{m43})V_{gs1}^3 \quad (29)$$

According to (29), by choosing a proper size and gate voltage for transistor M_4 the third order component of the current of transistor M_1 can be absorbed and its effect suppressed. Fig. 7 shows the variations of IIP3 of the circuit versus size and gate voltage variations of transistor M_4. The width and gate-source voltage of transistor M_3 are taken to be $W_3 = 22 \times 8$ µm and $V_{gs} = 0.5$ V.

As can be observed in Fig. 7, by gradually increasing the size of transistor M_4 and, therefore, increasing its effect on the first stage, the improved linearity of the circuit which had reached −5dBm by adding transistor M_4, starts to increase (Fig. 4).It can be seen in Fig. 7 that by choosing a width of $W_4 = 14 \times 8$ µm and gate-source voltage $V_{gs} = 0.45$ V for transistor M_4, the circuit would have a desirable linear behavior. Additionally, in choosing the size of transistor M_4, power consumption should also be considered. In this state, the IIP3 of the circuit will be 0.0dBm. Furthermore, choosing $V_{gs} = 0.45$V and increasing the width of transistor M_4, capac- itor C_{gs4} would also increase. This increase would result in a better noise matching in the input, and therefore improvement of the overall noise of the circuit. The effect of increasing the width of transistor M_4 on the circuit noise is shown in Fig. 8. As can be seen, choosing $W_4 = 14 \times 8$ µm, the noise of the circuit at 5GHz is very close to the minimum noise.

The cost of improvements in linearity and noise is that increasing the width of transistor M_4 also increases its power consumption. A choice of width will therefore be a compromise between these parameters. Power consumption for each transistor is tabulated in Table 1.

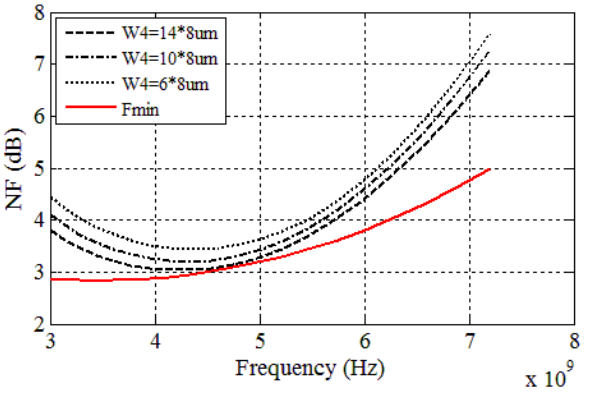


Fig. 8. Variations of noise of the proposed LNA versus different sizes for transistor M_4

Table 1. Power consumption and transconductance of each of the Transistors

Transistor	(M1)	(M2)&(M3)	(M4)
Width (µm)	9 × 8	18 × 8 , 22 × 8	14 × 8
PDC (µW)	834	306	144
gm (mA/V)	16.5	6.9 , 9.7	4.8

4. SIMULATION RESULTS

The proposed LNA has been simulated by HSPICE RF simulator using 0.l8µm CMOS process BSIM3 model. Spiral inductors are used for the inductors and metal-insulator-metal (MIM) capacitors are used for the capacitors in the simulation. Characteristics of applied devices in simulation are tabulated in Table 2. The simulated LNA operates with a 0.6V supply voltage and consumes 1.28mW of power. In order to evaluate the linearity of the proposed LNA, the two-tone test is used, in which two single frequency signals with the same power at 5GHz and 5.01GHz are applied to the circuit. In Fig. 9, output power variation of the main signal and its third order intermodulation components versus input power before and after linearization is depicted.Figure 9 shows that the IIP3 is improved by 10dB to a value of 0.0dBm.

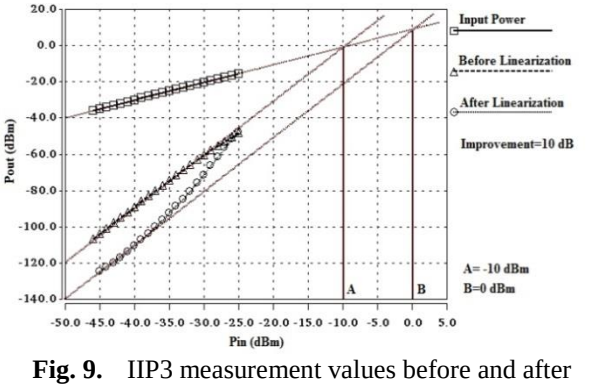
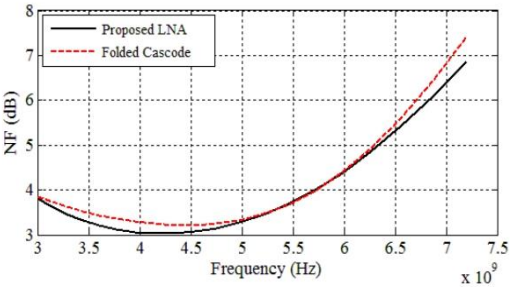


Fig. 9. IIP3 measurement values before and after linearization.

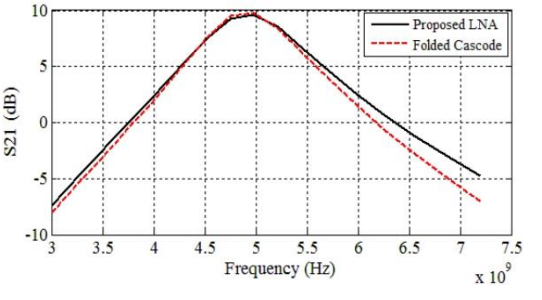
Table 2. Proposed lna operates with 0.6v supply voltage and consumes 1.28mw power.

Devices	Design Values
M1	9 × 8µm/0.18µm
M2	18 × 8µm/0.18µm
M3	22 × 8µm/0.18µm
M4	14 × 8µm/0.18µm
Ls	N = 1 , R = 70 µm
Lg	N = 2.5 , R = 110 µm
Ld	N = 2 , R = 125 µm
L1	N = 5 , R = 125 µm
Lo	N = 2 , R = 114 µm
Co	W = 14 µm , L = 14 µm

N: number of inductor turns, R: inner radius of inductor, for all inductors W = 15 µm.



(a)



(b)

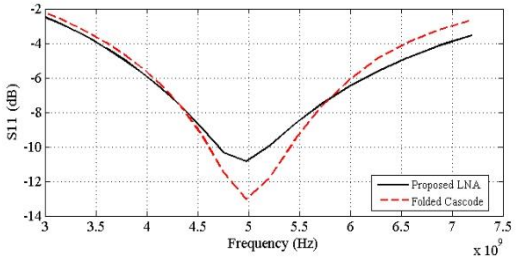
Fig. 10. **a.** noise figure **b.** gain of the presented LNA (solid lines) and the conventional folded cascode structure LNA (dashed lines).

At 5GHz the proposed LNA has a noise figure (NF) of 3.24dB and voltage gain (S21) of 9.6dB shown in Fig. 10, where the dashed lines and solid lines indicate the simulated values before and after linearization. Figure 11 indicates the input reflection coefficient (S_{11}) and the output reflection coefficient (S_{22}). In the frequency of 5 GHz the input and output reflection coefficients are -10.8 dB and -19.8 dB, respectively. Moreover, for the whole bandwidth of the circuit, isolation is below -27 dB. To evaluate the performance

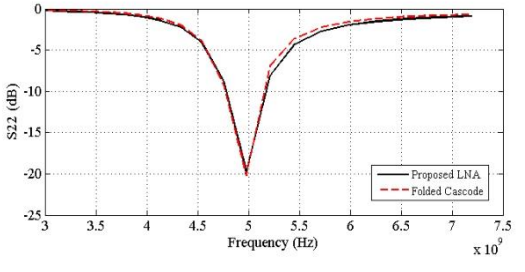
of LNAs and to draw a better comparison between them, various figures of merit are defined and used. To compare the overall performance of amplifiers, we used a FOM which includes the effect of amplifier gain, noise figure, linearity (IIP3), operational frequency (*f*o), and DC power consumption (PDC) as defined by [14].

$$FOM = 10\log_{10}\left(100.\frac{Gain[dB]}{(F-1).[v].P_{DC}[mW]}.\frac{IIP3[mW]}{P_{DC}[mW]}\right) + 10\log_{10}\left(\frac{f_o}{1GHz}\right) \quad (30)$$

The FOM for the presented LNA in this paper is 34.22. Table 3 compares the performances of the proposed LNA with a selection of previously published works.



(a)



(b)

Fig. 11. a. input reflection factor (S11) **b.** output reflection factor (S22) of the proposed LNA (solid lines) and the conventional folded cascode structure LNA (dashed lines).

5. CONCLUSION

In this paper, a low-noise amplifier design with low voltage and power consumption, and improved linearity in 0.18 µm CMOS technology was presented. By adding two auxiliary transistors to the folded cascode structure and using multi-gated configuration and feed-forward methods, it is possible to significantly improve linearity of the circuit without deterioration of other parameters such as gain. It was also demonstrated that besides the improvement in linearity the noise of the circuit was optimized. Simulation results yield an improved circuit linearity of 10dB, equal to 0.0dBm, while consuming only 122 µW more power compared to the conventional folded cascode structure.

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Table 3. Comparison of the performances of the proposed LNA and data included in previously published works.

	Tech.	Fo (GHz)	S21 (dB)	NF (dB)	IIP3 (dBm)	Improvement (dB)	IIP3/PDC	FOM (GHz)	Vdd (v)	PDC (mW)
This work	0.18 µm CMOS	5	9.6	3.24	0	10	0.78	34.22	0.6	1.28
[15]	0.18 µm CMOS	2	12.9	3.4	15	8.2	4.65	31.72	1.8	6.8
[16]	0.13 µm CMOS	0.9	15.4	1.74	4.09	4.94	0.50	24.33	0.6	5.16
[17]	0.13 µm CMOS	2.45	23.75	2.02	-8.5	N/A	0.03	17.80	1.2	4.8
[18]	0.25 µm CMOS	1.8	9.5	3.38	-0.4	N/A	0.18	24.53	0.863	2.16
[19]	0.18 µm CMOS	2.1	16.5	1.97	9.7	12	0.59	23.51	1.8	15.84