

A High-Gain, Low-Noise 3.1–10.6 GHz Ultra-Wideband LNA in a 0.18 μ m CMOS

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ABSTRACT

An ultra-wideband (UWB) common gate-common source (CG-CS) low-noise amplifier (LNA) in a 0.18 μ m CMOS technology is presented in this paper. A capacitive cross-coupling fully differential amplifier with the current-reuse technique is described that in the entire 3.1–10.6 GHz UWB band, achieves a high and flat power gain with low noise and good input impedance matching among low power consumption. The current-reuse technique is used to achieve a wideband and reduce the power consumption. The capacitor cross coupling technique is used to g_m -boosting and hence to improve the NF of the amplifier. Therefore, the dependency between noise figure (NF) and input impedance matching is reduced. The proposed CG-CS amplifier has a fairly low NF compared with the other previous works in similar technology. In addition, a good power gain over all bandwidth and a high isolation with good input/output impedance matching are achieved. The minimum NF is 1.8 dB, the maximum power gain is 14.2 dB, the inverse gain is <-50 dB, and in the entire 3.1–10.6 GHz UWB band, the input and output matching S_{11} and S_{22} are <-10.3 dB and <-11.3 dB, respectively. The input third-order intercept point (IIP3) is -5 dBm. Moreover, the power consumption of the core is 10.1 mW with the supply voltage of 1.8 V.

KEYWORDS: LNA; UWB, CMOS Technology, Current-reuse Technique, Capacitive Cross-coupling Technique, CG-CS Amplifier.

1. INTRODUCTION

As the first stage of a receiver, low-noise amplifiers (LNAs) play a critical role in the overall performance of the system. The use of ultra-wideband (UWB) frequency range (3.1–10.6 GHz) for commercial applications was approved in 2002 by the Federal Communications Commission [1]. The UWB technique provides high data-rate transmission and reduces the power consumption. An UWB LNA must exhibit a flat power gain over the entire UWB bandwidth and have a broadband input matching, a low noise figure (NF), and a high linearity while consuming a little power [2].

In modern wireless products, CMOS technology benefits are low cost, high level of integration, and low power consumption. There are many research works related to UWB LNA design with new structures and design techniques [3], [4]. The distributed amplifier of [4] provides good properties, but the cost is consuming large power. In multistage LNAs, there are multiple DC bias paths, which result in a large total power consumption [5]. A CMOS UWB LNA employing the noise-canceling technique is reported in [6]. However, the gain performance of such a configuration is often less superior [7]. The resistive shunt feedback

amplifiers provide wideband input matching. Nevertheless, resistive feedback amplifiers cannot provide required performance with low power consumption [8].

To realize low power, common gate-common source (CG-CS) and CS-CS current-reuse structures are generally adopted which high gain also can be achieved [9-12]. Compared with the narrowband LNA designs, a severe tradeoff between NF and source impedance matching exists in a wideband LNA. To design a fully differential capacitive cross-coupling CG LNA in [13], a g_m -boosted technique is used and a low NF and high linearity along with a good input matching is achieved. The capacitor cross-coupled CG-LNA reduces the NF and the power consumption by a factor of two [14]. The cross-coupling techniques trade the power consumption and linearity to improve the amplifier noise and gain values. Nevertheless, the circuit needs to use a balun because of its differential input.

In order to do the noise-cancellation, the wideband Balun CS- LNA in [15] converts the single-ended input to differential signal at the output and can also be used as an active balun in the receiver. This amplifier with

active feedback and differential output cancels the nonlinearity of the feedback transistor and hence achieves better linearity in compare to the single-ended amplifier. The proposed method of [16] relaxes the trade-off between linearity and noise performance in LNAs with an active balun.

In this paper, a fully differential CG–CS LNA is proposed for using in UWB receivers. We have combined current–reuse and g_m -boosting techniques. In order to g_m -boosting, the capacitor cross coupling technique is used in this work. As a result, the dependency between NF and input impedance matching is reduced. Moreover, a good power gain over all bandwidth and a high isolation with good input/output impedance matching are achieved. The proposed LNA has a relatively low NF compared with the other LNAs.

In Section 2, the proposed CG-CS LNA is described. First, the CS-CG amplifier with the current-reuse technique is briefly studied. Then, the design concepts such as bandwidth extension, input/output impedance matching, and noise performance are analyzed. In Section 3, the simulation results obtained from the proposed fully differential CG-CS LNA are presented. This paper is concluded in Section 4.

2. PROPOSED CG-CS LNA

2.1. CG–CS with the current–reuse technique

Compared with CS LNA, the CG amplifier offers an appropriate impedance matching in its input. The CG stage is well-known for a wideband input impedance matching of $R_{in}=1/g_m$ where g_m is the transconductance of the transistor. However, the amplifier suffers from poorer noise performance and the minimum available NF in the basic CG LNA of Fig. 1a is $1+(\gamma/\alpha)$ [17]. For CG LNA, NF is approximately independent of frequency and bandwidth [18]. On the other hand, NF in CG is inversely proportional to g_m , however, we have restricted to increase g_m because of obtaining a proper input impedance matching.

The main problem of the CS architecture is the narrowband input impedance matching, which makes it difficult to achieve a broadband input impedance matching in the presence of parasitic capacitors. In [11, 19], some useful techniques are studied applying to the cascode CS topology.

In the LNA design for UWB receivers, the two stage CG-CS topologies are used widely in the literatures [9, 10]. Fig. 1b shows a two-stage CG–CS LNA. The CG, cascaded to CS topology, provides a current-reuse technique. The current-reuse technique reduces the power consumption [10, 11]. Broadband impedance matching is obtained by using CG at the first stage. Furthermore, the current-reuse technique has stagger tuning characteristics and is used to achieve the broadband operation as shown in Fig. 1c. The first

stage resonates at low-frequency f_L , and the second stage resonates at high-frequency f_H . Hence, a flat gain in the wide frequency range can be achieved [11], [12].

2.1.1. Low-band resonant frequency of the first inter-stage f_L

The first stage with parasitic capacitances of the output is shown in Fig. 2a. The low-band resonant frequency, f_L , is determined by the RLC elements, C_1 , C_2 , L_1 , and R_1 . C_{in2} is the total capacitance at the input of M_2 , and C_{dl} is the parasitic capacitance at the drain of M_1 . Neglecting the parasitic capacitances, the output impedance of the first stage can be calculated as:

$$Z_{TL}(s) = \left[\left(Y_2 + \frac{1}{sC_2} \right) \parallel (Y_3 + R_1) \right] + Y_1 \quad (1)$$

Where

$$Y_1 = \frac{sL_1 Z_1}{Z_2}, Y_2 = \frac{sL_1}{g_{m2} Z_2}, Y_3 = \frac{Z_1}{g_{m2} Z_2} \quad (2)$$

And

$$Z_1 = \frac{1}{sC_1} \quad Z_2 = Z_1 + \frac{1}{g_{m2}} + sL_1 \quad (3)$$

g_{m2} is the transconductance of M_2 . The output impedance of the first stage is reduced as follows:

$$Z_{TL}(s) \equiv \frac{N_L(s)}{D_L(s)} \quad (4)$$

$$D_L(s) = K(s)A(s) \quad (5)$$

Where

$$K(s) = s^2 g_{m2} C_1 L_1 + sC_1 + g_{m2} \quad (6)$$

And

$$A(s) = s^3 R_1 C_1 C_2 g_{m2} L_1 + s^2 C_1 [R_1 C_2 + (1 + C_2 g_{m2}) \times (L_1 + L_2)] + sC_2 (R_1 + C_1) + C_2 g_{m2} + 1 \quad (7)$$

The third-order frequency-dependent function of (7) in the denominator of $Z_{TL}(s)$ will not affect the low-band resonant frequency (f_L) because the poles of $Z_{TL}(s)$, determined by $A(s)$, are located at the infinite of the frequency spectrum. The voltage gain of the first stage is calculated as

$$T_L(s) = \frac{v_{d1}}{v_{i1}} = \frac{g_{m1}}{1 + g_{m1} R_s} Z_{TL}(s) \quad (8)$$

Where R_s is the source impedance and g_{m1} is the transconductance of M_1 . Thus, f_L is derived as follows:

$$f_L = \frac{1}{2\pi} \sqrt{\frac{1}{L_1 C_1}} \quad (9)$$

It is seen that the low-band resonant frequency can be determined by adjusting C_1 and L_1 .

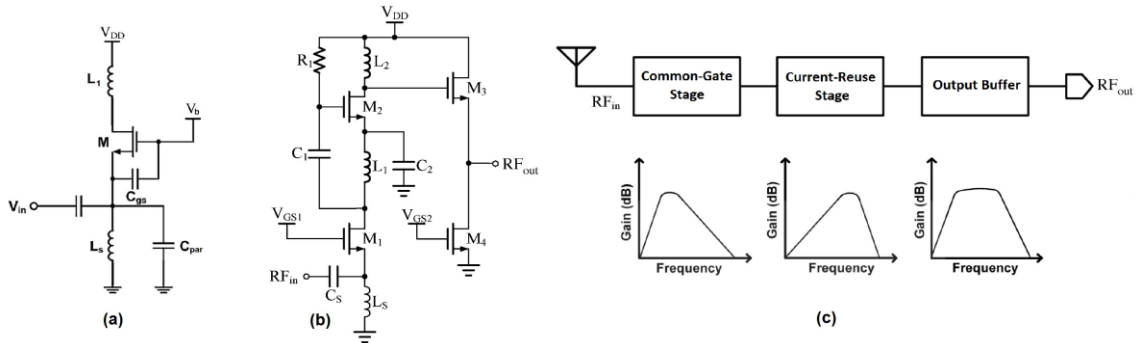


Fig. 1. (a) The basic CG LNA stage (b) The final schematic of the CG-CS amplifier with current-reuse technique and output buffer (c) Illustration of full-band frequency response of the stagger tuning technique

2.1.2. High-band resonant frequency of the second inter-stage f_H

High resonance frequency of the band, f_H , is determined by L_2 and the parasitic capacitance at the drain of M_2 . The schematic of the second stage and its equivalent small signal circuit is shown in Fig. 2b. The high-band resonant frequency, f_H , is derived as follows [9]:

$$f_H = \frac{1}{2\pi} \sqrt{\frac{1}{L_2 C_T}} \quad (10)$$

According to (10), f_H can be tuned by L_2 .

2.2. Noise analysis and g_m -boosting

Although the CG topology provides broadband matching, the NF is not favorable and the noise performance of the CG LNA is strongly dependent on its input matching network. According to the noise analysis, the NF can be given by [9], [13]:

$$F \approx 1 + \left(\frac{g_{d0}\gamma}{g_{m1}} \right) \quad (11)$$

Where γ is the coefficient of the channel thermal noise and g_{d0} is the zero-bias drain conductance. Impedance matching with $g_{m1}R_s=1$ imposes a condition that prevents the increase in g_{m1} to reduce NF. In order to reduce dependency between NF and impedance matching as shown in Fig. 2c, a negative feedback path with an inverting amplification can be inserted between the source and gate terminals to effectively increase the transistor transconductance [13], [14]. The NF now becomes

$$F_{g_m\text{-boosting}} \approx 1 + \frac{g_{d0}\gamma}{G_{m,eff}} \approx 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{(1+A_{neg})} \quad (12)$$

Where $\alpha = g_{m1}/g_{d0}$. It indicates that this technique reduces the channel noise by a factor $(1+A_{neg})$ under input impedance matching conditions. Of course, this

analysis is based on the assumption that amplification stage does not contribute significant noise.

Inverting amplification (A_{neg}) in the g_m -boosting CG LNA can be implemented in various ways. Using passive elements occupies less space and does not add noise to the circuit. Hence, to boost g_m in this work, the capacitive cross-coupling technique is used in the differential CG LNA (Fig. 2d).

By choosing a proper value for C_c , A_{neg} maxes out to 1 [14]. This technique significantly reduces the noise of input transistors and improves the overall NF. Comparing the NF before and after g_m -boosting technique results in:

$$\frac{F_{g_m\text{-boosting}} - 1}{F - 1} = \frac{\frac{\gamma}{\alpha} \cdot \frac{1}{2}}{\frac{\gamma}{\alpha}} = \frac{1}{2} \quad (13)$$

2.3. Input impedance matching

The proposed capacitive cross-coupling differential CG-CS LNA with the current-reuse technique is shown in Fig. 3. The parasitic capacitance (C_{par}) of the source terminal in M_1 (M_5) and L_{S1} (L_{S2}) provide 50 Ω impedance matching. According to Fig. 1a, C_{par} includes the source-body and source-gate capacitance of M_1 (or M_5). Using this figure, the input impedance can be calculated as follows:

$$Z_{in}(s) = \frac{1}{SC_{par}} \parallel SL_S \parallel \left(\frac{1}{G_{m,eff}} \left[1 + \frac{Z_{TL}(s)}{r_{ds1}} \right] \right) \quad (14)$$

Where r_{ds1} is the resistance between drain and source of M_1 and $Z_{TL}(s)$ is the load impedance at the drain of M_1 . In frequencies far from the input resonant frequency, the impedance of $(1/SC_{par}) \parallel SL_S$ is relatively large and can be ignored. Then, the input impedance of (14) reduces to:

$$Z_{in}(s) \approx \left(\frac{1}{G_{m,eff}} \left[1 + \frac{Z_{TL}(s)}{r_{ds1}} \right] \right) \quad (15)$$

Over a wide frequency range in the CG stage, the impedance $Z_{TL}(s)$ is smaller than r_{ds1} . Thus, the input impedance matching of 50Ω can be achieved under

$G_{m,eff} = 2g_m$ and to ensure that $1/2g_m = 50\Omega$ the bias current and the size of the transistors M_1 and M_5 can be adjusted by using less power consumption. The source followers are added as buffers by inserting transistors M_4 and M_8 that are cascaded to the second stage.

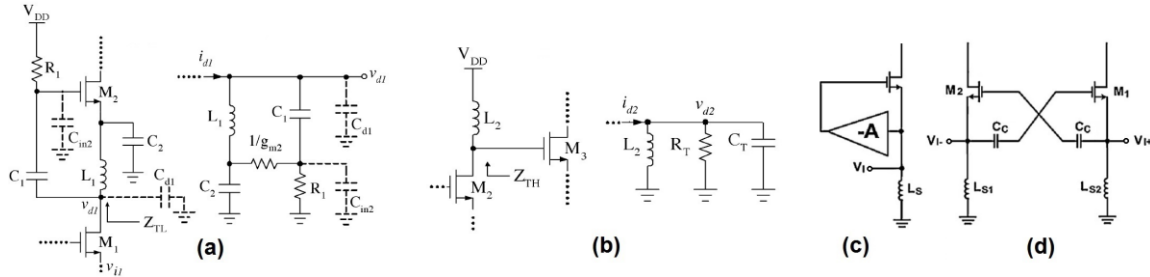


Fig. 2. (a) Schematic of the first stage and its equivalent small signal (b) Schematic of the second stage and its equivalent small signal (c) CG LNA stage with g_m -boosting feedback amplifier (d) Capacitive cross-coupling technique in a differential CG LNA.

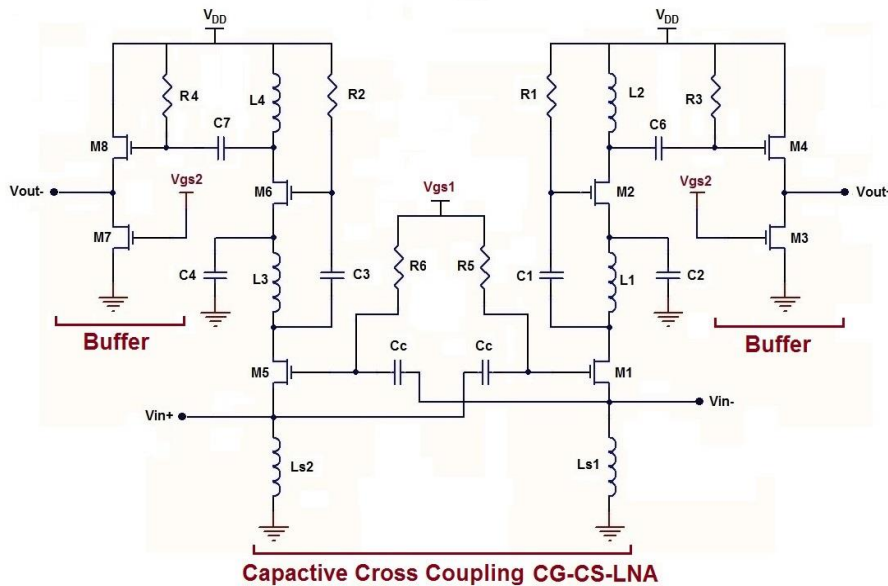


Fig. 3. Schematic of the proposed LNA

3. SIMULATION RESULTS

The proposed fully differential CG–CS amplifier with the current–reuse and g_m -boosting techniques (Fig. 3) is designed and simulated using ADS in TSMC 0.18 μm CMOS RF technology. The amplifier and the output buffers consume 5.6 mA and 5 mA from a 1.8 V DC supply, respectively. Then, the core power consumption is 10.1 mW and the buffer power consumption is 9 mW. As amplifier is fully differential and symmetric, the instance parameters are shown only for one side of the circuit in Table 1. According to Fig. 4, a minimum NF of 1.8 dB is achieved at frequency 5

GHz where the NF is 1.8-3.3 dB in the whole 3.1–10.6 GHz UWB band. The input and output return losses are <-10.3 dB and <-11.3 dB, respectively. Fig. 5 shows a flat small signal gain in the entire 3.1–10.6 GHz UWB band with a maximum gain of 14.2 dB. Over the entire 7.5 GHz bandwidth, the isolation (S_{12}) is <-50 dB. Fig. 6 indicates an input third-order intercept point (IIP3) of -5.0 dBm applying two tones with a 100 MHz spacing at 5.0 GHz RF signals.

In Table 2, we summarized the simulation results of this work. The results are also compared with those of some other reported LNAs using similar technology. It

is seen that the proposed LNA has good performance comparing with the other previous works and it outperforms most of them, especially, in NF and power gain.

4. CONCLUSION

In this paper, a fully differential LNA for UWB application is designed with CG-CS topology. The current-reuse technique is used to achieve a wideband and to reduce the power consumption of the core to 10.1 mW. Moreover, the g_m -boosting technique is employed to improve the NF of the amplifier, 1.8-3.3 dB in the whole 3.1–10.6 GHz UWB band, and this technique is implemented by using the capacitive cross-coupling scheme. Compared with the other previous works in similar technology, the proposed LNA has a lower NF and consumes reasonable power. Furthermore, a flat and high power gain is obtained in this work. Across the UWB frequency band, the power gain of 12.4-14.2 dB is achieved. In addition, over the entire 7.5 GHz bandwidth, the input and output matching, S_{11} and S_{22} , and the isolation, S_{12} , are <-10.3 dB and <-11.3 dB, and <-50 dB, respectively.

Table 1. Summary of the instance parameters

M_1	81/0.18 ($\mu\text{m}/\mu\text{m}$)	C_1	1.6 pF	L_1	9 nH	R_1	5 k Ω
M_2	82/0.18 ($\mu\text{m}/\mu\text{m}$)	C_2	7 pF	L_2	1.2 nH	R_3	5 k Ω
M_3	44/0.18 ($\mu\text{m}/\mu\text{m}$)	C_c	4 Pf	L_{S1}	0.9 nH	R_5	5 k Ω
M_4	114/0.18 ($\mu\text{m}/\mu\text{m}$)	C_6	7 pF	V_{dd}	1.8 V		

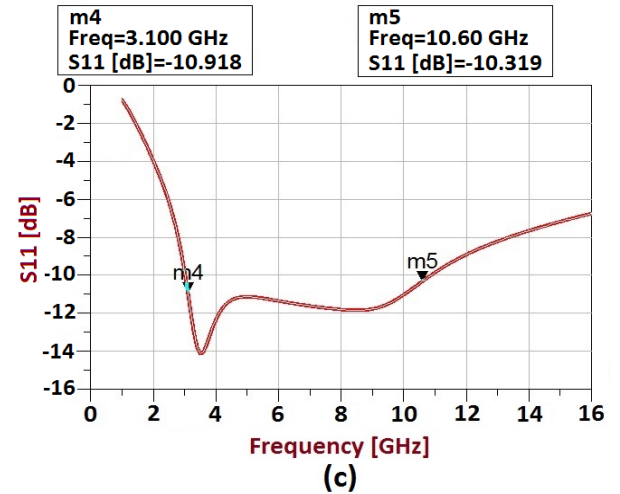
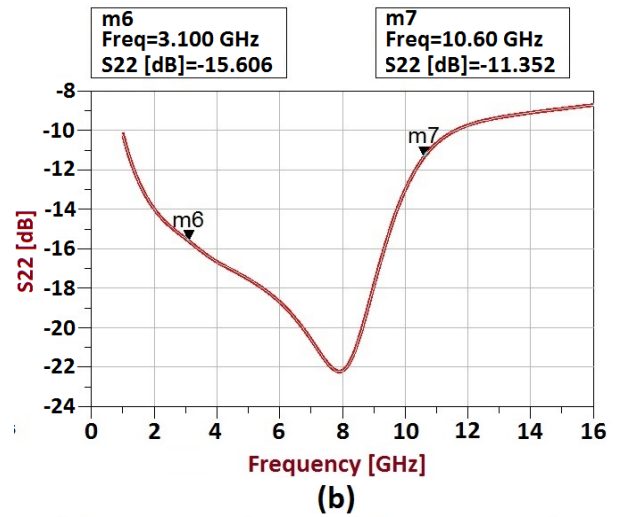
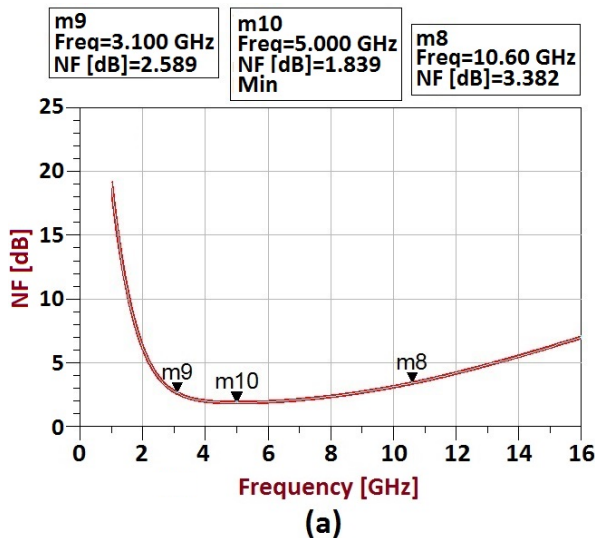


Fig. 4. (a) Simulated results of NF versus frequency (m_9 , m_8 and m_{10} show NFs of 3.1 GHz, 10.6 GHz and minimum NF frequencies, respectively) (b) Simulated results of output return loss versus frequency (m_6 and m_7 for 3.1 GHz and 10.6 GHz) (c) Simulated results of input return loss versus frequency (m_4 and m_5 for 3.1 GHz and 10.6 GHz)



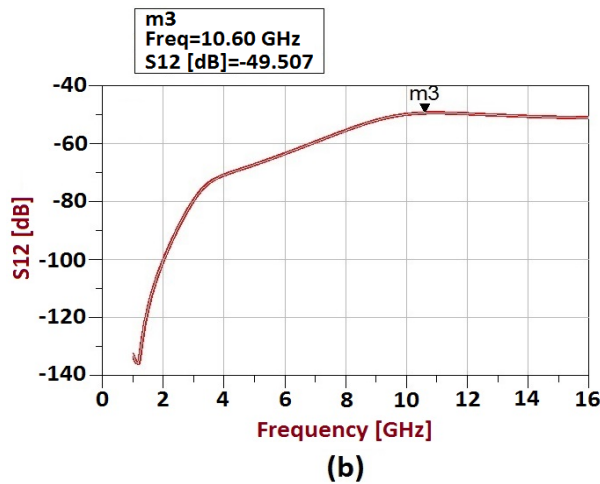


Fig. 5. Simulated results of (a) small-signal power gain (b) inverse gain.



Fig. 6. IIP3 with two input RF signals of 5.0 GHz with 100 MHz frequency spacing

Table 2. Performance summary and comparison

References	Technology	BW [GHz]	Gain [dB]	NF [dB]	S ₁₁ [dB]	IIP ₃ [dBm]	VDD [V]	P _{dc} [mW]	S ₁₂ [dB]
This Work	0.18μm CMOS	3.1 – 10.6	12.4 – 14.2	1.8 – 3.3	< -10.3	-5	1.8	10.1(Core)	< -50
[5]	0.18μm CMOS	3.4 – 11	15 – 15.2	4.3 – 5.5	< -12	-5.3	1.8	30	< -65
[9]	0.18μm CMOS	3.1 – 10.6	12.2 – 13	2.8 – 5.2	< -13.5	-2.23	1.5	4.5(Core)	< -43
[18]	0.18μm CMOS	3.1 – 10.6	5 – 13.2	4.5 – 6.2	< -9.2	-1.4	1.8	23	-
[13]	0.18μm CMOS	2 – 14	9 – 10.3	2.7 – 6.2	< -10	-3	1.5	9	< -60
[11]	0.18μm CMOS	3.1 – 10.6	10 – 11.7	2.9 – 3.6	< -10	-10.4	1.1	10	< -30
[12]	0.18μm CMOS	3.1 – 10.6	10 – 12	2.9 – 5.4	< -10.3	-4.6	1.8	15.2	< -40
[7]	0.13μm CMOS	2 – 9.6	8 – 12	2.8 – 3.5	< -9	-7.2	1.5	19	-
[10]	0.13μm CMOS	2.3 – 9.3	9 – 10.3	3.6 – 6	< -8	-4	1.3	10	< -8

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