An Overview on RAM Memories in QCA Technology

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ABSTRACT
Quantum-dot Cellular Automata (QCA) is a computational technology that can be used to construct nanoscale circuits. Nowadays, this technology is a good alternative for CMOS technology due to features such as high speed, low occupied area and low power consumption. Memory is utilized as one of the basic elements in digital circuit design hence the design and optimization of high-speed RAM memory cells have become one of the most attractive research areas; in the realm of QCA. In this paper, we present a comprehensive investigation on RAM memories. For this purpose, the proposed schemes in terms of functionality, the number of cell consumption, and latency are implemented and compared using QCA Designer software. The results show that some of the proposed schemes show better performance in terms of parameters such as occupied area and delay. Nevertheless, they are still suffering from less stability; hence introducing an optimum scheme is infeasible.

KEYWORDS: Quantum-dot Cellular Automata (QCA), RAM Memory, Nano Circuits, QCA Designer Software**.**

1. INTRODUCTION

In recent years, the quantum cellular automata (QCA) has attracted attentions. The reason behind this is the increasing demand for building computers at the nanoscale. The dimensions of the QCA have an important advantage compared to conventional integrated circuits such as CMOS and even quantum computers. As size of components decreases, efficiency increases commensurately, hence there is a direct relationship between the compression and efficiency. But dimension reduction in CMOS technology will be resulted in efficiency reduction. It is still not clear whether this technology can replace CMOS or not, but the design and modeling show that QCA has many advantages than CMOS. Furthermore, the obstacles for building QCA are being vanished. On the other hand, the simple form of QCA design is very attractive and varied. The QCA topologies and logic circuits share many differences; therefore, new ideas for converting logical units to QCA circuits are required. Circuits that are made under QCA technology are disparate in terms of area and power consumption than CMOS circuits. These unique features of QCA technology are considered as a breakthrough in the field of computer science and logic circuits.

Regarding to novel and attractive features of QCA technology, a massive number of logic circuits have been built, namely, RAM memory cell, which is a major component in the design of logic circuits. In this mechanism, flip-flops are usually used to design a closed loop [3-12]. In this article, all designing methods of RAM memory based on loop structure have been studied and evaluated.

The rest of this paper is organized as follows. In section 2, some backgrounds about QCA are expressed. In section 3, the presented structures for RAM memory in QCA technology are investigated. In section 4, detailed information about implementation is presented. And finally, the conclusion is given in section 5.

2. BACKGROUND

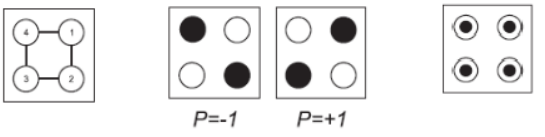
In order to create any digital logic, basic elements including wire, NOT gate, AND gate, OR gate and majority gate are required to implement that logic. In this section, the most common constructor elements of QCA circuits and some laws and rules as well as the design of the clock circuits in this technology are examined and then the traditional structure of RAM memory cells is expressed.

2.1. Overview of the QCA technology

2.1.1. QCA cells

A QCA cell can be built using four quantum dots. These four points are at the corners of a square (Fig.1(a)). Two electrons can switch at this point of their mutual electrostatic repulsion due to try to as far as possible to each other inside cells, and therefore occupy the corners of the square cells. So there can be

only two stable states of the electron states in relation to each other, with minimum energy [3]. These scenarios are shown in Fig. 1(b). One of these states can be called logical zero and another can be named logical one. It should be noted that NULL which is another possible scenarios in QCA is also shown in Fig.1(c). It is mentionable that the electrons can move between points, but there is no possibility of leaving the cell.



(a) (b) (c)

Fig. 1. (a) QCA cell structure (b) Fix QCA cell (c) Null QCA cell

2.1.2. Binary wires and connectors in QCA

Wire is one of the important needed elements for circuit design in QCA. By putting the cells in the standard linear arrangement, wire can be easily manufactured. Two types of wires can be used in QCA. In the first type, all free cells drive to input cells or to the setting cell. So in this type of wire, the information of the driver cells transfer to the end wire (Fig. 2(a)). The second type of QCA wire can be called inverse wire .In this type of wire, cells fall in a diagonal 45-degree together and the value of input cell moves between others cells and each cell reverses to the prior cell (Fig. 2(b)).

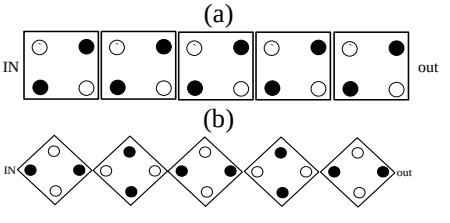


Fig. 2. (a) Normal QCA wire (b) Diagonal QCA wire

In this type of wires, with connecting a 90-degree cell in the middle of the two 45-degree cells, both input signal and its complementary are available. Furthermore, by putting a 90-degree binary wire between two opposite sequence of 45-degree inverter chain, two signals can cross without interfering in one plan [2]. This type of connection structure is shown in Fig. 3.

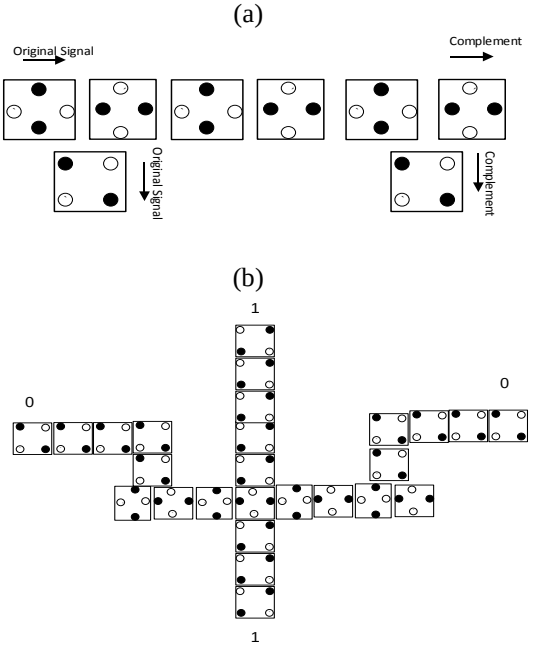


Fig. 3. (a) Inverter Chain, Original and Complement Signal (b) Coplanar Wire Crossing of Two QCA Wires

2.1.3. Base gate in QCA

If two cells skewed together, the second cell can result in reverse of the first cell. This behavior can be used in designing a QCA inverter. Fig. 4(a) shows the structure of a standard QCA inverter, and Fig. 4(b) shows an arrangement of five standard cell gates to implement the majority gate. In this layout, top, left and bottom cells are fixed and the center and right cells are free to respond to constant charge. In a real implementation, these three cells are not fixed, and are driven by the results of previous calculations or input from the other parts of QCA circuit. By using the majority gate and fixing one of its input, AND gate and OR gate can be created. If we set one of the inputs to constant value ‘0’, the output will be equal to the AND of the other two input values (Fig. 5(a)). Also by setting one of the inputs to constant value ‘1’, the output will be equal to the OR of the other two input values (Fig. 5(b)).

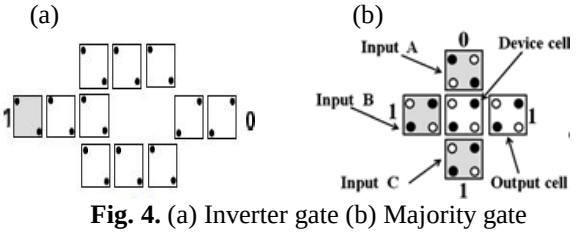


Fig. 4. (a) Inverter gate (b) Majority gate

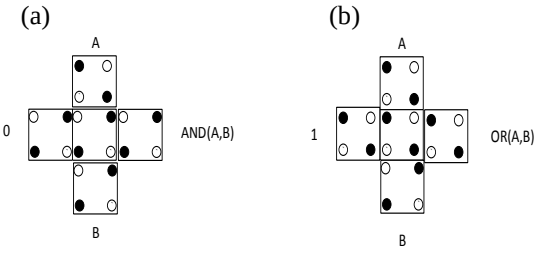


Fig. 5. (a) AND gate (b) OR gate

2.1.4. The concept of Clock in QCA

In QCA circuits, clock controls the movement of electrons within the cell compared to traditional circuits such as electronic factor. In fact how to control clock is that, while information is part of the circuit that they should be combined with other input and generate the desired output, if other inputs later to reach the circuit, clock prevents propagation of information in that section until arriving the other inputs. In fact, clock causes to synchronize different parts of the circuit. Fig. 6 shows the four phases of a clock and its zone:

- **Switch:** In this phase preventing the movement of electrons within the cells begin to rise, and the movement of electrons to be calm.
- **Hold:** In this phase preventing the movement of electrons within cells reaches its maximum extent and location of electrons remains constant.
- **Release:** In this phase deterrent force declines and electrons are released slowly.
- **Relax:** In this phase, no cell and not polarized electrons move freely within the cell.

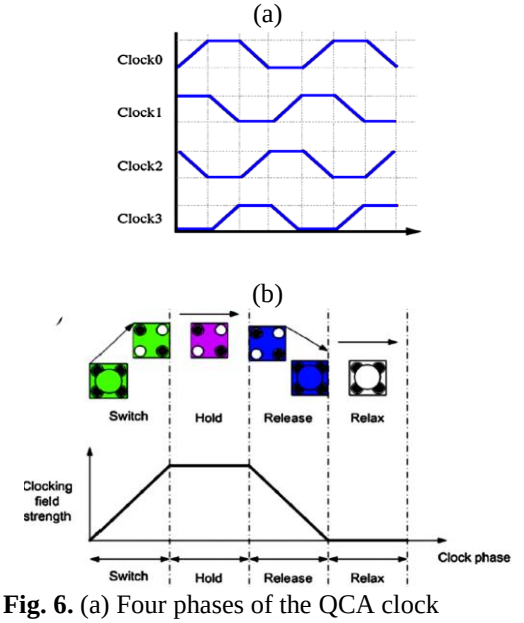


Fig. 6. (a) Four phases of the QCA clock (b) clock zones signal

2.2. RAM memory cell with transistor

RAM memory design is in two forms, static RAM (SRAM) and dynamic (DRAM). Static memory has digital structure for storing and retrieving information from the feedback transistors. Fig. 7(a) shows static RAM memory cell. In this circuit, with adjusting *Wordline(WL)='1'*, the memory content in the forms of direct and inverse exists in the output of NOT gate, and these data can be obtained via *BitLine* and $\overline{BitLine}$. Moreover, *Wordline (WL) ='1',* allows initializing inputs of NOT gates and writing one bit data in the memory [1]. Dynamic RAM memory store and retrieve data using the transistor and capacitor. In Fig. 7(b), a dynamic memory cell with one transistor is shown. The joint line *WORD* is used for reading and writing. In the writing cycle, data value is placed on the *BIT* and the line *WORD* is been *'1'*. Then regarding to the data values on the line *BIT*, charging or discharging of capacitor cells are carried out. Moreover, in the reading cycle, the line *WORD* assumes *'1',* and the stored value in the capacitor is read through the *BIT* line [1].

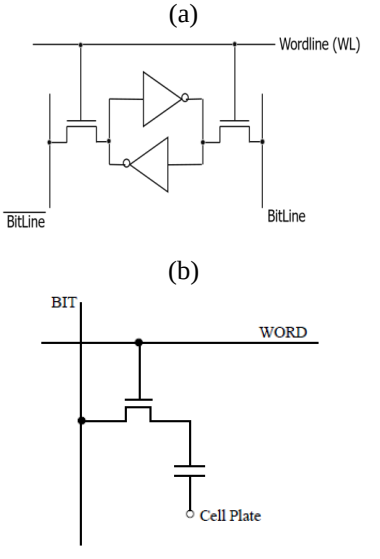


Fig. 7. (a) The SRAM Cell (b) The DRAM Cell

3. SRAM CELLS IN QCA TECHNOLOGY

RAM cell is one of the widely used basic circuits in the design of logic circuits and memory structure. In QCA technology, a loop-based structure is used for the SRAM memory cell design. In this mechanism, storage is implemented via circling a bit of data within a closed-loop of QCA cell. Techniques such as D-Latch [4, 9], SR-Latch [9], multiplexer [11] and majority gate [12] are usually used for cell design. In this study, within the proposed framework of a category, available loop-based RAM memory cells method have been investigated.

3.1. SRAM cell design based on D-Latch

D-Latch is one of the candidates for the design of loop-based structures that are widely used in the design of RAM cells. Walus et al. in 2003, proposed a RAM memory cell using the D-latch [4]. Fig. 8(a) shows the schematic design of its latch. In this structure, the *output* is disabled when the *Enable* value is' 0'. While the *Enable = '0',* the value stored inside the *output* will not change. Also, if the *Enable = '1'*, *Input* value is driven into the loop and *output*. Structure schematic of this presented RAM cell is shown in Fig. 8(b). In this Fig. until the lines *Write / Read =' 1'*, and *Row Select =' 1'*, the value of memory circle is within the loop, which in this case the *input* value can be fed into the output and rotating. And if the *Row Select = '1',* and the *Write / Read = '0* ', the value of circle data can be transferred into the *output*.

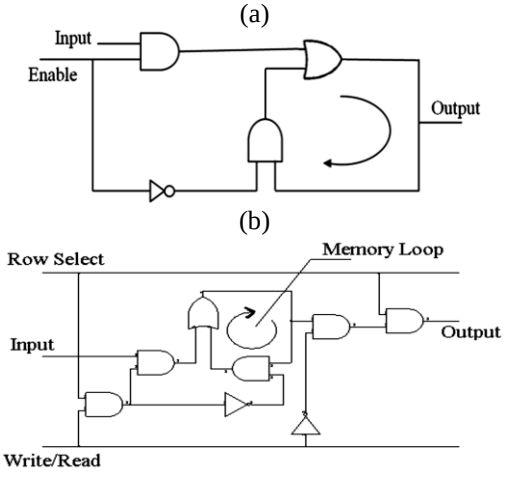


Fig.8. (a) The D-latch circuit diagram in [4]
(b) The Conventional RAM cell based on D-latch in [4]

QCA layout of this cell is shown in Fig. 9. In this scheme, Coplanar wire crossing design method has been used. QCA layout of the cells is not optimal in terms of cell number, consumption area, the number of consumer clock and the beginning to the end delay.

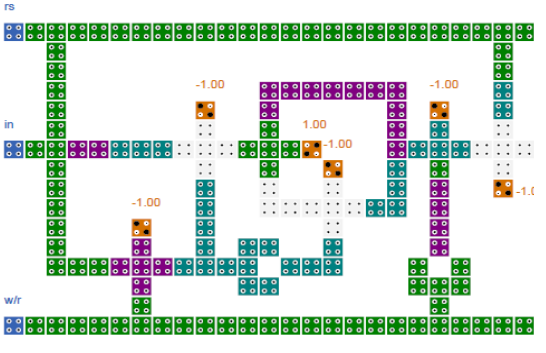


Fig. 9. QCA layout of the presented RAM Cell in[4]

In 2011, Dehkordi et al. proposed another memory cell using D-Latch [9]. The latch schematic structure of this method is shown in Fig. 10(a). In this structure, when *Enable = '0* ', the next state of latch will be equal to the previous state, and When *Enable =' 1',* the next state of latch will be equal to the *input* line. A schematic of proposed RAM cell is shown in Fig. 10(b). In this schematic, when the *write / Read =' 0',* the next state of latch is equal to the current state and output of cell. In this case, the read operation of the cell is performed. And when the *write / Read = '1',* the next state of cells is equal to input and output is zero, and in this case, write operation is performed in the cell. In this structure, three-input majority gate are used to implement AND and OR gates.

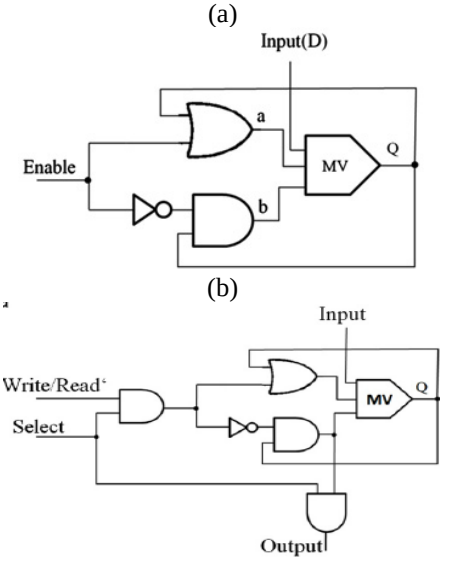


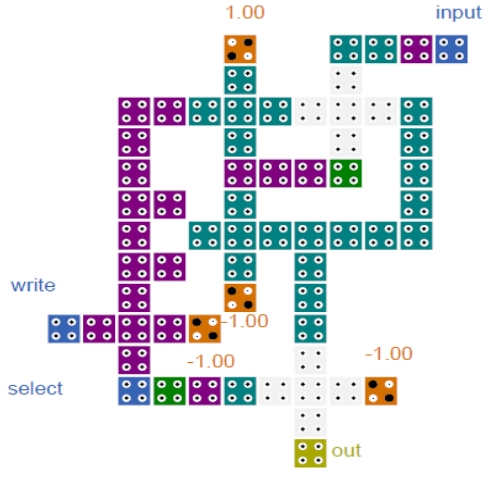
Fig.10. (a) Proposed D-latch structure in[9] (b) proposed RAM cell's circuit diagram based on D-latch in [9]

In this structure two QCA layouts are proposed. The first design is shown in Fig. 11(a) and the second design in Fig. 11(b). The first design is more efficient in terms of the number of consumption cells rather than to the second design and proposed design in [4] but it does not have the appropriate stability in output due to the use of clock phase for a QCA cell .Also the second scheme have problems such as: unstable output result, high number of cells consumption and occupied area, Lack of clock synchronicity in the inputs of the majority gate and sudden changes in the output waveform, due to poor design.

3.2. SRAM cell design based on SR-Latch

Dehkordi et al. in 2011, proposed a RAM cell design with SR-Latch-based structure [9]. Primary schematic of this cell is shown in Fig. 12(a). Each RAM cell in

(a)



(b)

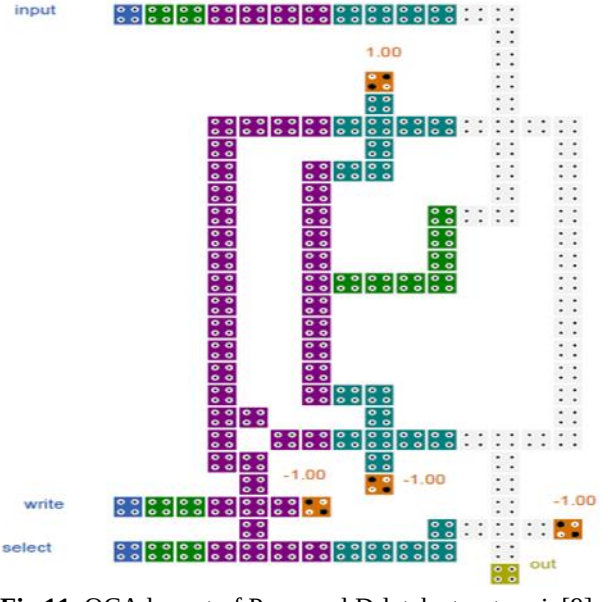
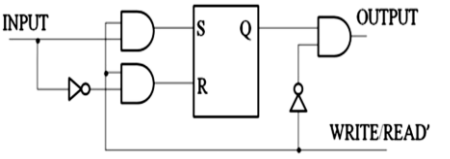


Fig.11. QCA layout of Proposed D-latch structure in[9] (a) QCA layout (b) QCA layout with regular clock zones

This structure has two inputs and one output. If *WRITE* / $\overline{READ}$ = *'1* ', entry path opens onto data and input data is written into the cell, and when *write / Read =' 0* ', output path is opened and the data can be read.

The final structure of the cells are provided by the demorgan rules and implementation of AND and OR gates with three-inputs majority gate (Fig. 12(b)). Author has proposed two QCA layouts for this RAM cell structure. The first layout (Fig. 13(a)), has the design problems same proposed method by D-Latch in [9], such as: applying the clock to only one QCA cell area and instability in output waveform. The second design shown in Fig. 13(b) has the problems such as: much number cells, high occupied area, Lack of clock synchronicity in the inputs of the majority gate, and instability in design.

(a)



(b)

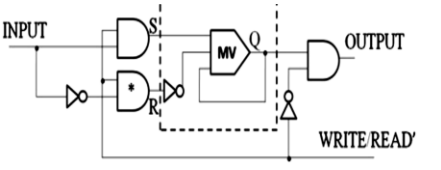
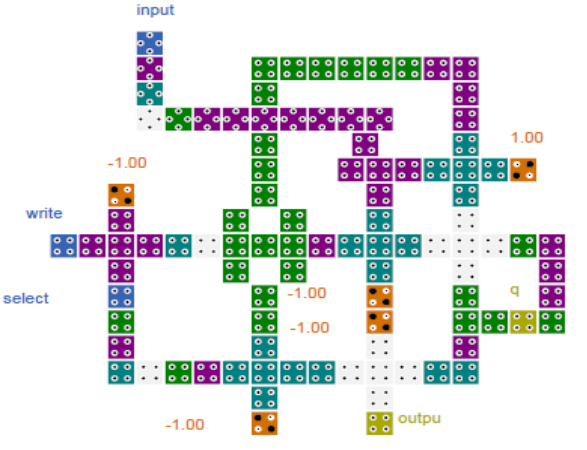


Fig. 12. proposed RAM cell's circuit diagram with SR-Latch (a) First circuit (b) Final circuit

(a)



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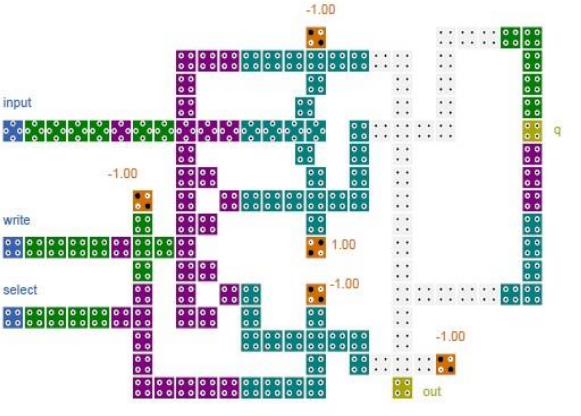


Fig. 13. QCA layout of proposed SR-latch structure in [9] (a) QCA Layout (b) QCA layout with regular clock zones.

3.3. Multiplexer-based RAM cell design

Hashemi et al. in 2012, proposed a RAM cell with Set / Reset ability, using 2 × 1 multiplexer [11]. A Schematic of this multiplexer is shown in Fig. 14(a). In this schematic, if *Select = '0'*, then Output = *'in0'*, and if *Select = '1'*, then *Output = 'in1'*. Also QCA layout of this multiplexer can be seen in Fig. 14(b). In this layout, three-input majority gates are used to design AND and OR gates. This design has good results in terms of output stability against temperature changes. A schematic of this RAM memory cell is shown in Fig. 15(a). In this structure, when *Read / Write =' 0'*, regardless of the *Set / Reset* and *Select* values, *output* value will not change, and in this case, the value of cell can be read, And when *Read / Write = '1'*, and other Set / *Reset* and *Select* inputs are equal to zero, the *output* value is zero, in this mode clear operation of memory cell is done. Also if Read */ Write =' 1'*, *Set / Reset = '1'*, Select =' 0', then *output ='0'*, and Set operation of memory cell is done. Finally, if *Read / Write = '1'*, and *select = '0* ', regardless of the *Set / Reset* input value, new *input* value takes place in *output* and the write operations of cell is done. QCA layout of this RAM memory cell is shown in Fig. 15(b). In our simulations, this layout is more optimal than the memory cells layout by D-Latch and SR-Latch, in terms of number of QCA cells, occupied area and stability in output result.

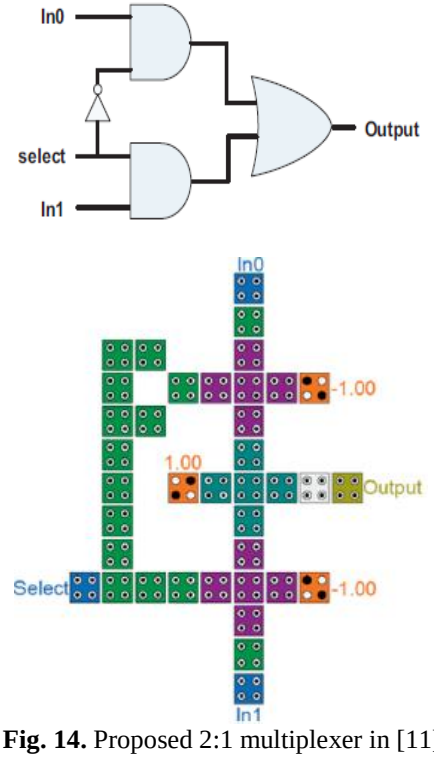
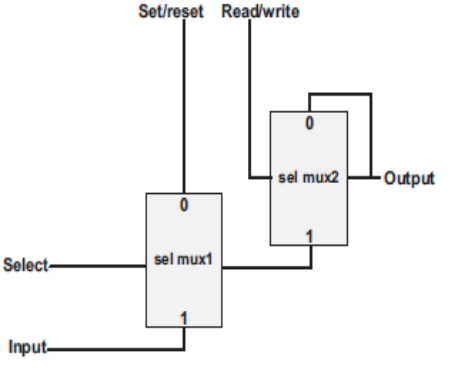


Fig. 14. Proposed 2:1 multiplexer in [11]
(a) Schematic (b) layout

3.4. SRAM cell design based on Majority Gate

In [12], the author proposed a RAM cell with *Se/ Reset* ability and structure based of five and three-input majority gates. The scheme and layout of the five-input majority gate are shown in Fig. 16, and the Table 1 is shown its operation. The schematic circuit of proposed memory cell is shown in Fig. 17. In this schematic, memory cell control by two *Set* and *Reset* inputs. In the normal mode, *Reset = '1', Set = '0* ', and both read and write operations are implemented in this mode, This means that in normal mode for writing in cell, must *Set =' 0', Reset = '1', Select = '0', Read / Write = '1',* also, when the new *input* value can appear in the *output*. And in the normal mode for the read operation must, *Set =' 0', Reset = '1', Select = '1', Read / Write =' 0',* that in this case regardless of the *input* value, new cell *output* remains unchanged, and the data into memory cell is readable. Complete list of desired cell operation is shown in Table 2 and QCA layout of this memory cell is shown in Fig. 18. This layout is optimal in terms of cell number, occupied area and stability in output waveform, this design has features and full functionality of a memory cell.

(a)



(b)

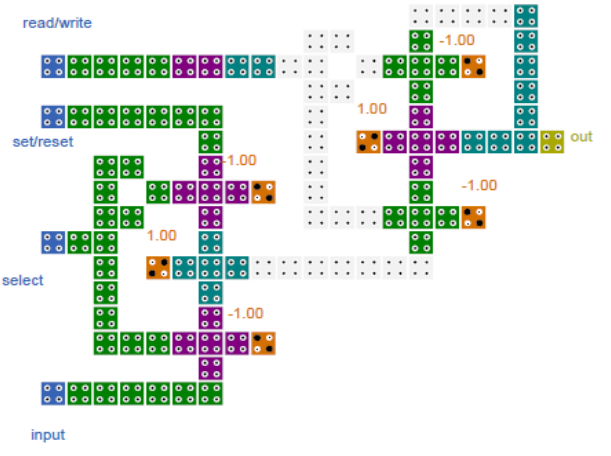


Fig. 15. Proposed RAM Cell In[11]
(a) Schematic (b) QCA layout

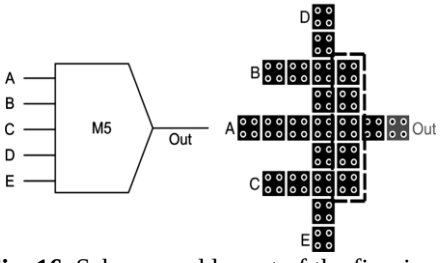


Fig. 16. Scheme and layout of the five-input majority gate

Table 1. True table of five-input majority gate

Sum (A, B, C, D , E)	Maj (A, B, C, D , E)
0	0
1	0
2	0
3	1
4	1
5	1

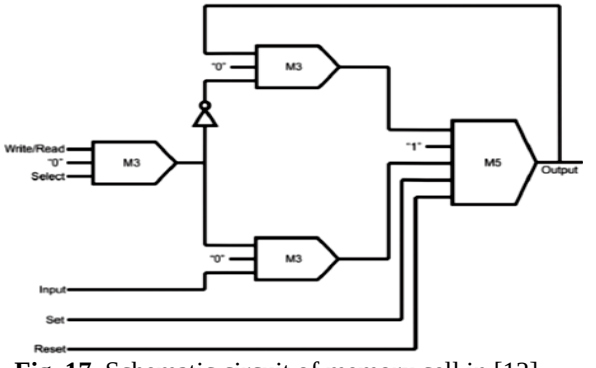


Fig. 17. Schematic circuit of memory cell in [12]

Table 2. Operations list of proposed RAM cell in [12].

Mode of operation	operation	Select	Set	Reset	Write/ read	Input	Previous output	**Output**
Normal	Write	1	0	1	1	1	x	1
	Write	1	0	1	1	0	x	0
Normal	Read	1	0	1	0	x	0	0
	Read	1	0	1	0	x	1	1
Set	Set	x	1	1	x	x	x	1
Reset	Reset	x	0	0	x	x	x	0

4. COMPARISON

This section compares the methods listed in section 3 in terms of: number of used gate, number of QCA cell, area, and number of clock consumption and cell delay. For comparison, all circuits are implemented by QCA Designer software version 2.0.3 with the default parameters and settings and then the results are compared in tables, in terms of usability and distinctive features. Finally, with Analyzing the results, the most optimal and inefficient RAM cell design at each step of comparison has been determined.

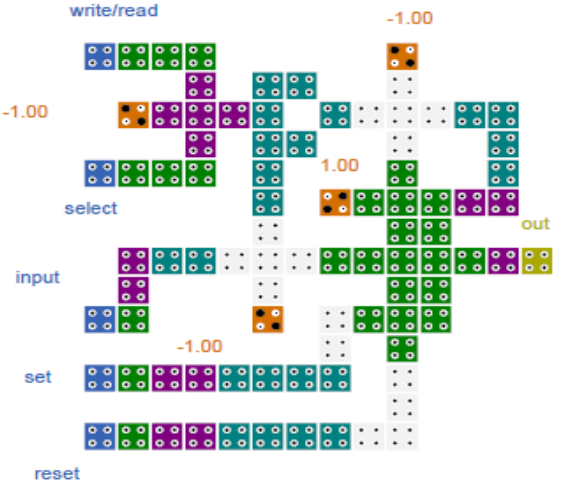


Fig. 18. Proposed QCA layout RAM cell in [12]

4.1. Comparing the number of used gates and the cell Set / Reset Ability

Regarding to this fact that, in all designs, AND and OR gates are implemented by the majority gate; in this section we compare the number and type of used gates and the *set / rest* ability cells. This comparison is shown in Table 3. According to the table, we can see that the proposed method in [12] with the *set / rest* ability, in terms of Number of used gates, has less gate than other methods and would be more efficient. Next, proposed D-Latch design methods [9] without the *set / rest* ability cell, used less gate in compared to the other methods. Finally, proposed methods with D-Latch in [9] and [4] have largest number of used gates.

4.2. Comparing the QCA cell number and occupied area

In this section, irrespective of the type and number of used gates, all methods in terms of the number of QCA cells and area consumption were compared. The result of this comparison is shown in Table 4; According to the table, proposed method based on D-latch design by [9] was the most optimal design in terms of occupied area and the number of memory cells. And next, presented design by [12] is better and more efficiently than other designs. Finally, proposed D-latch design with regular clock zones by [9] was the worst design in term of occupied area. And worst design in term of minimum number of the QCA cell proposed by [4].

4.3. Comparing the number of clock consumption and cell delay

In this section, a comparison is done in term of the number of clock delay from the input up output of memory cells. Results of this comparison can be seen in Table 5. Regarding to the table, design of the Regular Clock Zone presented in [9] with one clock delay, has minimal delay from input up to output of cell and it is the fastest memory cell. And next, the design of the [12] with 1.5 clock delay has better speed and lower latency.

4.4. Comparing the stability against temperature changes

In this section to compare the stability against temperature changes, by QCA designer software and with default values, temperature value has been changed in the range of 0 to 20 Kelvin; In these conditions method, Proposed in [11] generated quite stable output up to 15 Kelvin, and for the temperature value more than 15 kelvin, the reversed output result will be produced. This method has considerable stability than other methods. And next, the method in [12], produces stable output up to 7 Kelvin. Finally, the unstable design proposed in [9] with the smallest temperature changes, achieved unstable output and unique results.

Table 3. Comparison of the number of used gates and the cell Set / Reset Ability

Method	Set / reset Ability	The number and type of used gate
K. Walus[4]	NO	8 Gates= 6 three inputs majority Gates + 2 NOT gates
Dehkordi SR latch[9]	NO	8 Gates= 6 three inputs majority Gates + 2 NOT gates
Dehkordi D latch[9]	NO	6 Gates= 5 three inputs majority Gates + 1 NOT gate
Hashemi [11]	YES	8 Gates= 6 three inputs majority Gates + 2 NOT gates
Angizi[12]	YES	4 Gates= 6 three inputs majority Gates + 2 NOT gates

Table 4. Comparison of the number of QCA cell and occupied area

Memory cell	Number of QCA cells	Area (μm^2)
K. Walus[4]	158	0.16
Dehkordi SR latch[9]	100	0.11
Dehkordi SR latch with regular clock zones[9]	144	0.18
Dehkordi D latch[9]	63	0.07
Dehkordi D latch with regular clock zones[9]	132	0.21
Hashemi[11]	109	0.13
Angizi[12]	88	0.08

Table 5. Comparison of the number of used clock and cell delay

Method	The number of clocks(Latency)
K. Walus[4]	2
Dehkordi SR latch[9]	2
Dehkordi SR latch with regular clock zones[9]	1
Dehkordi D latch[9]	2
Dehkordi D latch with regular clock zones[9]	1
Hashemi[11]	1.75
Angizi[12]	1.5

5. CONCLUSION

In this paper, regarding the importance of memory cells in the design of logic circuits, the methods provided for RAM memory cell design were reviewed, compared and discussed, In general, four main design strategies are used: design-based D -Latch, design-based SR- Latch, design-based multiplexer and design-based majority gate. Majority gate was used in QCA layout of all methods and it is a basic used gate in all designs. All methods were designed by QCA Designer software. Regarding to the result achieved, design by Angizi et al. with the lowest number of majority gates was more efficient than others in terms of gate count. And in terms of occupied area and number of QCA cell, D- Latch-based design presented by Dehkordi et al had the lowest number of cells and area. Of course; it should be noted that this design has been presented without *Set / Reset* ability, and if we want to consider this feature for RAM cells, the proposed design by Angizi et al. with *Set / Reset* ability and less number of QCA cell can be the most efficient cells than other designs in terms of number of cell and occupied area. Finally, in terms of delay and memory cell stability against temperature, regular clock zones design by Dehkordi and colleagues by one clock delay has the least amount of delay; but in terms of stability, these design methods in our experiments have been most unstable. Finally, proposed design method by Hashemi et al. by using 1.75 clock, with high sustainable difference compared to other designs, was the most stable design.

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