A Low-Power CMOS Optical Communication Front-End Using a Three-Stage TIA for 5Gb/s Applications

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ABSTRACT:
In this paper, an optical communication receiver system for 5Gbps applications is proposed concerning power consumption. An inductor-less circuit in three-stages is proposed as the trans-impedance amplifier (TIA), which benefits from the inherent low input resistance of a common gate topology as the first stage. By forming two zeros in this TIA, proper frequency response is obtained while the DC current is reduced. In order to obtain extra gain for the receiver system, three stages of conventional limiting amplifier (LA) are used. In order to verify the circuit performance, the proposed receiver is simulated in HSPICE using 90nm CMOS technology parameters. The receiver is mathematically studied and is matched with the simulations. This paper conducts the simulations, such as eye-diagram, noise analysis and fabrication process analysis (Monte-Carlo). The proposed Trans-Impedance Amplifier shows 53.9dbΩ gain, 3.5GHz bandwidth, 15.2pA/√Hz and only 1.52mw power consumption for 1.2v supply voltage, and the receiver system shows 90.9dbΩ, 3.5GHz bandwidth and 6.34mw power consumption (for 2 stages of TIA and 3 stages of LA) for 1.2v supply voltage. Results indicate that the proposed receiver is suitable to work as a low-power 5Gbps optical communication receiver system.

KEYWORDS: Low Power, Trans-impedance Amplifier, Limiting Amplifier, Optical Receiver.

1. INTRODUCTION

Nowadays, optical communication systems have become more and more important and useful. Optical communications between chips, among PCBs and inside the chips are examples of applications for these systems. It is suitable to use optics for transmitting data, whenever the transmission rate is more than Giga-bits per second.

In receiver systems photons are converted to electrons. The photodiode receives the optical signals and produces current signal proportional to density of the received light. The produced current, of course, may be as weak as a few tens of micro amperes [1]. That is why beside a photodiode, a receiver system consists of a TIA stage and up to 5stges of LAs is used to obtain proper domain and swing for digital blocks, as in figure (1).

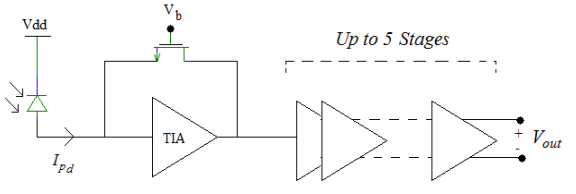


Fig. 1. Block diagram of a typical optical communication receiver

The TIA stage converts and amplifies the input current to voltage, and LA stage provides extra gain. These kinds of receiver systems are implemented in different technologies such as SiGe, BiCMOS, CMOS, GaAs and bipolar [1-3].

Whenever using CMOS technologies, several considered might be noticed. First of all, TIA and LA stages are supposed to operate at high speed applications. Second, the large photodiode parasitic capacitance creates dominant pole at the input node, which needs to be compensated. Third, the output current should be large enough to drive 50Ω load. On the other side, there are several methods to design high speed circuits such as inductive peaking, shunt peaking and series peaking technique [4-6], f_T doubler [1], active feed-back [7], 3D inductor serial peaking [8] and slew boosting [9]. Although the above mentioned methods have some superiors, they may have some disadvantages. For example, using inductors in circuits occupies a large area and f_T-doubler technique doubles the power consumptions in the circuit. In another hand, there are several techniques to reduce the effect of the input capacitance, for instance Regulated cascade (RGC) configuration [10-12,19] and T-coil inductor matching [13]. Regulated cascade configuration has

great effect on enlarging the bandwidth, but it is difficult to implement at a low supply voltage [14]. The T-coil inductor matching technique uses inductor coupling to increase the bandwidth and gain in cost of occupying larger area [15].

In this paper, the focus is on obtaining a low power receiver. Challenges are considered to decrease the power consumption while proper bandwidth and gain can be obtained. This is obtained by forming two zeros in the transfer function of the TIA and at each stage of LAs. Hence, the proper frequency response is obtained by consuming less DC current with less power consumption. Besides that, in order to occupy minimum chip area, the proposed receiver is fully designed with transistors (only one resistance is used) and no inductor is used. The proposed circuit is mathematically studied and several analyses are done in order to prove the proper performance of the proposed receiver and the quality of the output signal.

This paper is organized as follows: In section 2 the proposed TIA is given, mathematically discussed and required simulations are done. In section 3, the LA stage is analyzed. In section 4 the receiver system is discussed and finally, conclusion results are given in section 5.

2. TIA STAGE

2.1. The Proposed TIA

Figure (2) shows the proposed TIA circuit, and figure (3) shows its open loop equivalent circuit. As it can be seen, in order to obtain proper trans-impedance, gain from the TIA stage, 3 stages of amplifiers are connected in series.

M1 and M6 are operating at their saturation region in order to provide proper dc bias current. M2 and M7 complete common gate topology, while M4 completes common source topology. Trans-impedance gain is mostly obtained from this common source structure (M4). Combination of M8 and the resistance provides an active inductive peaking technique (as it is shown in small signal model in figure (3)) which creates a zero in the transfer function at output node, and combination of r_{o3} at the gate of M4 creates another zero at the drain of M4. These active inductors resonate with the capacitances seen at the output node and drain of M4, respectively and move the poles at these nodes to higher frequencies. Therefore, the effect of parasitic and load capacitance decreases, and hence increases the bandwidth of the TIA. Using these combinations at these two nodes, allows us to decrease the DC current, while proper bit-rate is obtained. Accordingly, a low-power TIA structure is achieved.

The dominant pole is formed due to parasitic capacitance of photodiode at input node; and to make it go farther from the origin, the input resistance should be reduced. For this, a common gate stage is used at input node for amplifying the signal. Considering M1 operating as an ideal current source and $r_{O2} \to \infty$, the input resistance of the circuit can approximately be written as follows:

$$R_{in} \approx \frac{1}{g_{m2}+g_{mb2}} \quad (1)$$

In which, g_m represents the trans-conductance. This shows quite a small value for input resistance. So far, poles at each three stage in the TIA are compensated.

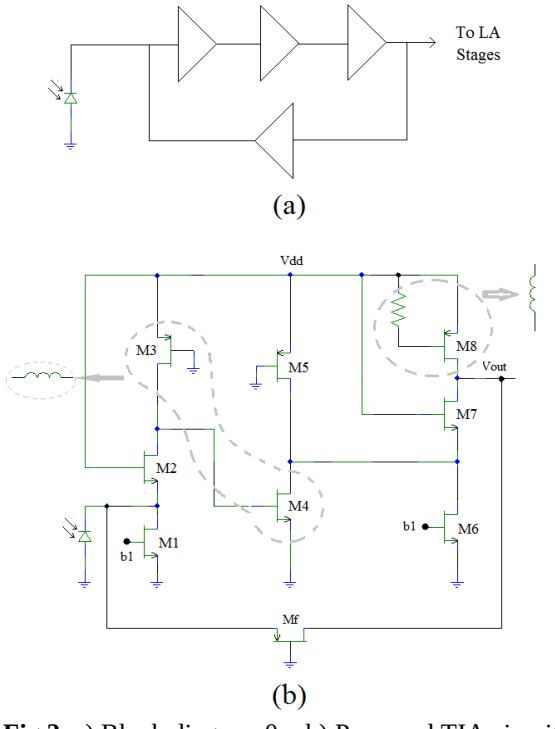


Fig.2. a) Block diagram.0m b) Proposed TIA circuit

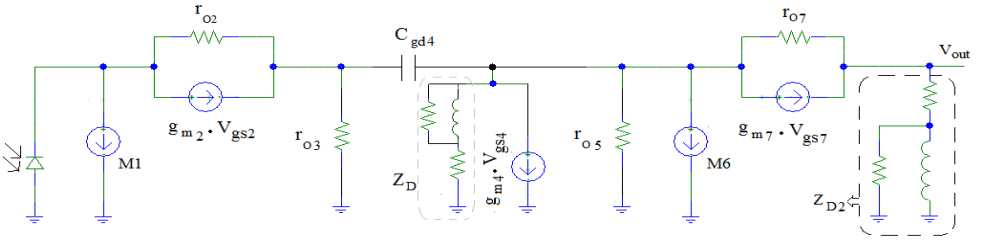


Fig.3. Small signal equivalent circuit of the proposed TIA

So, for the input pole it is possible to write:

$$S_{P,in} = -\frac{g_{m2}+g_{mb2}}{C_{in}} \quad (2)$$

In which C_{in} is as follows:

$$C_{in} = C_{pd} + C_{gd1} + C_{gs2} + C_{sb2} \approx C_{pd} \quad (3)$$

Where C_{pd} is the parasitic capacitance of photodiode, C_{gd} is the gate-drain capacitance, C_{gs} is the gate-source capacitance and C_{sb} is the source-bulk capacitance.

By increasing the trans-conductance of M2, the dominant pole can be moved far away from the origin, and hence proper bandwidth can be obtained. The effect of M2 on input resistance and bandwidth are shown in figure (8) and (9), respectively.

Also, open loop trans-impedance gain of the proposed TIA, which consists of two common gate stages and a common source stage, is as follows:

$$A_V = A_{v,Common\ Gate1} \times A_{v,Common\ Source} \times A_{v,Common\ Gate2}$$

$$A_{v,CommonGate1} = \frac{(g_{m2}+g_{mb2})\times r_{O3}}{(g_{m2}+g_{mb2}+C_{in}.S)\times(r_{03}.C_{out1}.S+1)}$$

$$A_{v,CommonSource} = -g_{m4} \times r_{o5}$$

$$A_{v,CommonGate2} = \frac{(g_{m7}+g_{mb7})\times Z_{D2}}{(g_{m7}+g_{mb7}+C_{in3}.S)\times(Z_{D2}.C_{out}.S+1)} \quad (4)$$

Where, C_{out1} is the capacitance seen at drain of M2, C_{in3} is the capacitance seen at source M7 and C_{out} is the output parasitic capacitance (poles for common source stage are negligible), and we also have:

$$Z_{D2} = \frac{R.C_{gs8}.S+1}{g_{m8}+C_{gs8}.S} \quad (5)$$

Equation (4), proves that by increasing trans-conductance of M2, M4 and M7, more gain can be obtained, it also reveals that proper amount of trans-impedance gain of TIA mostly depends on the quantity of trans-conductance of M4 and r_{O5}.

Effect of trans-conductance of M4 and r_{O5} on trans-impedance gain is shown in figure (10). Equation (5), clearly depicts the effect of active inductive peaking in figure (3) at output node.

Output resistance at low-frequencies can be written as follows:

$$R_{out} = \frac{r_{o7}.r_{o6}.(g_{m7}+g_{mb7})}{g_{m8}.(g_{m7}+g_{mb7})r_{o7}.r_{o6}+1} \approx \frac{1}{g_{m8}} \quad (6)$$

And at high frequencies, it can be written as equation (7):

$$Z_{out} = \frac{C_{gs8}.R.r_{o7}.r_{o6}\,(g_{m7}+g_{mb7}).S + r_{o7}.r_{o6}\,(g_{m7}+g_{mb7})}{C_{gs8}\,(R+r_{o7}.r_{o6}(g_{m7}+g_{mb7})).S+g_{m8}.(g_{m7}+g_{mb7})r_{o7}.r_{o6}+1} \quad (7)$$

So, by considering the above mentioned equations, the output pole can be represents as equation (8):

$$S_{p,out} = -\frac{1}{C_{out}.R_{out}} \quad (8)$$

Where, $C_{out} = C_{dg7}+C_{db7}+C_{dg8}+C_{db8}$ and R_{out} is the output resistance. Also, by knowing the fact that the dominant pole is formed at input node$\left(C_{in} \gg C_{out} \rightarrow S_{p,in} \ll S_{p,out}\right)$, f_{-3db} can approximately be written as equation (9):

$$f_{-3db} \approx \frac{g_{m2}+g_{mb2}}{2\pi.C_{in}} \quad (9)$$

It is clearly revealed that by increasing the trans-conductance of M2 (g_{m2}), as it is depicted in next section, the input impedance is lessened, and the bandwidth is enlarged.

3. SIMULATION RESULTS

In order to verify the circuit performance, the proposed TIA is simulated in HSPICE using 90nm CMOS technology parameters. Figure (4) shows the frequency response and phase of the proposed TIA. As it can be seen in figure (4), the proposed TIA shows 53.9dBΩ trans-impedance gain, 3.5GHz bandwidth and a proper phase margin. Also, power dissipation for this circuit is 1.52mw for 1.2v supply voltage.

As it was important to study the input resistance and its effect on bandwidth, figure (5) shows the simulated input resistance and input impedance according to frequency variation. As it can be seen, input resistance at -3db frequency is less than 90Ω, and the input impedance at -3db frequency is less than 190Ω. This low range of resistance and impedance is due to the use of feedback network and also common gate topology at input node.

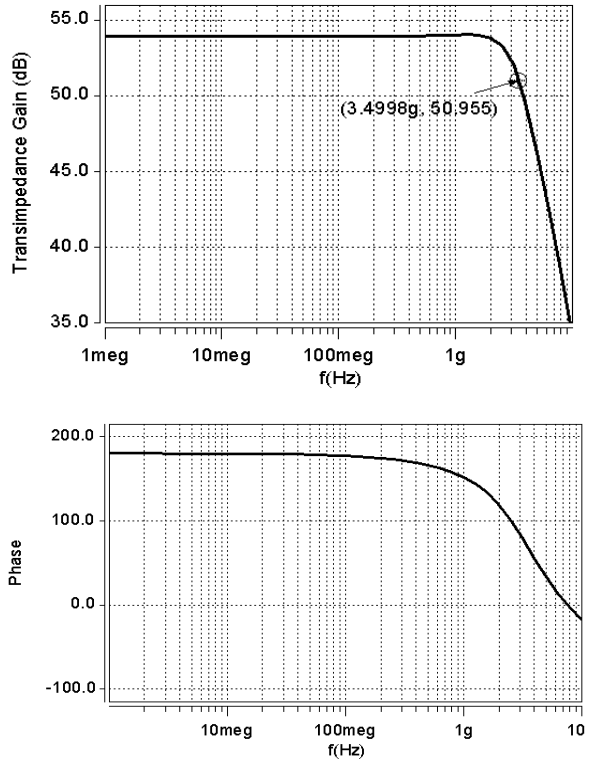


Fig. 4. (a) Frequency response (b) Phase of the proposed TIA.

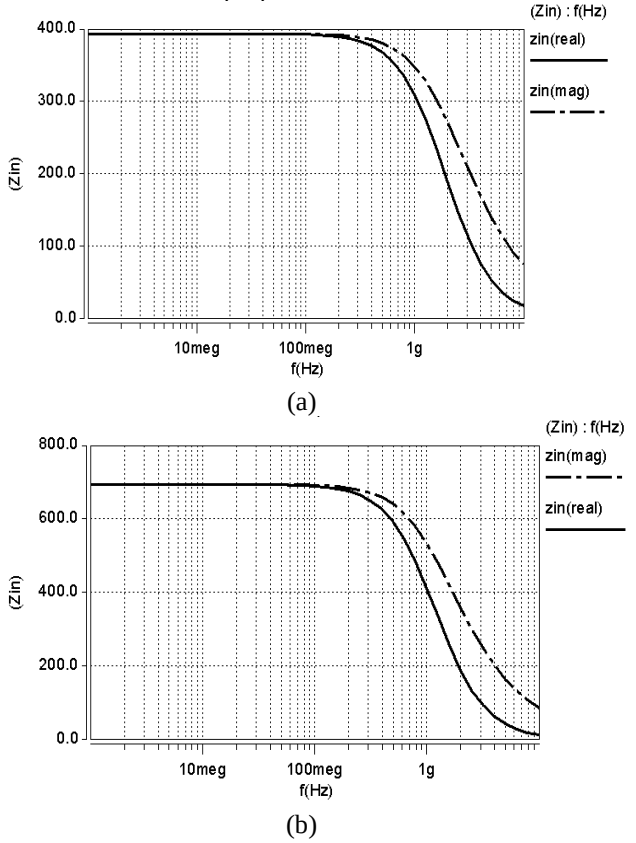


Fig. 5. Input impedance and input resistance (a) with feedback (b) without feedback network.

In order to study the impact of noise and inter-symbol interference (ISI) and the output signal quality of the proposed TIA, figure (6) shows the simulated eye-diagram of the proposed circuit for 100µA 5Gbps NRZ PRBS7. The vertical large opening of the eye in figure (6) reveals the low range of bit error rate (BER), and horizontal opening relates the jitter and the sensitivity. Generally, it can be said that wider the opening of the eye, the larger the bandwidth. The eye is opened to about 60mv for an input current of 100µA.

Also, in order to analyze the proposed TIA at fabrication process, Monte-Carlo analysis is done in HSPICE for 200 runs. Figure (7) shows the Monte-Carlo analysis of the proposed TIA. As it can be seen, trans-impedance variation in the fabrication process can be from 53dB up to 54.8dB.

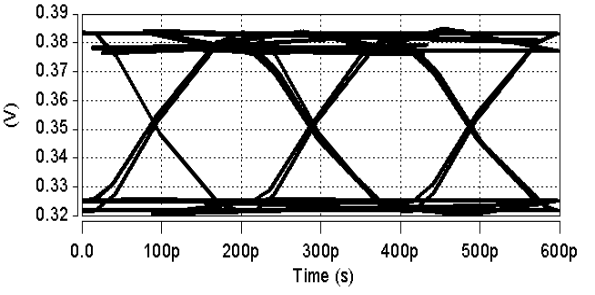


Fig. 6. Simulated Eye-Diagram of the Proposed TIA for 100µA 5Gbps NRZ PRBS7

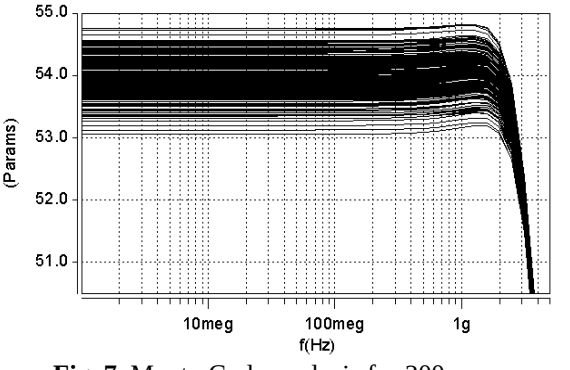


Fig. 7. Monte-Carlo analysis for 200 runs

In following, effect of width of M2 on input resistance according to equation (1) is analyzed and is shown in figure (8). Also effect of width of M2 on -3dB frequency is analyzed according to equation (9). Moreover, the effect of M4 and M5 width on gain of the TIA according to equation (4) is shown in table III, table IV and figure (10).

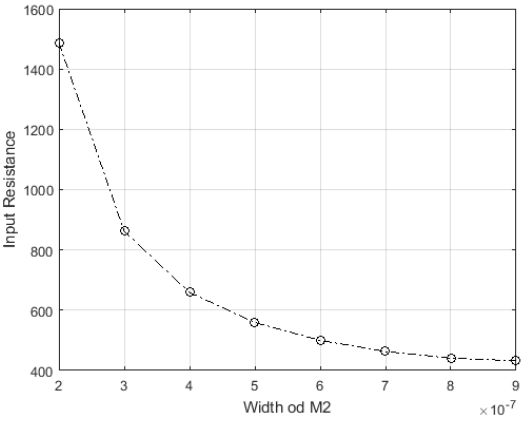


Fig. 8. Width of M2 vs. input resistance

Table 1. Effect of width of M2 on input resistance according to equation (1)

`	200nm	300nm	400nm	500nm	600nm	700nm	800nm	900nm
R_{in}	1487Ω	862Ω	659Ω	559Ω	500Ω	463Ω	441Ω	432Ω

Table 2. Effect of width of M2 on -3dB frequency according to equation (9)

W2	100nm	20nm	300nm	400nm	500nm	600nm
f_{-3dB}	223Meg.Hz	577Meg.Hz	1.01GHz	1.35GHz	1.85GHz	3.46GHz

Table 3. Effect of width of M4 on Trans-impedance gain according to equation (4)

W4	2.5µm	3µm	3.5µm	4µm	4.5µm	5µm	5.5µm	6µm	7µm	8µm
Gain	150Ω	192Ω	204Ω	211Ω	226Ω	251Ω	283Ω	320Ω	409Ω	516Ω

Table 4. Effect of width of M5 on Trans-impedance gain according to equation (4)

W5	2.5µm	3µm	3.5µm	4µm	4.5µm	5µm	5.5µm	6µm	7µm	8µm
Gain	664Ω	516Ω	430Ω	375Ω	339Ω	316Ω	301Ω	292Ω	284Ω	275Ω

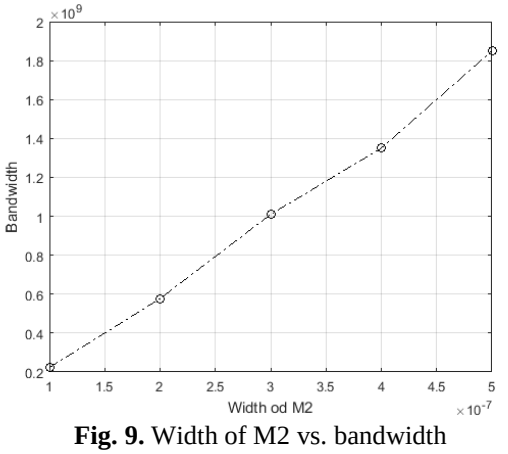


Fig. 9. Width of M2 vs. bandwidth

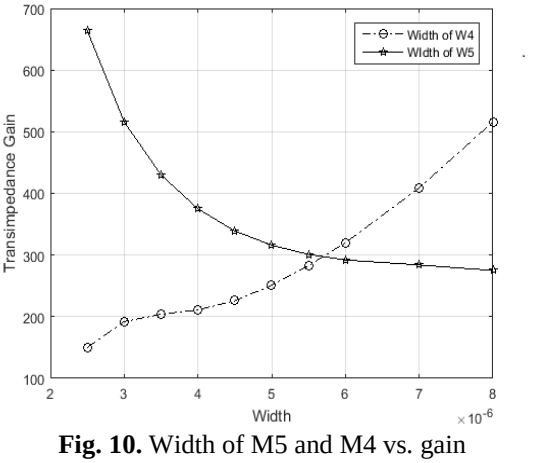


Fig. 10. Width of M5 and M4 vs. gain

4. NOISE ANALYSIS

Although thermal noise of the TIA stage can be reduced by common mode rejection parameter in LA stages, it is instructive to study the thermal noise of the proposed TIA.

Representing the thermal noise of each transistor by current source, figure (11) shows the equivalent thermal noise of the proposed TIA.

At the first stage of the TIA in the common gate structure, all $\overline{I_{n,M1}^2}$ flows through M_3 and no part of $\overline{I_{n,M2}^2}$ flows through M3 [1]. So, M2 actually produces no thermal noise in the circuit. The thermal noise of the first stage (common gate stage) at drain of M2 is according to equation (10):

$$\overline{V_{n,1st\ stage}^2} = \left(\overline{I_{n,M1}^2} + \overline{I_{n,M3}^2}\right) \times r_{o3}^2 \qquad (10)$$

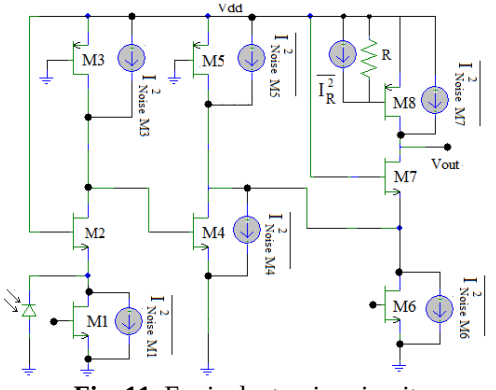


Fig. 11. Equivalent noise circuit

Dividing this quantity by the trans-impedance gain of A_{V1} yields the input referred noise of the first stage, which is equal to equation (11):

$$\overline{I_{n,1st\ stage}^2} = \overline{I_{n,M1}^2} + \overline{I_{n,M3}^2} \qquad (11)$$

Equation (11), suggests that the noise current of M1 and M3 are referred to the input node with a unity factor.

For the second stage, that is the common source stage, representing noise of M4 and M5 by the current sources in figure (8), the thermal noise at drain of M4 can be written as equation (12):

$$\overline{V_{n,2nd\ stage}^2} = 4KT\gamma(g_{m4} + g_{m5}) \times (r_{O4} \| r_{o5})^2 \qquad (12)$$

In which K is the Boltzmann constant and T is temperature. Dividing equation (12) by gain of first and second stage, the input referred noise of this stage can be as equation (13):

$$\overline{I_{in,2nd\ stage}^2} = \frac{\overline{V_{n,2nd\ stage}^2}}{[g_{m4} \cdot (r_{O4} \| r_{o5})]^2} \times \frac{1}{\overline{A_{V,1st\ stage}^2}}$$

$$= 4KT\gamma \cdot \left(\frac{1}{g_{m4}} + \frac{g_{m5}}{g_{m4}^2}\right) \times \frac{1}{\overline{A_{V,1st\ stage}^2}} \qquad (13)$$

In which γ is the coefficient factor.

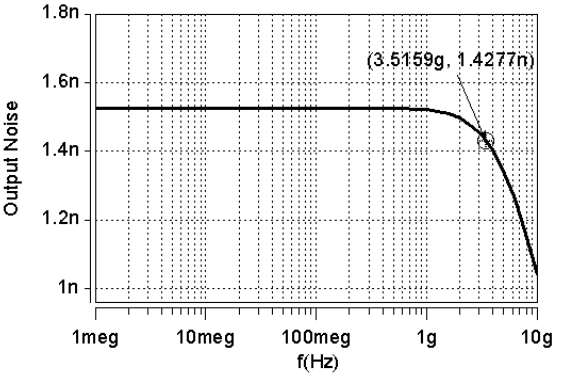
For the third stage, similar to the first stage, all $\overline{I_{n,M6}^2}$ flows through Z_{D2} and no part of $\overline{I_{n,M7}^2}$ flows through Z_{D2}. By considering this at the output node we have equation (14):

$$\overline{V_{n,3rd\ stage}^2} = \left(\overline{I_{n,M6}^2} + \overline{I_{n,ZD2}^2}\right) \times Z_{D2}^2 \qquad (14)$$

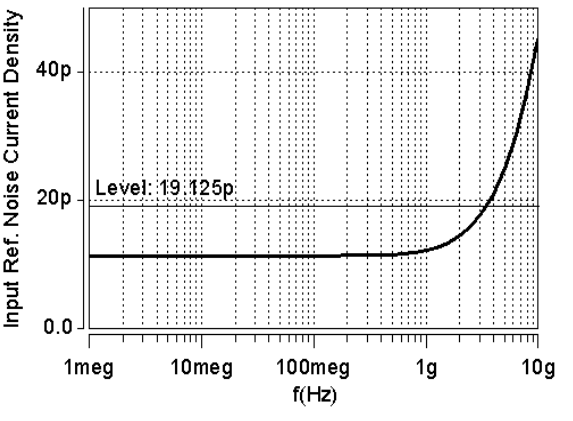
And the input referred noise of this stage can be written as equation (15):

$$\overline{I_{in,3rd\ stage}^2} = \frac{\overline{I_{n,M6}^2} + \overline{I_{n,ZD2}^2}}{\left(A_{V,1st\ stage} + A_{V,2nd\ stage}\right)^2} \qquad (15)$$

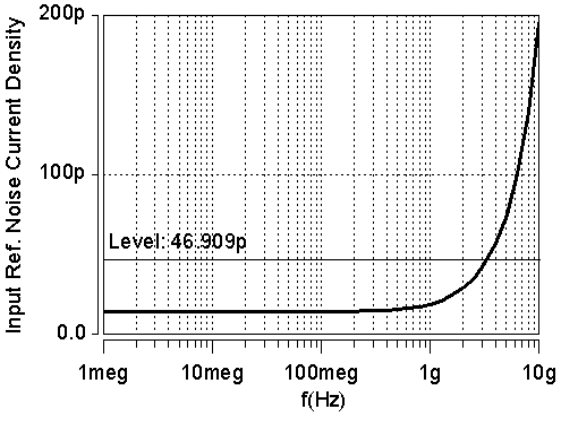
In order to verify the noise behavior of the proposed TIA, noise analysis is done in HSPICE. Figure (12) shows the simulated output and input referred noise of the proposed TIA, respectively. As it can be seen, the feedback network has reduced the input referred thermal noise at f_{-3dB} from 46.9p to 19.1p.



(a)



(b)



(c)

Fig. 12. (a) Output noise (b) Input referred noise of the proposed TIA. (c) Input referred noise of the TIA without feedback system.

5. LA STAGE

In order to achieve a proper gain for the receiver system, three stages of a conventional limiting amplifier (LA) is used in this work. Figure (13-a) shows the LA stage building block and figure (13-b) shows the structure of each cell gain.

As shown in figure (13), three differential stages are used as LA stages, with active inductive peaking technique as their loads. The equivalent circuit is shown in figure (14). By using half circuit, gain of each stage can be calculated as equation (16):

$$A_V = g_{m101} \times Z_{out,LA} \qquad (16)$$

In which, the output impedance of each stage can approximately be as equation (17):

$$Z_{out,LA} = \frac{r_{o104}.C_{gs103}.S+1}{g_{m103}+C_{gs103}.S} \qquad (17)$$

On the other hand, cascading three stages of amplifiers results in lowering the bandwidth. In order to analyze this effect, the transfer function of the LA stage is assumed as; $A_v = \frac{A_{V0}.W_n^2}{S^2+2\xi W_n.S+W_n^2}$, Where, ξ is the corresponding damping factor, the -3db frequency for each cell gain can be written as equation (18) [18]:

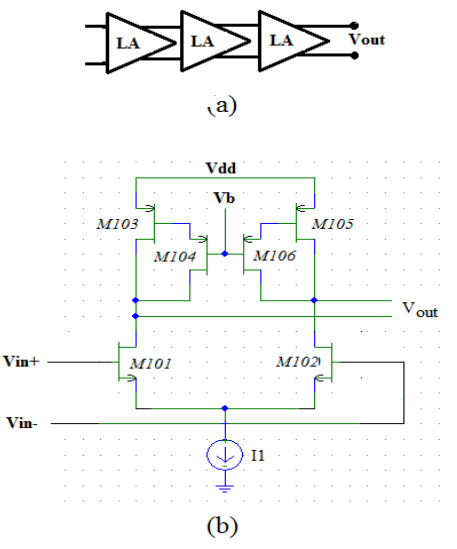


Fig. 13. (a) Block diagram of the Limiting Amplifier (b) Structure of each cell gain

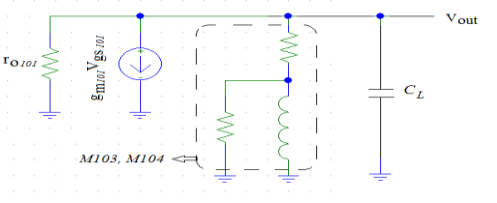


Fig. 14. Equivalent circuit of each cell gain of LA stage

$$w_s = \left[1 - 2\xi^2 + \sqrt{(1-2\xi^2)^2+1}\right]^{\frac{1}{2}} \times w_n \qquad (18)$$

Thus, for a three stage amplifier -3db frequency can be written as follows [8]:

$$w_C = \left[1 - 2\xi^2 + \sqrt{(1-2\xi^2)^2 - \left(1-2^{\frac{1}{2}}\right)}\right]^{\frac{1}{3}} \times w_n \qquad (19)$$

In which, to obtain a flat response, ξ is considered to be equal to $\sqrt{2}/2$.

6. RECEIVER SYSTEM

Block diagram of the simulated receiver system is shown in figure (15). Two TIA stages are used one for amplifying the main signal plus noise and the other for amplifying the noise. Therefore, the noise of TIA stage can be decreased due to common mode rejection in differential LA stages.

Figure (16) shows the frequency response of the receiver system with the gain of 90.9dbΩ and bandwidth of 3.5GHz. Also power dissipation for two stages of TIA and three stages of LA is 6.64mw for 1.2v supply voltage.

Finally, table V compares the proposed TIA with other reported ones and table VI reports the proposed

receiver system. As it can be considered, the proposed TIA has some priorities.

In table V, the figure of merit is defined as equation (20):

$$FOM = \frac{Gain(\Omega)\times Bandwidth(GHz)\times C_{in}(pF)}{Power\ Consumption(mW)\times Input\ referred\ Noise(\frac{pA}{\sqrt{Hz}})} \quad (20)$$

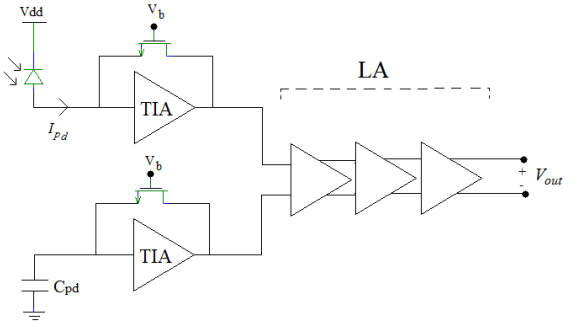


Fig. 15. Block diagram of the proposed optical receiver

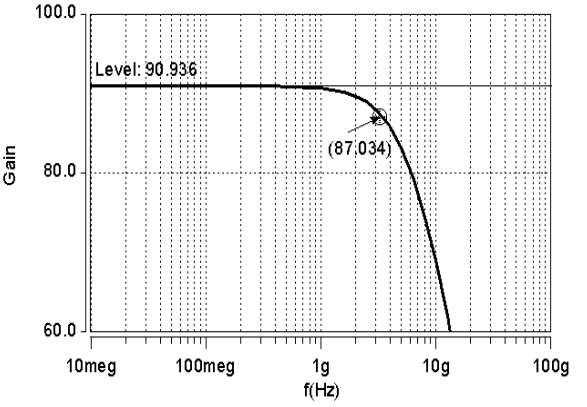


Fig. 16. Frequency response of the optical receiver system

Table 5. Comparison of the proposed TIA with other works

Ref.	[4]	[5]	[6]	[11]	This work
Tech.	65nm CMOS	0.13µm CMOS	40nm CMOS	0.18µm CMOS	90nm CMOS
Supply Voltage	1/1.8v	1.5v	1.3v	1.8v	1.2v
Power Consumption	93mw	68.6mw	103mw/ch	18.6mw	1.52mw
Gain	83dbΩ*	600kΩ*	64dbΩ	55dbΩ	53.9dbΩ
Bandwidth	20.5	-	14.5GHz	7GHz	3.5GHz
Speed	25Gbps	5Gbps	4×25Gbps	10Gbps	5Gbps
Input referred noise	1.8µArms	-	22.4pA/√Hz	17.5pA/√Hz	15.26pA/√Hz
Input capacitance	160fF	1pF	100fF	0.2pF	160fF
FOM	-**	-	1.02	2.5	11.73
Year	2014	2014	2014	2010	2017

*whole receiver (TIA+LA) **Gain of the TIA is not specified

Table.6. Properties of the proposed optical receiver

	TIA	LA
Gain	53.9dBΩ	37dB
Bandwidth	3.5GHz	3.9GHz
Power Consumption	1.52mW	3.6mW
Supply Voltage	1.2v	1.2v
Input referred noise	$15.26pA/\sqrt{Hz}$	-
Input capacitance	0.16pF	-
Output capacitance	-	100fF

7. CONCLUSION

In this paper, a 5Gb/s low power optical communication receiver system is proposed. A new TIA structure is proposed and discussed mathematically. In order to verify the proper performance and proper output signal of the circuit, required simulations are done. Three stages of differential LAs are added to the TIA and hence low-power receiver is obtained. The TIA stage shows 53.9dbΩ trans-impedance gain, 3.5GHz bandwidth, 963nA$_{rms}$ input referred noise and only 1.52mw power dissipation for 1.2v. The whole receiver system (2 stages of TIA and 3 stages of LA) shows 90dbΩ gain, 3.5GHz bandwidth, 6.64mw power dissipation for 1.2

supply voltages. Finally, the results indicate that the proposed receiver system is suitable to work as low power 5Gb/s optical communication receiver.

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