Simulation of the Process of LDMOS Transistor Manufacture and Optimizing it to Increase the Current of Work

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ABSTRACT:
This paper presents the simulation of the process of LDMOS transistor manufacturing by using Silvaco software and by relying on the ability of calculating the basic parameters of transistor dependencies, focusing on the optimization of the manufacturing process in order to increase the current of work. By using this simulation and reviewing each parameter, we can achieve the optimized manufacturing process by focusing each basic parameter and by paying attention to its required application. In order to design, we first define the construction procedures and the necessary processes using the Athena simulator, and then we use the Atlas device simulator to acquire electrical parameters. Simulation results show that by selecting the optimal parameters of the manufacturing process such as gate oxide thickness, channel length, and doping in channel, we can increase current of the LDMOS transistor.

KEYWORDS: LDMOS transistor, Current operating point, Threshold voltage, Cut-off frequency, Trans conductance, Breakdown voltage.

1. INTRODUCTION

The application of high power radio frequencies is growing respectively due to demands for wireless equipment market. Transistors with metal oxide semiconductor field effect (MOSFET) have been used in high power radio frequency systems due to their high-speed switching [1], [2]. This type of transistors also has a wide range of maximum voltage rating between 10 to 1500V for power application. Voltages rating less than 30V are usually used for power switches in portable electronic equipment including laptops, personal computers and etc. voltage ranges between 30 to 100 volts are used in the industry and car manufacturing. Voltages higher than 100V are generally used to control motors, power devices, and communications. In the past decade the laterally diffused metal oxide semiconductor (LDMOS) transistor has baeen the dominating technology for use in the RF-power amplifiers. We require a short channel length and low impurity level in drain area for power applications [3]. Having low impurity level guarantees the spread of channel into the area in drain association [4-8]. Current depends on different parameters such as gate oxide thickness, threshold voltage, width and length of channel, and channel voltage [9]. Threshold voltage also depends on the gate oxide thickness, and the surface concentration of the channel. Therefore, by changing the thickness of the oxide, implanting channel, and adjusting channel length in simulation process, we can increase current without causing change in other default parameters [10-14]. The breakdown voltage of the device depends on the thickness and resistance of epitaxy layer, the shape of the junction, and structure of the area in which junction reaches to the semiconductor surface [15]. It is predicted that by increasing the thickness of epitaxy layer and resistance of epitaxy layer, breakdown voltage will increase [16], [17]. Several methods to improve the breakdown voltage, on-resistance, and high-frequency operation of the LDMOS transistor have already been developed [18-20]. However, this work focuses on the optimization of manufacturing process in order to increase the current of LDMOS transistor. The simulation of manufacturing process of this type of transistor which is a base for its real manufacturing is of the utmost importance.

In this paper, we describe physical structure and manufacturing processes of LDMOS transistor. We determine parameters that affect the device current of work. Also, optimizing the current of the transistor by changing the thickness of oxide, thickness of the

epitaxy layer, channel length, and impurity concentration of the channel is investigated using the Silvaco device simulator. Furthermore, the threshold voltage, breakdown voltage, transconductance, and cut-off frequency of the optimized device are calculated.

2. LDMOS TRANSISTOR STRUCTURE

The function of the metal oxide semiconductor field effect transistor (MOSFET) was first proposed in a patent application filed in 1928 by J. E. Lilienfeld [21]. In 1960, processing had improved and the first silicon MOSFET was designed and fabricated [22]. Just a few years later in 1963, complementary MOS (CMOS) was presented laying the foundation for the coming integrated CMOS circuit [23]. The CMOS technology is easily scaled to improve performance but this also implies lower supply voltages. For high-voltage MOS transistor, the channel region is separated from the voltage supporting part and thus higher breakdown voltages are achieved. There are several different types of high-voltage MOSFET and interesting candidate is the LDMOS transistor. In power amplifiers for telecommunication in the higher UHF bands, Si-BJT transistors were not replaced until the LDMOS transistor entered the scene in 1996 [24]. Apart from the high-voltage support, the LDMOS transistor can achieve very good high-frequency performance due to that the channel length, that also sets high-speed properties, can easily be made very short. An LDMOS transistor can be made using, in the simplest form, one extra process step in addition to the standard CMOS process. The other important aspect that gives the LDMOS transistor is that the channel length is a process parameter and not a lithography parameter.

There are two major structural categories of RF- MOSFETs in use today. These structures, double-diffused metal oxide semiconductor (DMOS) and LDMOS have unique behaviors: semiconductor process and geometry dependent. Figure 1 depicts the physical structure of LDMOS transistor. The LDMOS channel is predominately defined by the physical size of the gate structure (ignoring secondary effects due to diffusion vagaries) that overlies the graded p-type threshold adjust, implantation and diffusion area. The source and drain regions are on the laterally opposing sides of the gate area, and the diffusion process may produce an undercut region below the gate due to the single-step lateral diffusion process that defines the source and drain regions. The source and drain regions under bias create depletion regions that are connected by the gate induced depletion region in the p-body, and this connection defines the "effective channel length" which is a measure of the distance between the source and drain depletion edges. The depletion region is a region where the high electric field lowers the energy barrier to the electron conduction band. Once the barrier is lowered sufficiently, current easily flows between source and drain. LDMOS channel current is controlled by the vertical electric field induced by the gate and the lateral field that exists between the source and drain.

The LDMOS transistor is investigated primarily from two aspects. The first is the high-voltage performance. For a high-voltage device the most important parameter is the breakdown voltage. The second most important parameter is the on-resistance that has the properly of being in contradiction of the breakdown voltage and usually trade-offs are made to achieve acceptable performance.

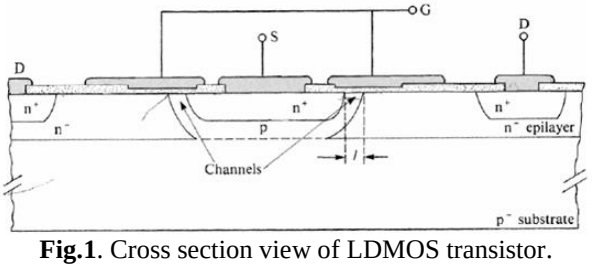

Fig.1. Cross section view of LDMOS transistor.

3. SIMULATION AND RESULTS

A <100> silicon substrate doped with boron impurity concentration of 10^{14} cm^{-3} was selected at selection stage to build the device. The growth of the epitaxy layer with a thickness of 4.5 microns at 1173 K is performed and next doped with arsenic concentration of 10^{16} cm^{-3}. An extra oxide layer was used for LDMOS transistor known as field oxide (FOX), which helps the control of breakdown voltage and on-resistance of the device. This operation is known as local oxidation of silicon (LOCOS) which is performed after epitaxial processes. After the completion of LOCOS process, we will reach to the process of building the gate. The oxidation of the gate takes place in two stages. For building the gate, first, wafer will be placed into a dried furnace for 10 min at 1308 K and 1atmosphere pressure. Then a poly-silicon layer with a thickness of 1 micron will be implanted on the substrate, phosphorus atoms with a concentration equal to 3×10^{16} cm^{-3} and 20 keV energy, will be added. At this stage, it is time to build the p-type well. To do this, first we will create a window at the desired place for the well, and then boron with impurity of 5×10^{15} cm^{-3} and energy equal to 20 keV will be added to build the well. The diffusion process is performed by entering wafer into 1373 Kfurnace for 150 min in the presence of nitrogen to help the penetration of boron. Doing this, the well building process will finish and time for the second oxidation of the gate will arrive. For this purpose, the silicon in the desired location will be removed and then a thickness equal to 0.05 micron will

be removed from the existed oxide layer [14]. Then a 0.5 micron-thick oxide layer will be added to the device and finally the oxide layer will be removed from those places that source and drain are going to locate there. The second stage of gate oxidation will come to an end by putting the device into a dried furnace with a temperature of 1308 K and 1 atmosphere pressure for 10 min [16]. After the completion of the second stage, manufacturing process of n-type will take place. For this purpose, first arsenic with an impurity equal to 5×10^{15} cm^{-3} and 50keV energy will be implanted. The diffusion process is done for arsenic penetration. This will be done by putting the device into the 1273 K furnace for 180 min in the presence of nitrogen. Then a 0.03- thick micron layer of extra oxides will be removed. The metallization process will carry out; manufacturing operation will come to an end by isolating the device. Figure 2 shows structure of the device which is simulated using Athena simulator. Moreover, some of the output parameters of the device are calculated using Atlas simulator.

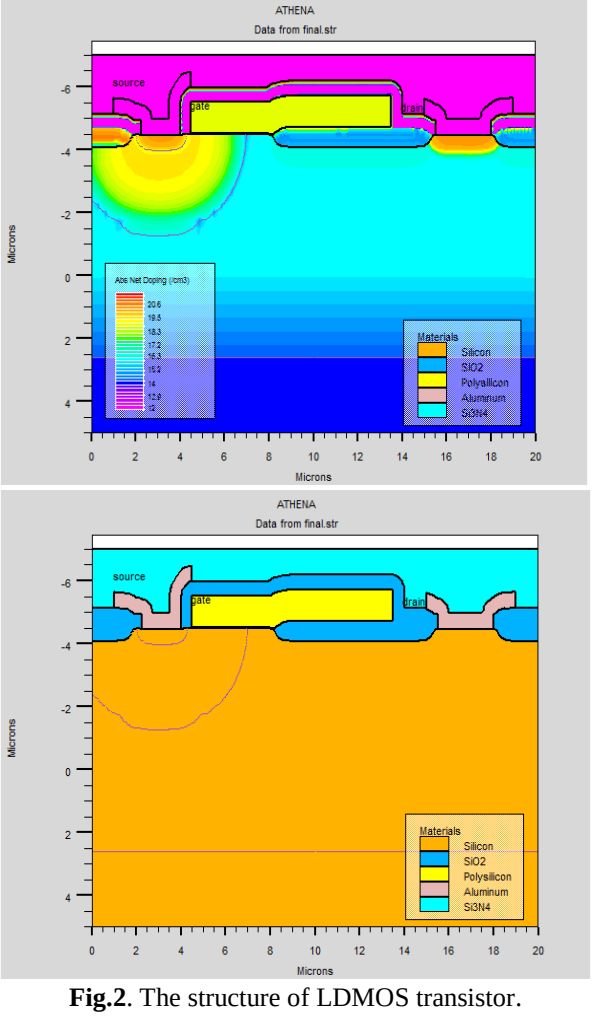

Fig.2. The structure of LDMOS transistor.

A diagram of drain current versus gate voltage was plotted to obtain threshold-voltage. We assume threshold-voltage as the gate voltage in which drain current reaches at 1μA. Figure 3 shows that threshold voltage of the device is about 1.8 V.

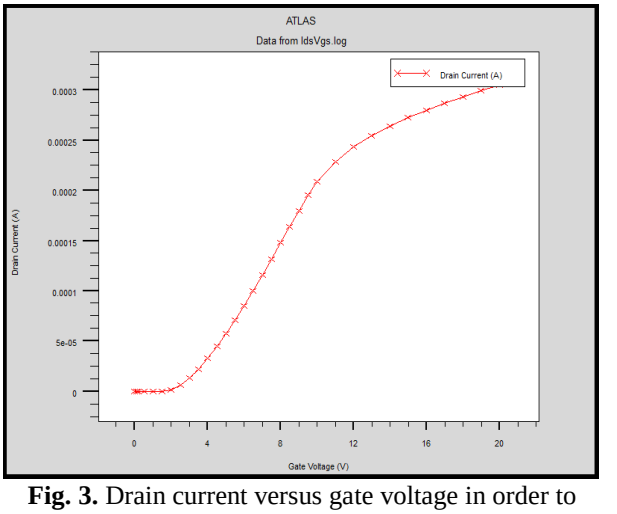

Fig. 3. Drain current versus gate voltage in order to obtain the threshold voltage.

In order to calculate breakdown voltage of the device, we should change gate voltage to zero. Figure 4 shows the drain current versus drain voltage for V_g=0. As can be seen, the current drain increases with increasing voltage. Also by paying attention to this figure, it is clear that after a while current starts to diverge and reaches to an unstable situation. The starting point of this instability is known as breakdown voltage. The results obtained from this graph shows that breakdown voltage of the device is about 59 V.

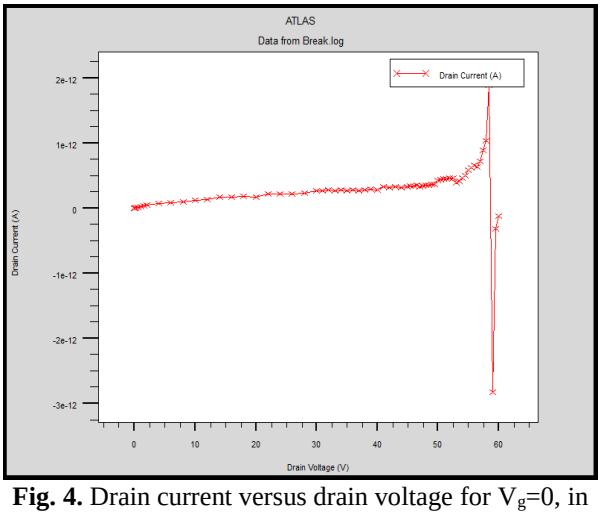

Fig. 4. Drain current versus drain voltage for V_g=0, in order to obtain breakdown voltage.

We have drawn current gain diagram in terms of frequency in order to find cut-off frequency. Figure 5 shows current gain versus frequency for the device. The point, in which current gain is equal to zero, is known as cut-off frequency. As one can see, the cut-off frequency of the device is about 2 GHz.

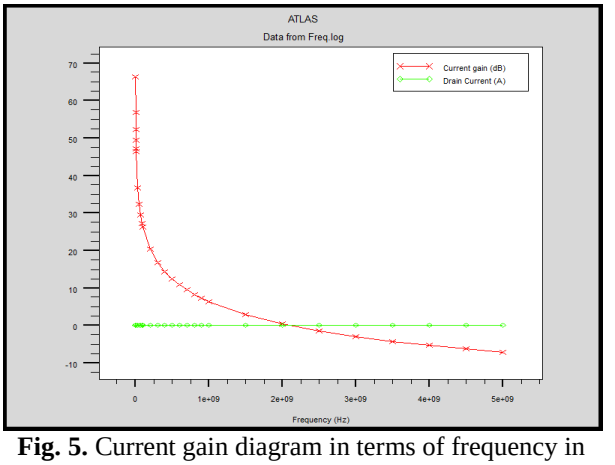

Fig. 5. Current gain diagram in terms of frequency in order to obtain cut-off frequency.

We need to calculate the slope of the drain current diagram in terms of gate voltage to calculate transconductance. Figure 6 shows drain current versus gate voltage for the device. We have extracted the slop of the curve as the transconductance of the device. The results show that maximum transconductance of the device is $4\times10^{-6}\ \Omega^{-1}$ corresponding to gate voltage of 8 V.

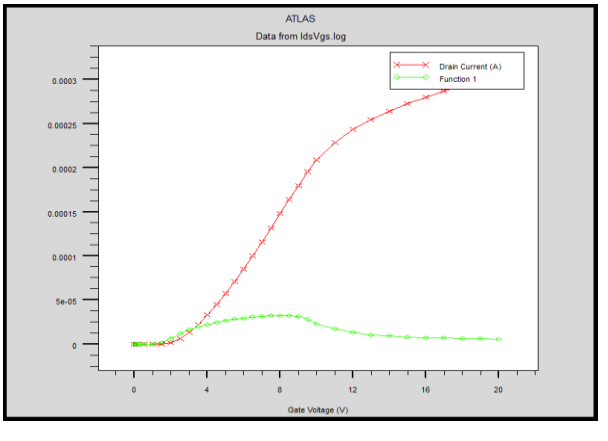

Fig. 6. Current changes diagram in terms of gate voltage changes in order to obtain transconductance.

Figure 7 illustrates the drain current versus drain voltage. The current of transistor operating point is obtained from this diagram. According to figure 6, drain current of the transistor is 8.3×10^{-5}A corresponding to drain voltage of 8 V.

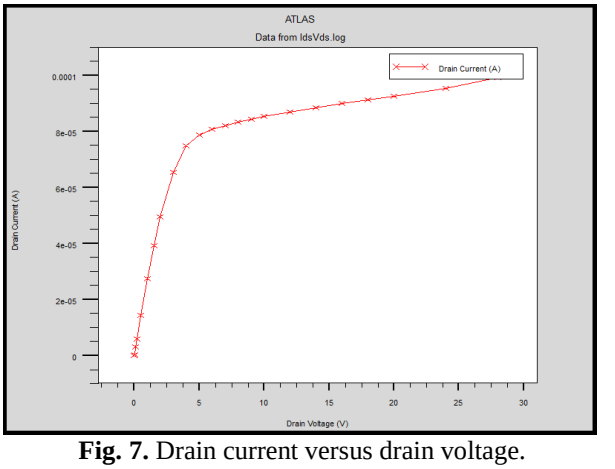

Fig. 7. Drain current versus drain voltage.

Now we want to increase the value of transistor current by changing effective factors, whereas other parameters such as threshold voltage, breakdown voltage, cut-off frequency, and trans conductance should not deviate from the desired value. As mentioned before, the value of current depends to various parameters. Therefore, by changing the thickness of oxide, implanting channel and adjusting channel length in simulation process, we try to increase current while preserving other presumed parameters which were obtained in the previous stage. First we increase the thickness of the epitaxy layer and from 4.5 to 7 micron. Then we change the thickness of the gate oxide. As we know, a decrease in gate oxide thickness will cause an increase in the current of the device. We reduce the time of oxidation process from 50 min to 45 min in order to decrease gate oxide thickness. Hence, we can increase current of the device without other parameters of the transistor which have been changed considerably. The channel length reduction is achieved by reducing time of diffusion boron impurity in stage of the channel formation. Therefore, we reduce channel length by reducing diffusion process time from 150 min to 100 min or even less. By doing so, channel length will decrease and current of the device will increase. Finally, it is to increase boron concentration in the channel formation. This operation causes a reduction in voltage drop across channel, reduction in threshold voltage and hence an increase in current of the device. The obtained results with these changes are shown in Fig.8-a to Fig.8-e.

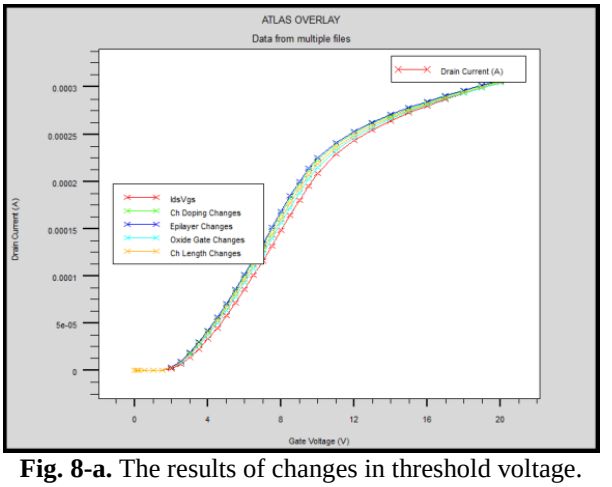

Fig. 8-a. The results of changes in threshold voltage.

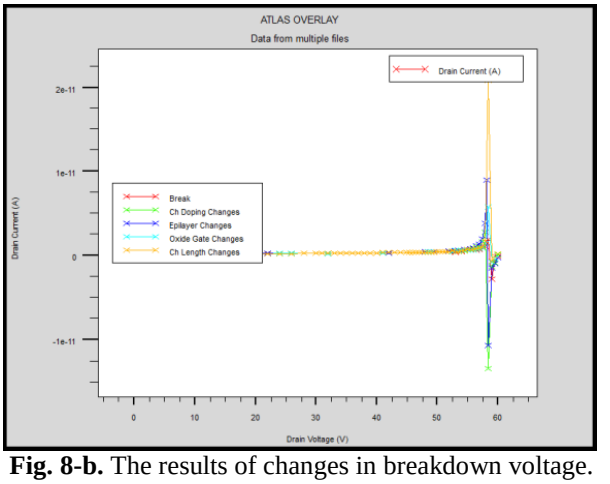

Fig. 8-b. The results of changes in breakdown voltage.

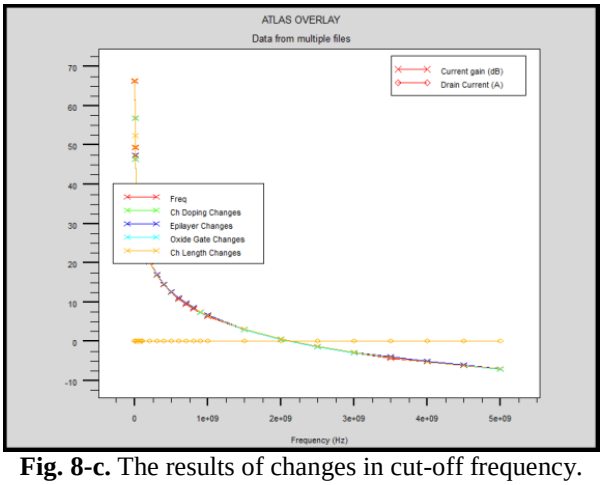

Fig. 8-c. The results of changes in cut-off frequency.

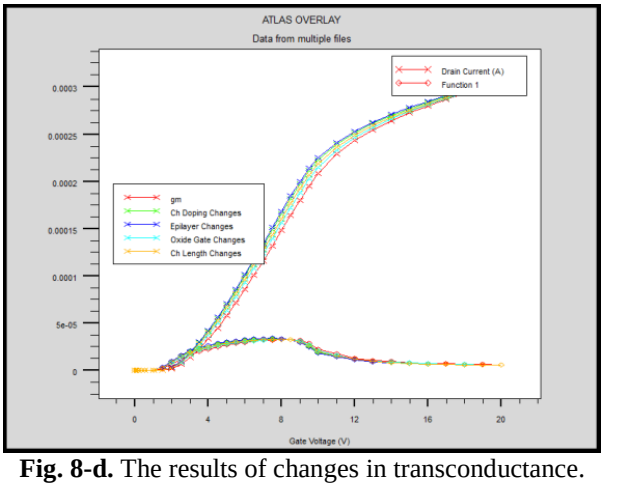

Fig. 8-d. The results of changes in transconductance.

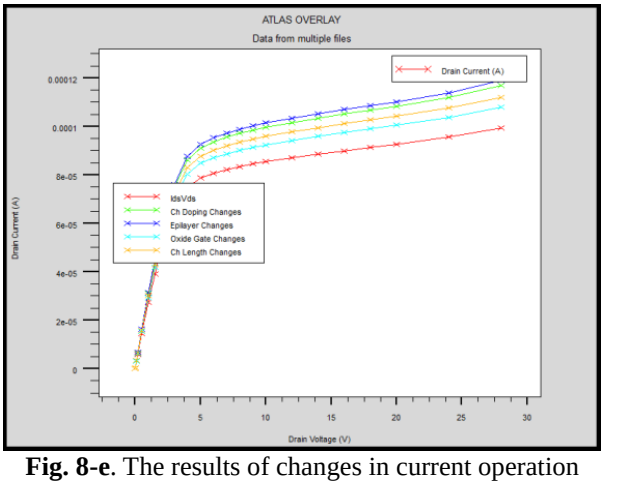

Fig. 8-e. The results of changes in current operation point.

As it is shown in figure 8a, changing these parameters does not have significant impact on the threshold voltage of the transistor. According to figure 8b, after applying changes, breakdown voltage remains nearly constant and is equal to 59 V. Figure 8c illustrates cut-off frequency after applying the changes which is constant and equal to 2 GHz. Figure 8d shows that the transconductance parameter is also constant, its maximum change value is at V_{gate} = 8V and is equal to 4×10^{-6} Ω^{-1}. However, as shown in figure 8e, by reducing gate oxide thickness, the current of work reached to 9×10^{-5} A in V_D = 8V. On the other hand, the current of the transistor increased to 9.4×10^{-5} A corresponding to V_D = 8V by means of reducing channel length. Also, current of the transistor reached to 9.65×10^{-5} A in V_D = 8V by an increase of doping concentration in channel. And finally by increasing the thickness of epitaxy layer, the current of work will reach to 1×10^{-4}A. Therefore, by optimization of manufacturing processes, we were able to increase current of the transistor compared to the initial structure

which had 8.3×10^{-5}A current corresponding to drain voltage of 8 V.

4. CONCLUSION

In this paper, our goal was to optimize the LDMOS transistor manufacturing process to increase the current of work using numerical simulation. For this purpose, we tried to increase current by changing oxide thickness, implanting channel and adjusting channel length in manufacturing process, while preserving other parameters of the transistor. First, we designed an initial structure of LDMOS transistor, and calculated important parameters of the device such as threshold voltage, drain current, breakdown voltage, transconductance, and cut-off frequency of the transistor. Then we determined parameters that affect the current of the transistor. We tried by changing characteristics of the manufacturing processes, to increase current of the transistor without considerably changing other parameters of the device. We increased thickness of expitay layer and an increase in the current of the device was seen. Therefore, the current of the transistor has a direct relationship with expitay layer thickness. In the next stage, gate oxide thickness was reduced and an increase in the value of the current was seen. Indeed, by decreasing oxide thickness, the channel formation improves; and as a result the current of the transistor increase occurred. Therefore, current of work of the device has an indirect relationship with gate oxide thickness. The next parameter was channel length; we reduced channel length by reducing diffusion time of boron impurity in stage of the channel formation. By this doing, an increase in current of the transistor occurred. Therefore, current of the device has an indirect relationship with channel length. The reason for this phenomenon is the fact that a reduction in channel length causes a reduction in resistance of the channel and as a result an increase occurs in the value of current. Finally, the doped concentration of the channel was increased, and an increase in the value of the current was seen. Hence, the current of the designed transistor structure has an indirect relationship with channel surface concentration. This phenomenon was predictable, because an increase in channel surface concentration cause an increase in transconductance and a reduction in its voltage drop.

By optimizing all of these parameters, the current of the LDMOS transistor increased to 1×10^{-4} A. Also, breakdown voltage and the maximum transconductance of the device are 59 V and $4\times10^{-6}\,\Omega^{-1}$, respectively.

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