A Novel High Voltage Gain and Low Voltage Stress DC-DC Boost Converter for Photovoltaic Applications

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ABSTRACT:
Photovoltaic (PV) panels rely on environmental conditions such as irradiation or temperature, and thus they require an interface boost converter. Non-isolated DC-DC boost converters have a lower volume, lower costs and lower power dissipation compared with isolated converters. In this study, a novel high efficiency non-isolated DC-DC boost converter is proposed to be used in PV systems. The converter includes only one semiconductor switch which causes lower switching losses. The main advantages of the proposed converter include low input current ripples, low voltage stress on semiconductor switches, high efficiency and low conduction losses. Moreover, maximum power is achieved from PV panels. A prototype of the proposed converter has been built, and experimental results are presented which explicitly validate theoretical results, suggesting that this boost converter is desirable for PV applications.

KEYWORDS: Non-isolated DC-DC boost converter, Photovoltaic systems, High voltage gain, Low voltage stress, High efficiency.

1. INTRODUCTION

Recently, global attention to renewable energies has grown more than ever due to their environmental merits and depletion of fossil fuels. Investment in clean energies such as wind turbine, PV and fuel cell is increasing. The PV systems enjoy clean and free operation which have great potentials to generate power [1]. However, the PV panels' output voltage is too low and dependent on environmental conditions such as temperature. Thus, a high voltage gain DC-DC boost converter is required to stabilize variable voltages and obtain maximum power from panels [2]. Traditional boost converters are not appropriate for this purpose because of dynamic limits, high input current and low efficiency.

Nowadays, various types of PV interfaces are proposed to achieve higher efficiency as well as lower stress. Non-isolated converters [3], and isolated converters [4] are the two main types of DC/DC boost converters, widely used in renewable energy applications. The advantages of transformer based boost converters or isolated potential include isolated DC-link voltage and more flexibility for higher voltage levels. Disadvantages of isolated structure can be expressed as:

- Input impulse current decreases the PV panel's life time.
- a large capacitor is required to regulate input current ripples [5].
- Transformer leakage inductance causes higher stress on semiconductor switches, EMI generation and higher conduction losses [6].

With respect to the mentioned disadvantages of the isolated DC-DC converter, a non-isolated one has been used in this paper. Higher efficiency, lower volume and lower costs are the reasons of non-isolated configuration superiority over the isolated model.

In [7], a high step-up DC-DC converter has been presented based on Cockcroft-Walton (CW) voltage multiplier without a step-up transformer to obtain a high voltage gain. By considering cascaded stages, voltage stress does not have any effect on switches, capacitor and inductor, but control complexity is a disadvantage of the mentioned converter. A DC-DC boost converter with a high voltage gain based on the three-state switching cell (3SSC) has been presented in [8] for split capacitor neutral-point clamp inverters. The advantages of this topology include operation at a high switching frequency, a small ripple of the input current and balanced output voltage. Moreover, in [9], a coupled inductor with three state commutation cell based converters has been presented. However, the mentioned converters in [8], [9] are hard switched converters. A switched capacitor (SC) cell in boost converter as a new method for combination of the SC converter and

switching mode DC-DC converter has been presented in [10] to achieve a hybrid solution. This solution can provide large DC gain, but it affects the non-pulsating character of the input current. Recently, more impedance source network inverters with magnetically coupled inductors have been proposed like Y-source [11, 12]. These types of converters can achieve a high variable gain, but there is large voltage spike on switches due to leakage inductor of the coupled inductor. In [13, 14], a new family of single-switch DC-DC PWM converters, operating at a constant frequency as well as duty-cycle has been presented. The advantages of this converter include higher voltage gain, small ripples of the output voltage and lower voltage stress on switches, but floating outputs with control complexity are the main drawbacks.

In this paper, a novel configuration of non-isolated boost converter is proposed. High voltage gain, high efficiency, low stress on switches and simple structure are the major benefits of this circuit. At first, the proposed boost converter and its operation modes are described in Section 2. The basic equations that are essential for calculations are presented in Section 3. Section 4 presents a comparison between the proposed configuration and other structures in order to have a comprehensive analysis about superiority of the converters. To validate the desired performance of the novel structure, computer simulations are carried out both by PSCAD/EMTDC and practically in a power electronics lab. Simulation and experimental results are presented in Section 5. Finally, Section 6 is dedicated to the conclusion.

2. PROPOSED STRUCTURE

2.1. Model Description

The proposed converter has more elements compared with a traditional boost converter. Fig. 1 shows the proposed DC-DC boost converter, which consists of eight diodes, eight capacitors and two inductors. A PV panel supplies the output load through a boost converter. The main parts of the mentioned structure (Fig. 1) are a DC power supply (V_i), a power switch (S), an input inductor (L_1), an output inductor (L_2) and two output diodes (D_7 and D_8). Other diodes (D_1-D_6) and capacitors (C_1-C_8) are used to increase the voltage gain. The number of corresponding capacitors is more than that of conventional boost converters, but they increase the converter static gain. Moreover, stress on switches is lower in comparison with the conventional boost converter. The proposed structure has eight operational modes in a continuous conduction mode (CCM) with a duty-cycle percentage equal to 60%. It is assumed that all the elements are ideal and the capacitors are large enough to keep the voltage stable in one switching period.

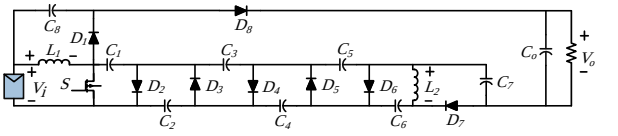


Fig. 1. The proposed DC-DC boost converter.

2.2. Converter Operation Modes

As mentioned previously, the proposed converter has eight modes in CCM and the maximum power is transferred from the PV panel to the load. At the first four modes, the power switch is turned on and then it is turned off for another set of four modes. Both inductors store energy during one switching cycle. The description of modes are as follows:

2.2.1. Mode 1 ($0 \le t \le t_1$)

In this mode, switch S, D_3, D_5 and D_8 are simultaneously turned on. Diodes D_1, D_2, D_4, D_6 and D_7 are turned off because a reverse voltage is generated by V_{Co}-V_{C7}-V_{C5}-V_{C3}-V_{C1}, -V_{C2}, -V_{C3}, -V_{C5} and $-V_{C5}+V_{C6}$-V_{C7}, respectively. During this mode, L_1 stores the system energy and its current increases linearly with the input voltage V_i. In contrast, the current of L_2 decreases linearly, as it charges C_6. In addition, Capacitors C_1, C_3 and C_5 charge C_2, C_4 and C_6, respectively. The voltages of C_7 and C_8 remain constant. Fig. 2 shows the DC-DC converter at the first mode. The gray elements in Fig. 2 are related to turned off diodes, which are in reverse bias. According to Fig. 2, the voltage equations are as follows:

$$v_{L1} = V_i \tag{1}$$

$$v_{L2} = V_{C6} - V_{C5} \tag{2}$$

$$V_{C1} = V_{C2} \tag{3}$$

$$V_{C3} = V_{C4} \tag{4}$$

$$V_o = V_i + V_{c1} + V_{c3} + V_{c5} + V_{c7} + V_{c8} \tag{5}$$

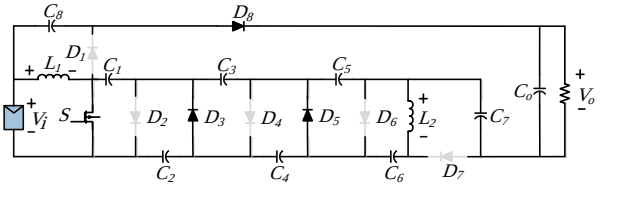


Fig. 2. The proposed DC-DC boost converter at first mode.

2.2.2. Mode 2 ($t_1 \le t \le t_2$)

In this mode, the switch S is turned on as well as D_3 and D_8. Diodes D_1, D_2, D_4, D_5, D_6 and D_7 are turned off as a reverse bias and are introduced by V_{Co}-V_{C7}-V_{C5}-V_{C3}-V_{C1}, -V_{C2}, -V_{C3}, V_{C3}-V_{C4}, -V_{C3}+V_{C4}-V_{C5} and -V_{C3}+V_{C4}-V_{C5}+V_{C6}-V_{C7}, respectively. Similar to the first mode, the currents of L_1 and L_2 increase and decrease linearly proportional to the input voltage V_i, respectively. Capacitor C_2 is charged by C_1 and the capacitors C_4 and C_6 are charged by L_2, C_3 and C_5. The voltage of C_7 and

C_8 remains constant as before. Fig. 3 demonstrates the proposed converter at the second mode. The main equation of this mode can be expressed as:

$$v_{L2} = V_{C4} + V_{C6} - V_{C3} - V_{C5} \quad (6)$$

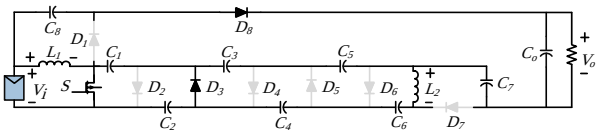


Fig. 3. The proposed DC-DC boost converter at second mode.

2.2.3. Mode 3 ($t_2 \le t \le t_3$)

In this mode, switch S and D_3 are simultaneously turned on. Diodes D_1, D_2, D_4, D_5, D_6, D_7 and D_8 are turned off because of a reverse bias which is generated by $-V_i+V_{C1}-V_{C2}-V_{C8}$, $-V_{C2}$, $-V_{C3}$, $V_{C3}-V_{C4}$, $-V_{C3}+V_{C4}-V_{C5}$, $-V_{C3}+V_{C4}-V_{C5}+V_{C6}-V_{C7}$, $V_i+V_{C2}+V_{C3}+V_{C5}+V_{C7}+V_{C8}-V_o$, respectively. The current of L_1 and L_2 increases and decreases linearly proportional to the input voltage V_i, respectively. The charging of capacitors is similar to the second mode and the voltage of C_8 is constant. Fig. 4 indicates the proposed structure at in third mode. The voltage equation is similar to the previous mode**.**

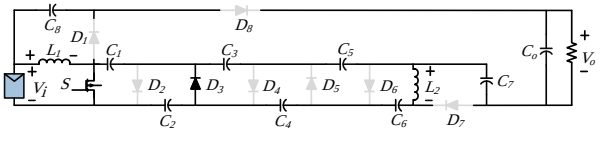


Fig. 4. The proposed DC-DC boost converter at third mode.

2.2.4. Mode 4 ($t_3 \le t \le t_4$)

In this mode, switch S is turned on and all diodes are turned off. Diodes (D_1-D_8) reverse voltages are $-V_i-V_{C8}$, $-V_{C1}$, $V_{C1}-V_{C2}$, $-V_{C1}+V_{C2}-V_{C3}$, $V_{C1}-V_{C2}+V_{C3}-V_{C4}$, $-V_{C1}+V_{C2}-V_{C3}+V_{C4}-V_{C5}$, $-V_{C1}+V_{C2}-V_{C3}+V_{C4}-V_{C5}+V_{C6}-V_{C7}$, $V_i+V_{C1}+V_{C3}+V_{C5}+V_{C7}+V_{C8}-V_o$, respectively. The current of L_1 is similar to previous modes as well as L_2, and the energy of the input power supply is stored by L_1. Capacitors C_1, C_3, C_5 and L_2 charge C_2, C_4 and C_6. The voltages of C_7 and C_8 remain constant. The proposed DC-DC boost converter in the fourth mode is shown in Fig. 5. According to Fig. 5, the voltage equation is as follows:

$$v_{L2} = V_{C2} + V_{C4} + V_{C6} - V_{C1} - V_{C3} - V_{C5} \quad (8)$$

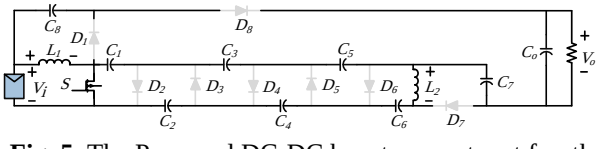


Fig. 5. The Proposed DC-DC boost converter at fourth mode.

2.2.5. Mode 5 ($t_4 \le t \le t_5$)

In this mode, both switch S as well as D_1, D_2, D_3, D_4, D_5 and D_8 are turned off. The voltages of $-V_i+V_{C1}-V_{C2}+V_{C3}-V_{C4}+V_{C5}-V_{C8}$, $-V_{C2}+V_{C3}-V_{C4}+V_{C5}$, $-V_{C3}+V_{C4}-V_{C5}$, $-V_{C4}+V_{C5}$, $-V_{C5}$, $V_i+V_{C2}+V_{C4}+V_{C6}+V_{C8}-V_o$ cause a reverse bias on D_1, D_2, D_3, D_4, D_5 and D_8, respectively. Unlike previous modes, the current of L_1 and L_2 decreases and increases linearly proportional to the input voltage V_i, respectively. Capacitors C_2 and C_4 are charged by input voltage (PV panel), L_1, C_1, C_3 and C_5. Moreover, the energy of C_6 is transferred to L_2 and C_7. The voltage of C_8 remains constant. Fig. 6 reveals the DC-DC converter in the fifth mode and the equations are as follows:

$$v_{L1} = V_i + V_{C2} + V_{C4} + V_{C6} - V_{C1} - V_{C3} - V_{C5} - V_{C7} \quad (9)$$

$$v_{L2} = V_{C7} \quad (10)$$

$$V_{C6} = V_{C7} \quad (11)$$

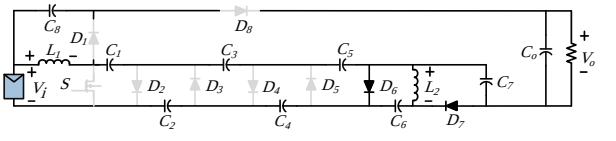


Fig. 6. The proposed DC-DC boost converter at fifth mode.

2.2.6. Mode 6 ($t_5 \le t \le t_6$)

in addition to switch S, Diodes D_1, D_2, D_3, D_5 and D_8 are turned off by the reverse voltage of $-V_i+V_{C1}-V_{C2}+V_{C3}-V_{C8}$, $-V_{C2}+V_{C3}$, $-V_{C3}$, $-V_{C4}$ and $V_i+V_{C2}+V_{C4}+V_{C6}+V_{C8}-V_o$, respectively. Similar to the previous mode, the current of L_1 and L_2 decreases and increases linearly proportional to the input voltage V_i, respectively. C_1 and C_3 are charged by the input power supply, C_2 and L_1. Capacitor C_4 charges C_5 and L_2 is charged by C_6 and C_7. The voltage across capacitor C_8 is constant. The proposed converter in the sixth mode is demonstrated in Fig. 7. The voltage of L_2 is similar to the previous mode and we have**:**

$$v_{L1} = V_i + V_{C2} - V_{C1} - V_{C3} \quad (12)$$

$$V_{C4} = V_{C5} \quad (13)$$

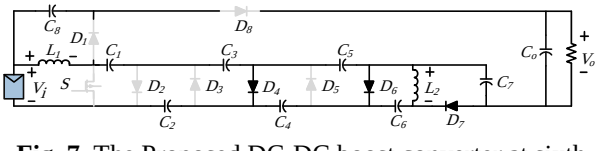


Fig. 7. The Proposed DC-DC boost converter at sixth mode.

2.2.7. Mode 7 ($t_6 \le t \le t_7$)

In this mode, switch S, D_3, D_5, D_7 and D_8 are turned off. The voltages of $-V_{C2}$, $-V_{C4}$, $V_{C6}-V_{C7}$ and $V_{C1}+V_{C3}+V_{C5}+V_{C7}-V_o$ cause D_3, D_5, D_7 and D_8, respectively to turn off. The current of L_2, unlike L_1, has

changes proportional to V_i. Capacitor C_1 is charged by the input supply and L_1, C_8 is charged by L_1, capacitor C_3 charges the C_2 and the energy of C_6 is transferred to L_2. The voltages of C_4, C_5 and C_7 remain constant. Fig. 8 shows the proposed structure in the seventh mode. The voltage equations can be expressed as:

$$v_{L1} = V_i - V_{C1} = -V_{C8} \quad (14)$$

$$V_{C2} = V_{C3} \quad (15)$$

$$v_{L2} = V_{C6} \quad (16)$$

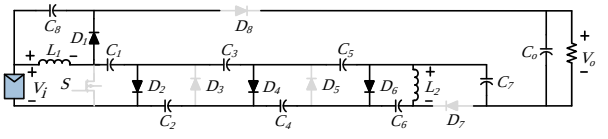


Fig. 8. The proposed DC-DC boost converter at seventh mode.

2.2.8. Mode 8 ($t_7 \le t \le t_8$)

In the final mode, switch S is turned off and D_1, D_2 and D_4 are turned on. Diodes D_3, D_5, D_6, D_7 and D_8 are turned off through reversed bias by voltages of $-V_{C2}$, $-V_{C4}$, $V_{C4}-V_{C5}$, $V_{C4}-V_{C5}+V_{C6}-V_{C7}$ and $V_{C1}+V_{C3}+V_{C5}+V_{C7}-V_o$, respectively. The current of L_1 and L_2 decreases and increases proportional to the input voltage V_i, respectively. Capacitor C_1 is charged by the input supply and L_1. The energy of L_1 and C_2 is transferred to C_8 and C_3, respectively. In addition, the stored energy of C_4 and C_6 is transferred to L_2 and C_5, respectively. The voltage of capacitor C_7 remains constant. The proposed converter in eighth mode is revealed in Fig. 9. According to Fig. 9, the voltage of L_1 is similar to the previous mode and other equations are as follows**:**

$$V_{C2} = V_{C3} \quad (17)$$

$$v_{L2} = V_{C4} + V_{C6} - V_{C5} \quad (18)$$

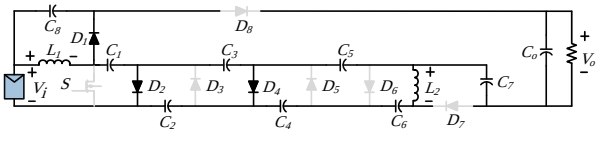


Fig. 9. The proposed DC-DC boost converter at eighth mode.

3. MATHEMATICAL EQUATIONS

Basic equations for the design and operation of the proposed DC-DC boost converter are presented in this section. The following equations are related to the voltage gain and voltage stress on circuit elements.

According to voltage balance law, inductors' (L_1 and L_2) average voltage in one switching period is zero. So, it can be written:

$$D(V_{C6} - V_{C5}) + (1-D)V_{C6} = 0 \quad (19)$$

Where D is duty cycle. The capacitor voltages can be expressed as:

$$V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_{C5} = \frac{1}{1-D} V_i \quad (20)$$

$$V_{C6} = V_{C7} = \frac{D}{1-D} V_i \quad (21)$$

$$V_{C8} = \frac{2D-1}{D(1-D)} V_i \quad (22)$$

The voltage gain of the converter is:

$$M = \frac{V_o}{V_i} = \frac{3+2D}{1-D} \quad (23)$$

Where M is the voltage ratio and V_o is the output voltage. Voltage stress on switch S is:

$$M_S = \frac{1+M}{4M} \quad (24)$$

Where M_s is switch voltage stress. The voltage stress on D_1 is:

$$M_{D1} = \frac{2(2+M)}{5M} \quad (25)$$

Where M_{D1} is D_1 voltage stress. The voltage stress on D_2-D_6 is as follows:

$$M_{D2} = M_{D3} = M_{D4} = M_{D5} = M_{D6} = \frac{1+M}{4M} \quad (26)$$

Finally, the voltage stress on D_7 and D_8 is:

$$M_{D7} = M_{D8} = \frac{1+M}{5M} \quad (27)$$

4. COMPARISION OF THE PROPOSED CONVERTER WITH OTHERS

Three important factors are considered to achieve a comprehensive analysis. Voltage gain versus duty cycle, switch voltage stress versus voltage gain, and converter efficiency versus output power are shown in the following figures. The results show that the proposed topology has a desirable performance compared with other models presented in the literature.

Voltage gain versus duty cycle for various models is shown in Fig. 10. The voltage gain of the proposed boost converter is higher than specified references for all values of duty cycle, so it has a desirable voltage gain across all power ranges and is appropriate for PV system applications.

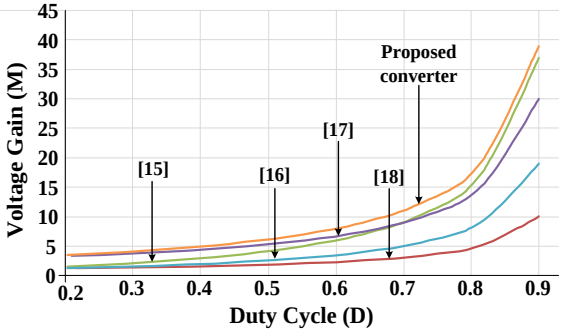


Fig. 10. Voltage gain versus duty cycle.

Fig. 11 shows voltage stress versus voltage gain for various models. According to Fig. 11, the voltage stress on switches in the proposed converter is lower than others. At high voltage gains, the voltage stress is equal to 0.25. Consideration of this factor in the design of converters is very important, because when the voltage stress decreases, it leads to lower power losses, higher efficiency and higher reliability.

The efficiency of the proposed converter for various powers is shown in Fig. 12. The converter efficiency is appropriate for all power ranges and highest efficiency is obtained at medium power levels. The converter efficiency is about 92.9% for 180W output power.

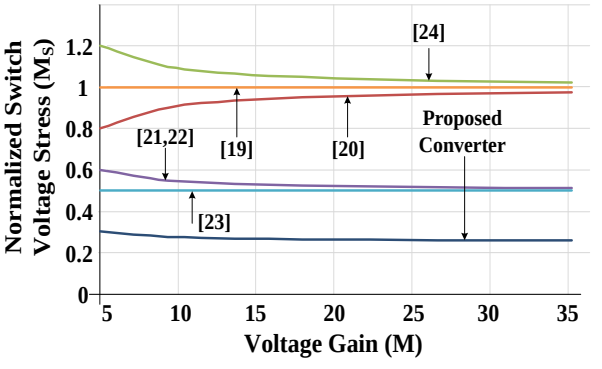


Fig. 11. Voltage stress versus voltage gain.

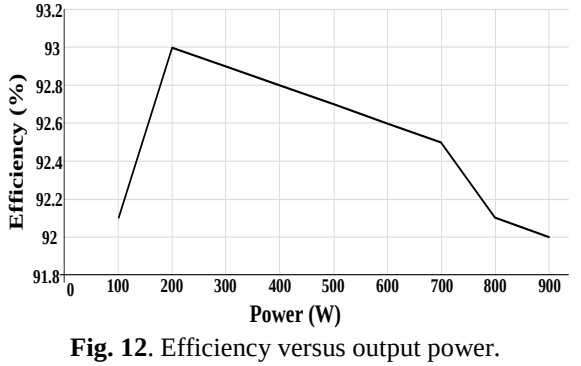


Fig. 12. Efficiency versus output power.

5. SIMULATION AND EXPERIMENTAL RESULTS

The DC-DC boost converter in Fig. 1 is simulated in PSCAD/EMTDC software. The converter input supply is a PV panel which operates on maximum power point. The maximum power which is achieved from PV panel is about 183 W. The PV panel and the converter parameter values are given in Table. 1.

Table 1. Parameters values of the PV panel and proposed converter.

	Parameter	Value
PV	Open Circuit Voltage (V_{oc})	24 V
	Short Circuit Current (I_{sc})	4 A
	The Parasitic Resistor (R_o)	0.5 Ω
	Parasitic Capacitors (C_o)	0.2 µF
Converter	Input Voltage (V_i=V_{pv})	12 V
	Output Voltage (V_o)	128 V
	Switching Frequency (f_s)	25 kHz
	Input Inductor (L)	1 mH
	Equivalent Series Resistor (R_{esr})	0.05 Ω
	Capacitors (C_1, C_2, C_3, C_4, C_5, C_6 and C_7)	330 µF
	Output Capacitor (C_o)	470 µF
	Duty Cycle (D)	0.6

In laboratory, a DC power supply has been used instead of PV panel to obtain experimental results. The following figures show that software simulation waveforms are matched with experimental results.

Fig. 13 shows the duty cycle of the converter. Duty cycle is 0.6, when maximum power is obtained from PV panel.

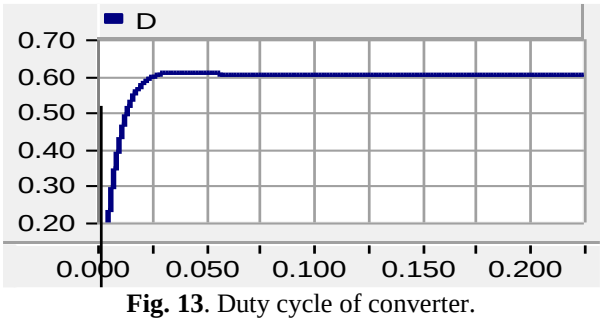


Fig. 13. Duty cycle of converter.

The output voltage of the proposed converter is shown in Fig. 14. The output voltage must be DC with low ripple and oscillations. It reaches about 128 V in 0.06 s. The experimental results confirm simulation results.

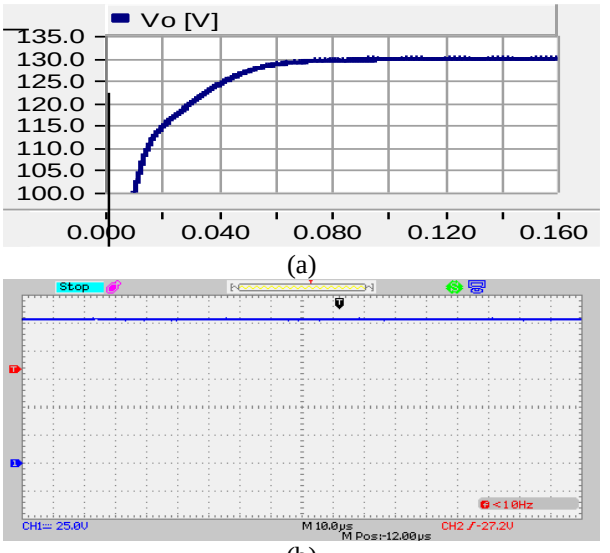


Fig. 14. Output voltage: (a) simulation result, (b) experimental result.

The current of inductor L_1 is shown in Fig. 15. Inductor L_1 current changes from 14.85 to 15.15 A with a low ripple in computer simulation. In addition, the experimental result shows that the current changes from 14.8 to 15.2 A. Both simuation and experimental results confirmed each other.

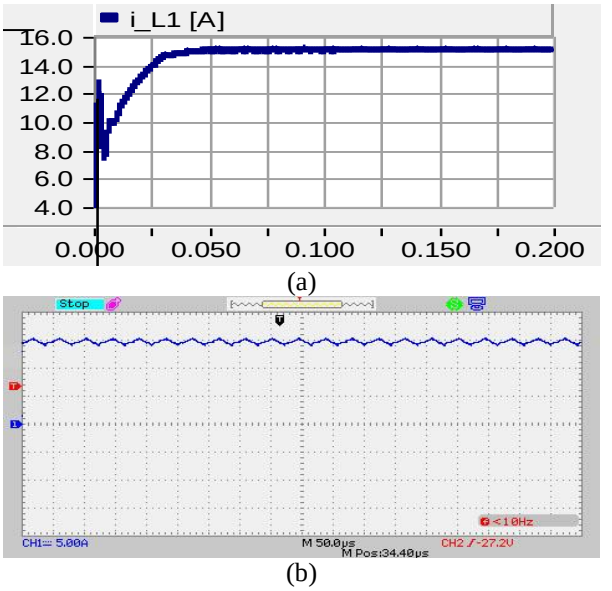


Fig. 15. Current of inductor L_1: (a) simulation result, (b) experimental result.

Fig. 16 reveals the current of inductor L_2 changing from 1.18 to 1.42 A in simulation and 1.14 to 1.45 A in the experiment. Increase and decrease in inductors' voltages occur during charging and discharging modes, respectively.

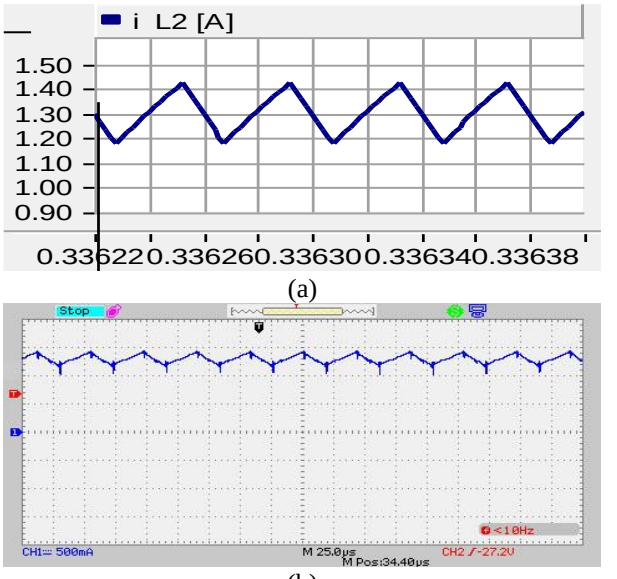


Fig. 16. Current of inductor L_2, (a) simulation result, (b) experimental result.

The voltage stress on switch S is shown in Fig. 17. Voltage stress in the simulation is about 35 V, but in the experiment, it is more due to voltage spikes.

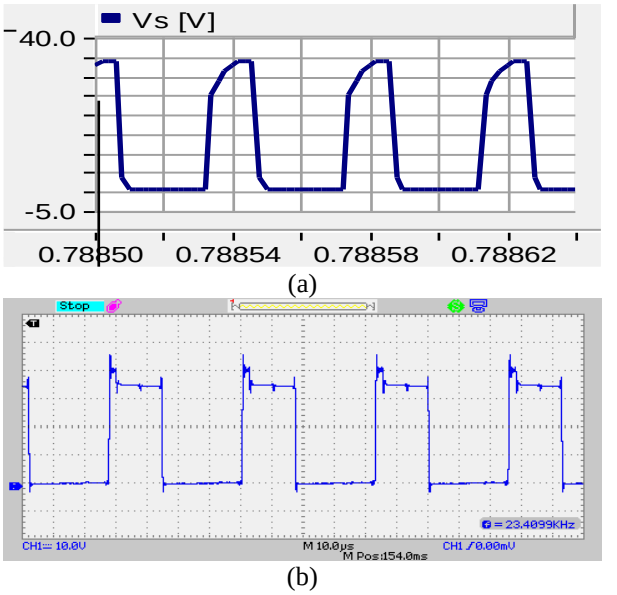
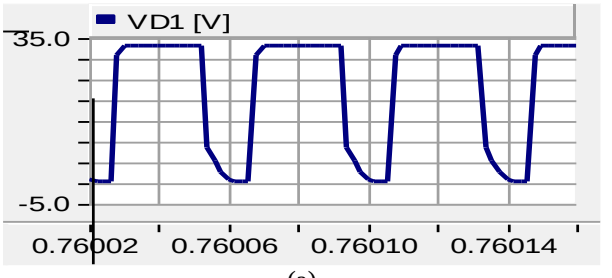
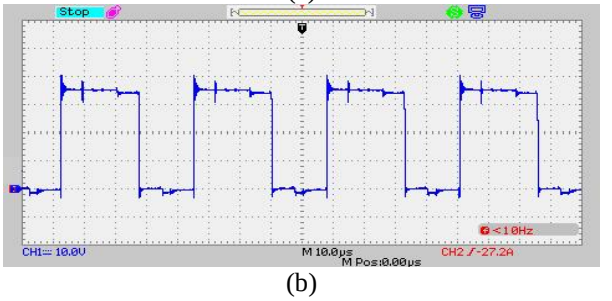


Fig. 17. Voltage stress on switch S, (a) simulation result, (b) experimental result.

Fig. 18 shows voltage stress on diode D_1. Voltage stress on D_1 is in accordance with theoretical analysis and it is about 33 V and 34 V for simulation and experiment, respectively. Voltage oscillations occur during diode conduction modes.



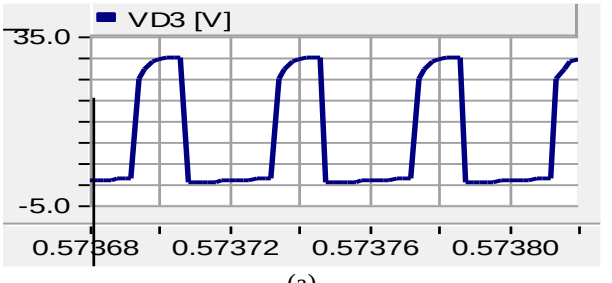
(a)



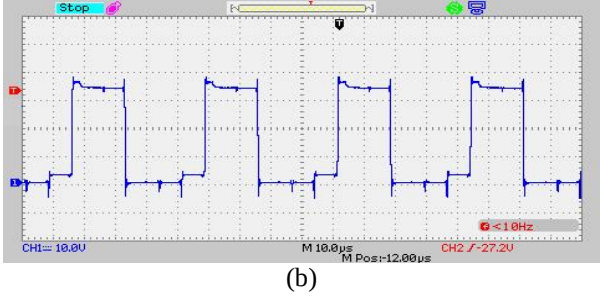
(b)

Fig. 18. Voltage stress on switch D_1, (a) simulation result, (b) experimental result.

Fig. 19 shows voltage stress on diode D_3. The voltage stress in the simulation is about 30V and in the experiment it is about 33V. When the diode conducts current, the voltage reaches its highest value and in contrast, when not conducting, the voltage is zero.



(a)



(b)

Fig. 19. Voltage stress on switch D_3, (a) simulation result, (b) experimental result.

The output power of the PV panel is shown in Fig. 20. Maximum power is achieved from the panel. It reaches 183 W below 0.1 s.

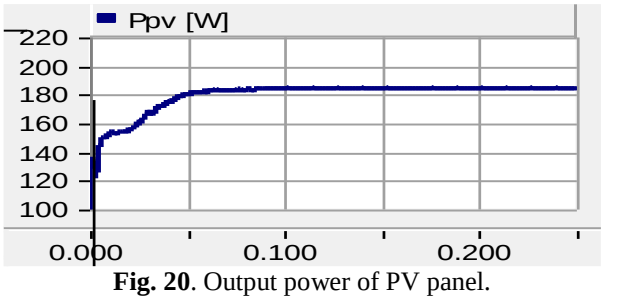


Fig. 20. Output power of PV panel.

Fig. 21 shows the voltage and current of the PV panel. The values of voltage and current are 12.2 V and 15 A, respectively. Waveforms reach a steady state within a short time.

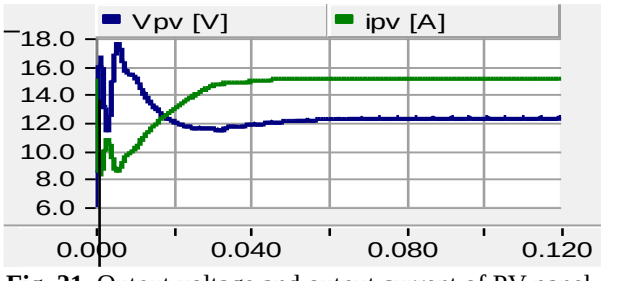


Fig. 21. Output voltage and output current of PV panel.

6. CONCLUSION

In this paper, a novel configuration of non-isolated boost converter has been presented to achieve maximum PV panel power. Other advantages of this converter include higher voltage gain, lower voltage stress on switches, lower conduction losses, higher reliability due to one semiconductor switch and high efficiency. The number of capacitors and diodes are more than that of conventional boost converters, but the nominal voltage and current are very low. This converter increases PV panel life time, as the input current ripples are about 1.87%. Moreover, the efficiency of the converter for 183 W output power is about 93%. In order to validate the proposed DC-DC boost converter, software simulation and experimental test have been used. The simulation and experimental results show that this structure is appropriate for PV panels due to low voltage stress, high voltage gain and high efficiency.

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