Low Power Delay Product 8-bit ALU Design using Decoder and Data Selector

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ABSTRACT:
The semiconductor circuits dissipate energy in the form of binary digits. This dissipation of energy is in the form of power consumption. ALU is complex circuit and is one of many components within CPU. It performs mathematical and bitwise operations. This paper proposes a new low power 8 bit ALU digital circuit for nano scale regions. The proposed ALU has two 4x1 data selectors, 2x4 decoder and an adder circuit as sub modules. The output of 2x4 decoder is connected to 3 input NAND, AND, OR, XOR gates. The low power adder and multiplexer are proposed and it is used for ALU design. With the help of selection lines of multiplexer, the conventional operations of ALU such as logical operations are performed. This proposed ALU caters the need of digital signal processing tools. Present ALU structure is simulated in Linux Computer using Cadence Virtuoso software and implemented in 180nm technology. The proposed ALU has delay of 386.0ps and average power of 677.2uW. The power delay product shows 65.58 % improvement when compared to the conventional 8-bit ALU design.

KEYWORDS: HDL, FPGA, ALU, DECODER, DATA SELECTOR, CMOS, FINFET, POWER, AREA, SPEED.

1. INTRODUCTION

A floating point ALU unit design functionalities are verified through VHDL simulation [1]. Arithmetic Logic Unit (ALU) was designed using Hardware Description Language (HDL) implemented on Field Programmable Gate Arrays (FPGAs) [2]. Authors investigated the floating point arithmetic logic unit and applied his new algorithm on FPU which reduces the area savings and total power latency [3]. A reversible design of 16 bit ALU which reduces the delay and power was proposed [4]. The author [5] has designed the low power CMOS full adder circuits using transmission function theory. All the units present in this design are operated parallel. The simulation results show slight reduction in area and power [5]. An ALU based on 4×1 and 2×1 multiplexer that shows 70% reduction in power consumption was designed using Novel 8T full adder and Pass transistor logic [6]. Another paper proposed the 4-bit ALU design for AND, OR, XOR, and ADD operations using QCA. The results show better improvement in result in terms of speed, area and power when compared to existing QCA designs [7]. A reconfigurable1-bit ALU based on double gate carbon nanotube field effect transistors (DG-CNTFETs). The obtained results show that this 1-bit ALU has 44% reduction in the consumption and 12% enhancement in delay time [8]. An ALU was designed for multifunctional processors and it was simulated in Xilinx Vivado 14.4 tool, implemented on 28nm 7000 FPGA board. Total on chip power used in this ALU is 0.123 W [9]. An ALU in seven, ten, fourteen sixteen, twenty nano meters technologies using finfet was designed in CADENCE VIRTUOSO for High Performance (HP) Mode and Low Standby Power (LSTP) Mode. The simulation results show 99.94% and 49.68% decrease in power using CD Logic in 7nm [10]. With the help of cascading technique, 8-bit ALU is designed by using 1-bit ALUs. The propagation delay was 5.52 ns in cadence tool when compared with the value of 8.29 ns for an existing system [11]. An ECRL logic ALUs in CMOS, ECRL and GNRFET-ECRL have been designed for 10nm technology and are simulated using H-spice. The power dissipation values of 38.75mW, 14.131 DW and 158.799nW respectively for CMOS, ECRL and GNRFET-ECRL ALUs were obtained [12]. This proposed paper possesses a mechanism which limits cascading data path in ALU stage. This mechanism can reduce the circuit area by 5.5% and the power consumption by 9.2% on average [13]. Using XNOR logic the low Power Area efficient ALU is designed in cadence virtuoso 180nm technology. The simulation is

carried out using, and compared with previous design of Gate Diffusion Input (GDI) technology [14]. This paper describes 8-bit ALU using low power 11-transistor full adder (FA) and Gate diffusion input (GDI) based multiplexer. The designs were simulated using Tanner EDA tool v15.0 in 32nm BSIM4 technology. Performance analyses were done with respect to power, delay and power delay product [15]. The ALU design is based on Look-Up Table (LUT) multiplier. The proposed ALU is designed using Verilog and verified using Xilinx Virtex-5 XC5VLX30 FPGA [16]. A new 32-bit ALU on 40nm based Virtex-6 FPGA is designed using voltage scaling and capacitance scaling. This ALU operated at 0.9 GHz at different voltages by also using capacitance scaling.

X-Power Analyzer was used for Power calculation and Xilinx ISE Design Suite 14.2 as simulator [17], A new ALU architecture that allows to Hard-core processors to be generic propose without losing hard-core performances [18]. Genetic algorithm processor comprises of designing of sub modules, like Control system, ALU, memory unit. The designed was carried out using VHDL in Xilinx ISE tool and implemented on Spartan 3A FPGA [19-21]. Energy efficient ALU on 90nm based Virtex-4 FPGA was designed using different I/O standards. The reduction in total power dissipation was to 95.13% with LVCMOS15 and a Clock Gating [22-25]. The AES algorithm plays a vital role in security communication and it has less memory and CPU constraints. The clock gating and power gating techniques are addressed for low power techniques in SRAM based FPGA system [26]. The minimum low power requirement is needed for optical switches and sensors [27]. The low power and high gain semiconductor optical fiber are implemented for power boost converters and switching functions [28]. The load frequency controller parameters tuning is proposed to minimize the error of power system. The GRC, GDB and communication time delay models are considered for power system [29]. The BESS is useful for low power electric vehicles and AC micro grid has been addressed. The dynamic model of EV has been proposed [30-31]. The high switching is obtained by using white graphene [32].

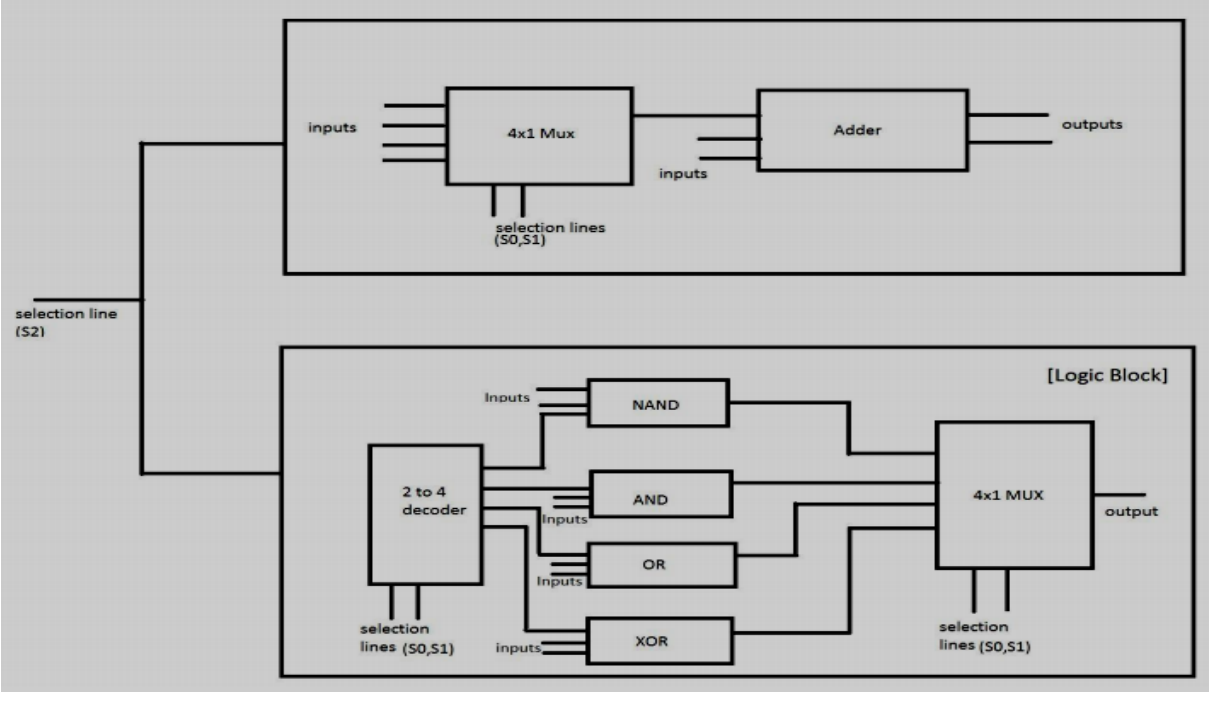

Fig. 1. The block diagram of proposed ALU.

2. SYSTEM MODEL

An arithmetic-logic unit (ALU) is the part of a computer processor (CPU) that carries out arithmetic and logic operations on the operands in computer instruction words [33]. The proposed architecture of ALU contains two data selectors of four inputs, we used a 2*4 decoder which operates with the selection line s2. The decoder has four outputs and each output is given to logic gates such as NAND, AND, OR and XOR. Again logic gates outputs are given to the

multiplexer. The general system model for ALU is shown in fig.1. Table1 shows the truth table for ALU operation in which different arithmetic and logical operations are performed with different inputs of selection lines of S_0, S_1, S_2. We have designed the truth table on our convenience. The operations such as decrement, increment, addition, subtraction, NAND, AND, OR and XOR are performed on this proposed ALU.

Table 1. Truth table used for ALU operation.

S_0	S_1	S_2	***Output***
0	0	0	*DECREMENT*
0	0	1	*INCREMENT*
0	1	0	*ADDITION*
0	1	1	*SUBTRACTION*
1	0	0	*NAND*
1	0	1	*AND*
1	1	0	*OR*
1	1	1	*XOR*
0	0	0	*DECREMENT*
0	*0*	*1*	*INCREMENT*

Implementation

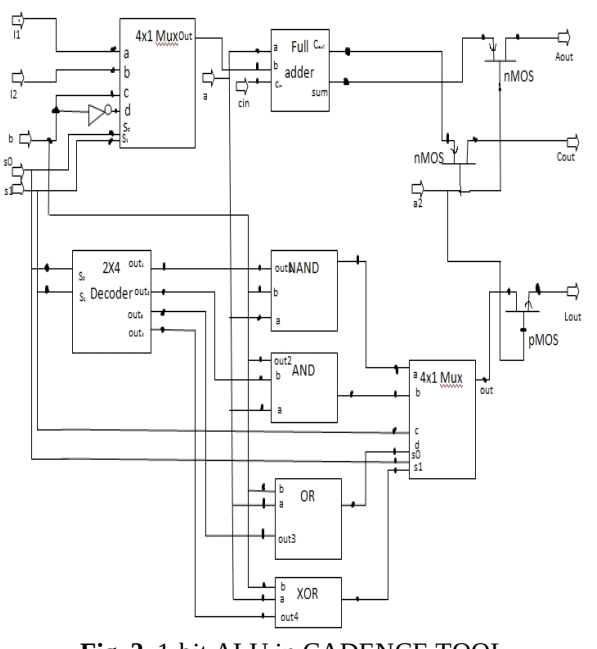

Fig. 2. 1-bit ALU in CADENCE TOOL.

The Arithmetic Logic Unit (ALU) is implemented by using Adder, Multiplexer, Decoder, and four logical gates (NAND, AND, OR, XOR). The design is performed at gate level as shown in fig.2. The standard primitive gates are used to build various blocks.

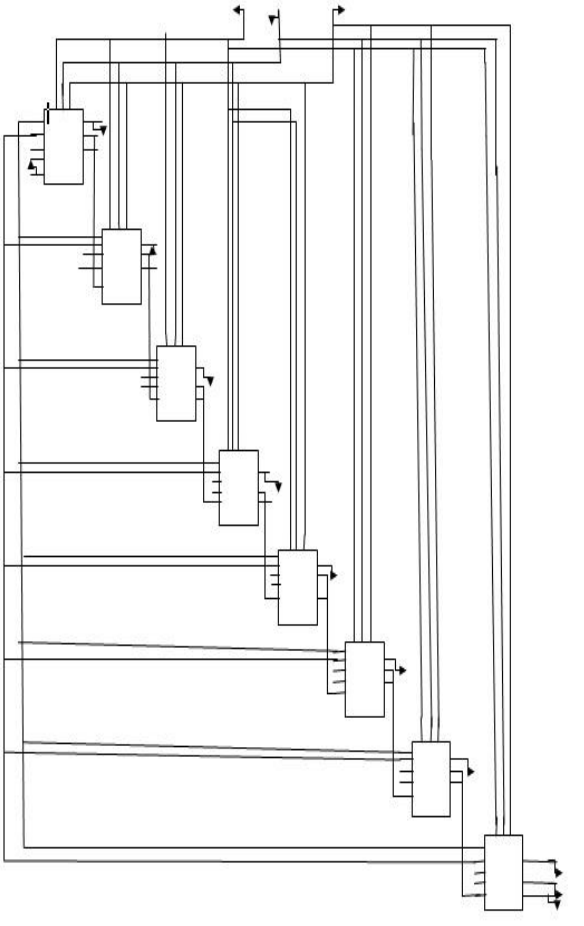

Fig. 3. 8-Bit ALU design using CADENCE TOOL.

The table 2 illustrates the performance comparison of proposed 8-bit arithmetic and logic unit and conventional 8-bit arithmetic logic unit with decoder and data selector modules. The reduction rate of power delay improved in proposed design than the conventional techniques. The fig.1. Shows the system model for one bit ALU in memory system. The delay and power measurement is analyzed by using transient analysis. When the same one bit ALU were used to design the 8 bit ALU, there was an increase of energy consumption for both conventional and proposed 8-bit full adder due to parasitic effects. The dynamic power is calculated using switching activity of logic gates, supply voltage of 1.8 V and load capacitance. The transient results are analyzed with input data at ambient temperature. The power of 16-bit arithmetic and logic unit is 1.44 times higher than 8-bit arithmetic and logic unit.

We have designed this 8-bit ALU by simply cascading the 1-bit ALU in the cadence tool software as shown in fig 3.

Table 2. Comparison with existing designs with respect to power and delay.

Design	Power	Delay	Power delay product
Design and optimization of 8 bit ALU using reversible logic [11]	-	5.52 ns	-
Design, analysis and performance comparison of GNRFET based adiabatic 8-bit ALU [21]	38.75 mW	-	-
Implementation of Low Leakage and High Performance 8-Bit ALU for Low Power Digital Circuits [22]	0.7786 µW	21.8 ps	16.97x10-18J
VHDL implementation of 8-bit ALU [23]	38 mW	13.58 ns	516.04 x10-12 J
Multi-level approaches to low power 16-bit ALU design [24]	54 mW	5 ns	270 x10-12 J
Design of High Speed, Area Optimized and Low Power Arithmetic and Logic Unit [25]	27 µW	76 ns	2.052x10-12 J
Proposed System	**0.6772 nW**	**386.0 ps**	**261.3992x10^{-21} J**

3. RESULT ANALYSIS

(i). Power comparison

The proposed ALU design is observed to offer low power characteristics at all VDD values. The dynamic power dissipation is calculated by the equation 1.

$$P_{dynamic} = \alpha \times f \times C_l \times V_{dd}^2 \quad (1)$$

The ALU is implemented by using full adder. The basic component of full adder is XOR gate. The sum and carry expression for full adder circuits are implemented by using equation 2 and 3.

$$Sum = (A \oplus B)C' + (A \oplus B)'C \quad (2)$$

$$Carry = (A \oplus B)'A + (A \oplus B)C \quad (3)$$

The circuit style of XOR gate is shown in fig 4. The circuit is implemented with 180 nm technology.

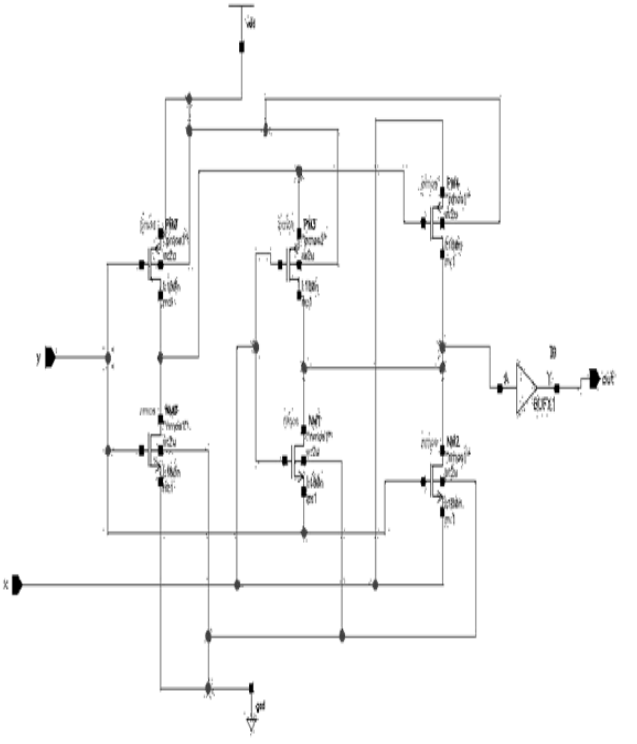

Fig. 4. XOR gate in circuit style.

All other designs offer intermediate power between the two extremes. The proposed ALU design offers 38% saving with respect to the Static CMOS and Mirror adders. This proposed design offers a minimum-transistor option to meet the desired requirements where other low-transistor designs fail to provide power efficiency.

(ii). Delay Comparison

Propagation delay generally depends on the supply voltage. As observed in the table the proposed design shows less delay than other topologies. Due to large amount of the threshold voltage loss in the pass-transistor circuits, the delay gets affected.

(iii). PDP Comparison

At very low supply voltages, ALU shows less performance. The proposed ALU offers stable PDP value throughout the supply voltage range, offering significant improvement compared to existing designs at lower voltages. In particular, it offers as much as 65.58 % improvement in PDP at VDD 1.8 V with respect to the conventional systems

(iv). Temperature Analysis

The variations in temperature will affect the performance of the circuits. This proposed design was

done under ambient conditions and mostly performance was estimated in range of room temperature. The supply voltage is fixed at 1.8 V.

The simulation result of 1-bit full adder as shown in fig 5. The input patterns are applied to stimuli to check the performance of 1-bit adder circuit. The full swing voltage is achieved through the transient analysis.

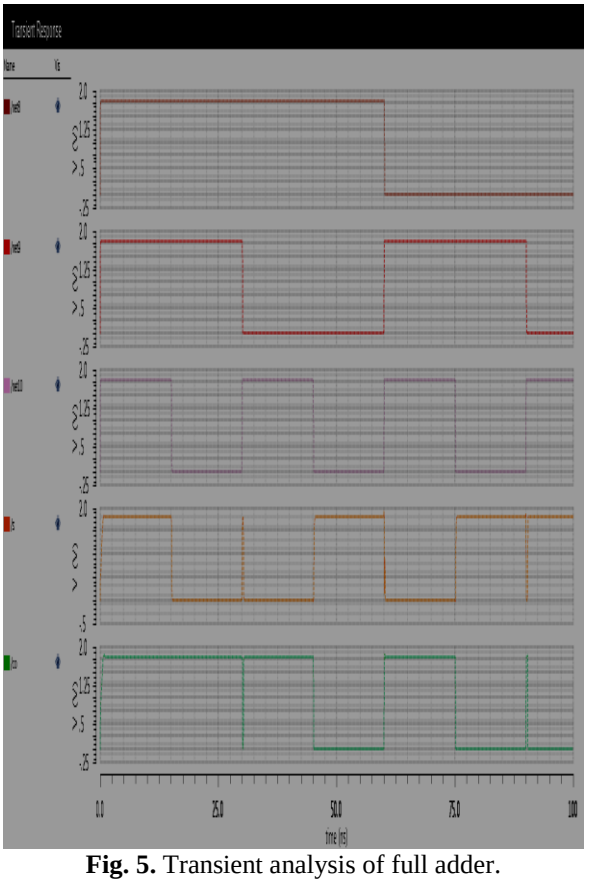

Fig. 5. Transient analysis of full adder.

4. CONCLUSION

The proposed ALU system is implemented in 180nm technology using cadence virtuoso tool. The circuit schematic designed and the circuits are simulated for functionality verification. The proposed ALU has delay of 386.0ps and average power of 677.2uW. The power delay product shows 65.58 % improvement when compared to the conventional 8-bit ALU design.

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