Design of a Novel Fault Tolerant XOR Structure in Quantum Dot Cellular Automata

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ABSTRACT:
Quantum Cellular Automata (QCA) is one of the main substitutes for CMOS technology and it is used in implementation of different systems. Manifest features including high speed and low power consumption increase the subject of the QCA in research. However, the extensive possibility of occurrence of defects and appropriate physical implementation in the QCA is one of fundamental challenges in using such technology. In this study, basic details about nanotechnology and related discussions to the fault tolerant in this field are presented. In addition, by investigation on several XOR gates, two novel XOR gates are proposed, these gates were designed by using fault tolerance tile structures. Afterwards, for determining the optimum gate, the tolerance rate of these gates against missing cell defects were investigated. Simulation results showed that proposed gates have more tolerance against missing cell defects.

KEYWORDS: Quantum Cellular Automata, Fault Tolerant, XOR Gate, Tile Structure, Nano Electronic.

1. INTRODUCTION

Quantum cellular automata (QCA) are one of the most significant new Nano scale technologies for the implementation of various systems that forms an atomic electron repulsion property. The basic element in this technology is a cell consisting of four quantum dots and two electrons as shown in Figure 1(a). By using this cell, the basic elements are made in this technology and by using them we make required different circuits [1], [4]. Reducing the dimensions of transistors will decrease the power supply voltages and will increase the operating frequency. These events cause inappropriate performance such as leakage current, which reduces the scalability of modern transistors. QCA is one of the qualified candidates for circuits alternative CMOS due to its advantages and features including; high speed, small size, and low power consumption [5]. QCA cells can be implemented with conductor, magnetic, and molecular structures. Among these, focuses on molecular and magnetic implementation that gives greater speed and moreover, can be functional in room temperature [6], [10]. In QCA, information processing can be performed through two essential inverter gates; the majority gate and the binary wire. In Figure1, these modules are illustrated.

In QCA fault tolerance is considered as one of the most important because, despite the existing defects in this technology, it is clear that reliability in QCA based systems faces problems. In modern Nano technologies such as QCA, with the large degree of doubt in performance due to quantum mechanisms that lead to a great number of different defects of implementation and operation of QCA circuits to happen, it is obvious that appropriate framework must be prepared [11].

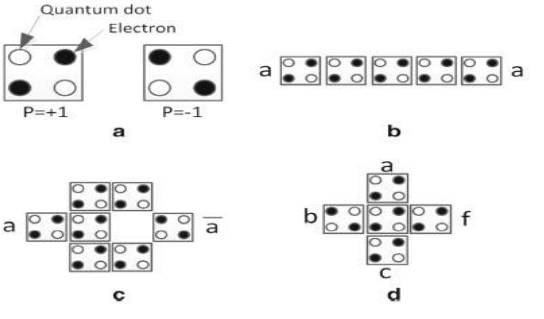

Fig. 1. Elements in QCA: (a) QCA cell, (b) binary wire, (c) inverter, (d) majority gate of three inputs base.

Therefore, there should be some solutions to identify it in the event of an error. In other words,

circuits should be designed to show a higher level of fault tolerance. In this regard, in this paper a fault tolerance XOR gate is designed, in order to design larger modules and computing circuits fault tolerance. The rest of this article is prepared as follows. In part 2, the basic concepts of QCA are reviewed. In part 3, some of the existing QCA defects and discussions about the design of fault tolerant circuits and some of the XOR gates are discussed. In section 4, the proposed gate is introduced and the results of the simulations performed are presented. Finally, the fifth part deals with the conclusion of the paper.

2. MATERIALS AND METHODS

2.1. Clock Signal

Each cell in the QCA needs a clock signal, there are tunnels in the structure of the cell between the dots that allow the electrons to get transferred between the dots. These tunnels are equipped with obstacles that can block the connecting path between the dots. The cell signal clock by controlling these obstacles can put these cells in four phases, during switch phase the tunnels are closing and under the effect of neighboring cells a cell switches into one of the stable polarizations, in other words, that is the ability to capture. During hold phase the tunnels are closed and the potential amount in the cell is maintained regardless of the neighbors and the cell has a logical value. The next phase is called the release as the obstacles start to reduce the tunnels begin to open and the cell gradually loses its amount. At the last phase that is called relax phase, the tunnels are completely open and the cell is abnormal. In Fig 2, these four phases can be observed [12], [14].

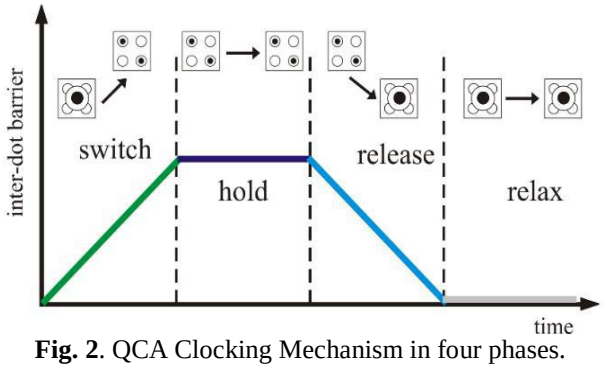

Fig. 2. QCA Clocking Mechanism in four phases.

2.2. Majority Gate

As aforementioned, the main element in QCA is the majority gate. Each circuit can be implemented by using the majority gate and an inverter, the majority gate of 5- inputs is particularly important in the design of QCA circuits, most of the circuits that design nowadays, by using majority gate of 5- inputs are design. In Fig 3, multiple majority gates of 5 inputs have gathered.

2.3. Gates based on NNI

However, the gates that have been introduced so far are enough to implement and design for all known circuits, but always having more gates hoping for a more efficient design will increase one of these gates that can be mentioned the NAND-NOR-INVERTER gate (NNI) [11], [17]. In Figure4, the building and its schematic are clarified and its logical function is also NNI (A, B, C) =A′B+BC′+ C′A′, This gate can also be converted to more recognized gates like the MV gate. If the inputs A and C are equal, the output regardless of the other input (B), gets a contrary value with the bases A and C. If the inputs A and C are different from each other they neutralize the effects of each other, and the winner of this competition is the input C, whose value will be inserted in the output. The significant difference that the NNI has with MV is in the asymmetry of their inputs, so that each of the four bases of the MV gate can be converted to input and output and does not affect the order and weight of the inputs on the gate output. But at NNI just one base can be the output of the gate and in their inputs we see the difference in the importance of them.

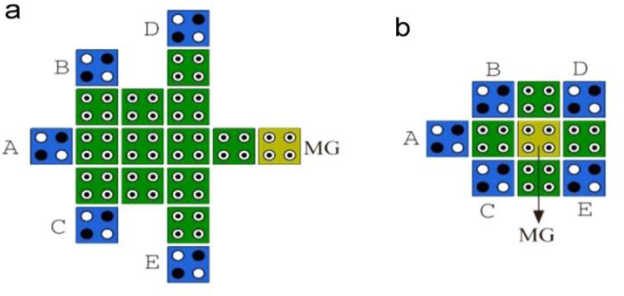

Fig. 3. Majority Gate of 5 inputs: (a) introduced sample in [16], (b) introduced sample in [15].

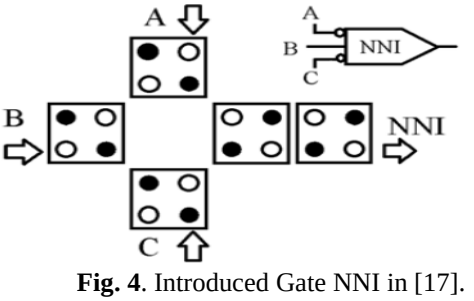

Fig. 4. Introduced Gate NNI in [17].

3. FAULT TOLERANT AND XOR GATES DESIGN

3.1. Common Faults in QCA

Considering the different defects of the QCA and the need to distinguish these defects, some of these essential defects will examine in this study in order to design fault tolerant circuits in QCA.

I. Cell displacement defects

This defect happens when the cell is deviated for a few nanometers from its original place and this creating distance causes to attenuation, if the distance increases it stops the signal transmission process [18] [23].

II. Cell misalignment defects

This defect can be created as a defect cell deviates from its true direction, in addition to the distance between the cells is more than normal cells, defective cell diverted from its axis [18], [23].

III. Missing cell defects

In this defect although a proper cell has already been fixed in a location, at the moment it is not at its specific place [18], [23].

IV. Cell rotation defect

This defect occurs when a cell rotates in the same location as it is. In a quantum block such a problem can be affected on adjacent cells and thus the circuit output [22], [24].

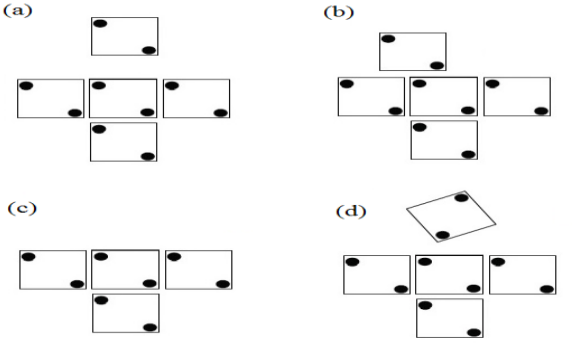

Fig. 5. Some common defects in QCA: (a) cell displacement, (b) cell misalignment defects, (c) missing cell, (d) cell rotation.

3.2. The Technique of Creating Fault Tolerance Structures using 3 × 3 Tiles

In [21], [23] tile structure is introduced such as a model to fabricate redundancy in the basic blocks of the QCA. On the whole, tile structure composed of the square set of QCA cells as N×N that are added to the circuit for instance 3× 3. A remarkable feature in tile structures is that the risk of signal attenuation gets the minimum value by making the redundancy and the signal that moves towards the output, furthermore to its logical stability has high level of polarization. According to simulation consequences output will be in strong polarization. In [25] at base blocks in terms of fault tolerant, the tile was evaluated and it became obvious that using tile due to redundancy to fabricate suitable direction in the circuit causes circuit tolerability against the defects.

3.3. XOR Circuit

The XOR gate is one of the most useful basic blocks in the QCA, which can be used for fabricating modules such as adder and parity generators. For this reason, the design of tolerance XOR gates which, as well as high speed and low area fault tolerant are from great values. In figure 6, the several XOR gate is designed in 3-input and 5-input majority gates base, each of these gates has specific features. Some circuit in [26], [28] only by using the gate of the majority of 3-inputs and some of [29], [30] using both structure of 3-input and the 5- input designed, the gate [31] has a different property than other gates, although this gate has a lower latency than the rest it is not evaluated due to use of multilayer structures in terms of appropriate fault tolerance. As can be observed in figure6, these XOR gates differ from each other in terms of physical features such as the number of cells, number of using gates in design and the rate of tolerance against defects. Following, the decision is to design a schematic and using both 3-input and 5-input majority gate in form of two different Gate tile XOR which will be introduced later.

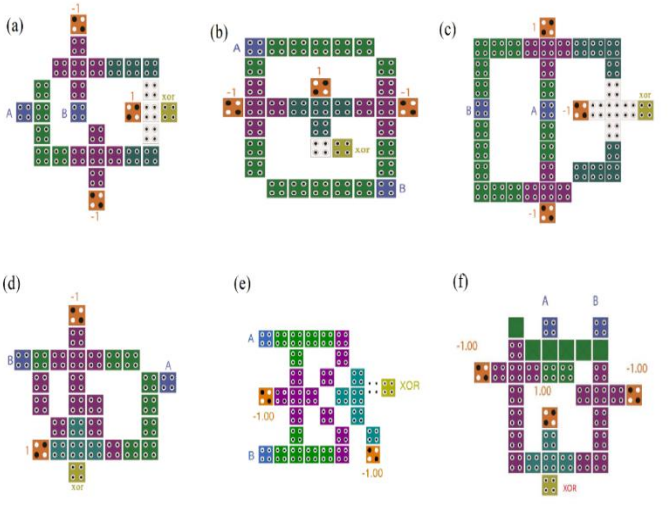

Fig. 6. The structure of some available XOR gates: (a) The introduced gate in [26], (b) the introduced gate in [27], (c) the introduced gate in [28], (d) the introduced gate in [29], (e) introduced gate in [30], (f) the introduced gate in [31].

4. THE PROPOSED GATES DESIGN AND SIMULATION RESULTS

The proposed XOR gates are simulated using QCADesigner2.0.3 [32] with specific features. The most important issue to be considered for designing new XOR gates is fault tolerance which will be discussed further, in the design of these gates redundancy was applied, however, at the first gate it is tried to use less redundancy so that the size of circuit is

not increased. On the other hand, the fault tolerance of the defects of this gate is also greater than the other designed circuits. According to the above, the physical properties of the first gate seems that has an appropriate area of 0.11 micrometers square with 61 cells and a clock delay due to the redundancy and toughness of the circuit, this gate was created with employing 3 × 3 tile structures for 3- input and 5- input majority gates. However, in the second gate a complete fault tolerant gate was designed regardless to rise in cell number. The new gate area did not change much and increased by 0.01 micrometer to 0.12 micrometers, but the number of the cell has increased by 57% to 96, However it is important to note that the delay of the circuit has not changed. At the first level, both of circuits instead of using 3-input, a tile structure of 3 × 3 NNI was used and the number of employed gate levels has decreased from 3 levels to 2 levels. Figure7 presents the structure and waveforms of the proposed gates, Table1 also indicates the physical characteristics of different gates. In the following, the tolerant rate and comparison of new gates against missing cell defects will be investigated.

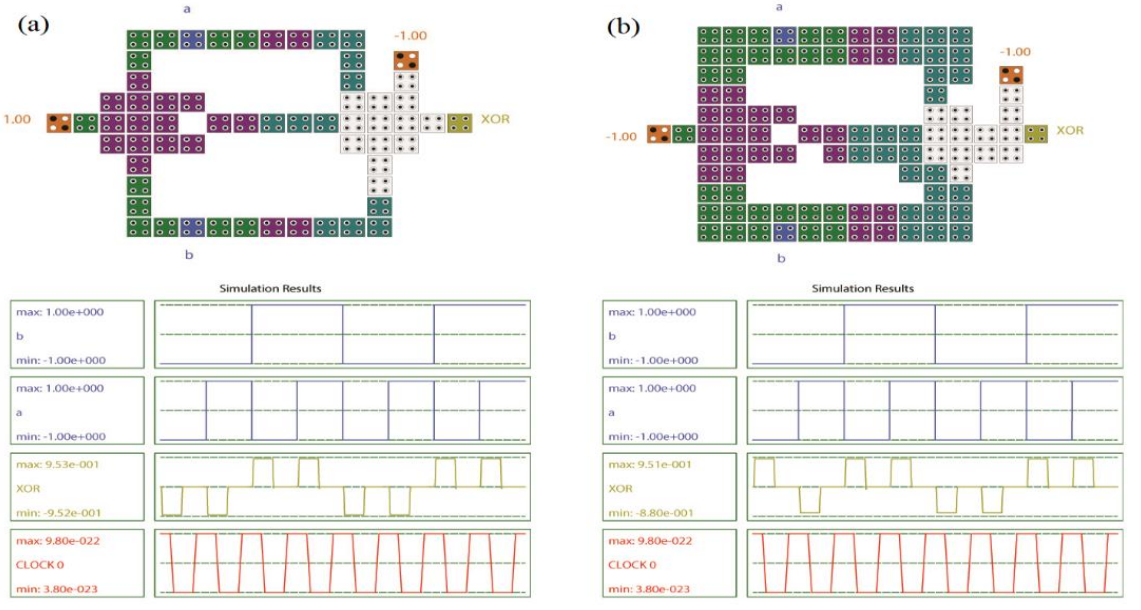

Fig. 7. The structure and form of the introduced new wave of the gates: (a) structure and waveform of the first fault tolerance of XOR gate that are used in this gate with tile structure in majority gates, (b) Structure and Waveform XOR second fault tolerant which is also used in tile structures in addition to majority gates in the wiring.

Table 1. The characteristics of simulated gates with new gates

#	Design name	number	area (um^2)	latency (Clk)
1	[26]	29	0.03	1
2	[27]	35	0.02	1
3	[28]	41	0.04	1
4	[29]	29	0.03	0.75
5	[30]	32	0.02	1
6	[31]	39	0.03	0.75
7	Proposed 1	60	0.11	1
8	*Proposed 2*	*96*	*0.12*	*1*

4.1. Assessing the Tolerance Rate of XOR Gates to Missing Cell Defects

The use of fault tolerant structures utilizes the circuit more resistant and reduces the circuit sensitivity to defects such as the missing cell. According to the evaluations carried out in [33] the results indicate that using majority gate structure in the form of an NNI reduces the circuit sensitivity to the missing cell defects, for this reason in order to increase the circuit tolerance in the XOR gate design, a similar structure was employed. Another point that makes the use of this gate more relevant is that the circuit gate level also has come lower with this structure because in place of using a majority gate and a inverter and increasing the area and number of cell in the circuit, using this structure caused both the majority and the inverter property to be gathered in a smaller gate to see a decrease in a gate surface, which has great significance in creating a smaller area and lowering the general delay. As is presented in the table1, the delay of this gate with redundancy and having fault tolerance features is just one clock and in the low latency phase, it is also possible to compete with today's small circuits. Missing cell defects is one of the most important defects that occur in QCA based on circuits. In the event of this occurrence due to cell misalignment in its place, the circuit operation that is transmitting the polarization is compromised which in most case causes a defect in the circuit main operation. To determine the circuit tolerance rate against this defect, the number alone does not illustrate the fault tolerance in the circuit because the number of gate cells is different. There may be a 200-cell gate where, cutting off a 15-cell caused defect in the circuit. There is also a 30-cell gate and removing only 5 cells caused the defect in circuit operation. Figure 8 represents the percentage results in another perspective for a better evaluation. The existing numbers in Figure8 represent the percentage of cells in the circuit, by removing them from the output, circuit did not change. In the simulation that is exhausted, each cell was removed from the circuit and thus at each phase the recorded output result was observed, whether the output changes or not. The results of these simulations revealed that introduced gates in this paper have a much more acceptable and powerful performance than other gates.

5. CONCLUSION

In this study XOR fault tolerant circuits with using 3*3 tile structures for 3 and 5-input majority gates was suggested. The use of fault tolerant utilizes the circuit more resistant and reduces the circuit sensitivity to defects such as the missing cell. A remarkable feature in tile structures is that the risk of signal attenuation gets the minimum value by making the redundancy and the signal that moves towards the output, furthermore to its logical stability has high level of polarization. The simulation result indicated that the designed XOR gates in this study have a higher fault tolerant level rather than previous XOR gates.

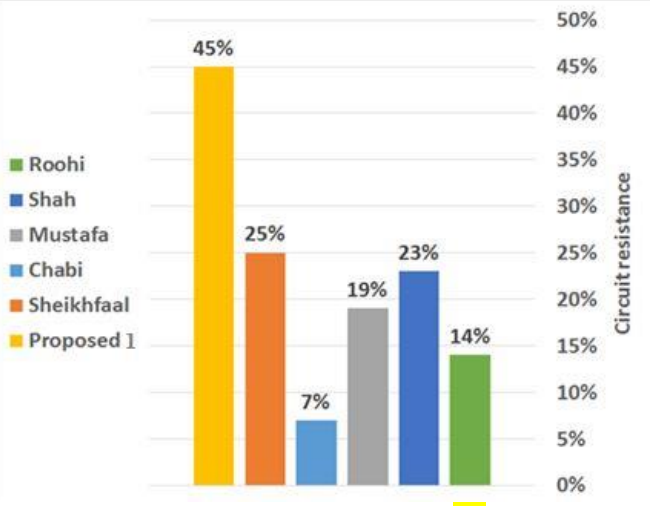

Fig. 8. Evaluation of the tolerance rate of the gates to missing cell defects.

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