Utilization of a Novel Meta Heuristic Algorithm to Minimize Total Harmonic Distortion

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ABSTRACT:
Recently, application of multi-level inverter become more convenient in power electronic. The output of this inverter is close to sinusoidal waveform, it has the capability of creating high value of voltage or current and less blocking voltage on switches. These advantages make the multi-level inverter a popular solution in many power electronic applications. There are several types of multi-level converter including; neutral point diode clamped, fly capacitor, and Cascade H-Bridge (CHB). The CHB inverter are more popular compared to other multi-level inverters; controlling this type of inverter is very simple. A new approach to seven-levels Space Vector Modulation is presented to produce required fundamental voltage in CHB. In addition, the algorithm values were compared with arbitrary values, Cat Swarm Optimization (CSO) is introduced as a new meta heuristic algorithm to minimize Total Harmonic Distortion and to tune switching parameters. The simulation results were carried out using MATLAB/SIMULINK software.

KEYWORDS: Cascade H-Bridge inverter, Space Vector Modulation, Cat Swarm Optimization, Total Harmonic distortion.

1. INTRODUCTION

In order to create output voltage or current in several values, multilevel inverters are used [1]. This kind of inverters has various advantage and disadvantages. High quality output, less block switch blocking voltage and decreasing utilization of transformers are its advantages. Large number of devices, complicate switching methods and high cost of designing are its disadvantages. There are three main types of multilevel inverters: Diode clamped, Inverter-Capacitor clamped, and inverter -cascade inverter.

To combine a multilevel waveform, the AC outputs of each of the different level H-bridge cells are connected in series [2]. The cascade multilevel converter consists of *m* full bridge topology which has been connected series to produce high level voltage. Figure 1 illustrates the schematic diagram of single-phase *m* level cascaded inverter using H-bridge cells and separate DC sources.

As been illustrated, the value of output voltage in each phase is given below:

$$V_o = V_{o1} + V_{o2} + ... + V_{om} \quad (1)$$

Considering the input DC voltage Cascade H-bridge converter is classified into symmetrical and unsymmetrical classes. If all DC voltage source have a same value, it is introduced as symmetrical, otherwise an asymmetrical. Considering *m* number of cells, the converter output voltage level (N) is shown as follow:

$$N = 2 \times m + 1 \quad (2)$$

As found out from equation (2), increasing inverter's level requires a large number of switches.

Utilization of large number of semiconductor devices (switches and diodes) to create output closer to sinusoidal waveform have high cost to designers. To present proper design with tradeoff between cost and quality, authors proposed inverters with a smaller number of devices. In [3] a new topology with reduced number of devices was introduced. Figure 2 Illustrated the basic unit for a sub-multilevel which is proposed by author.

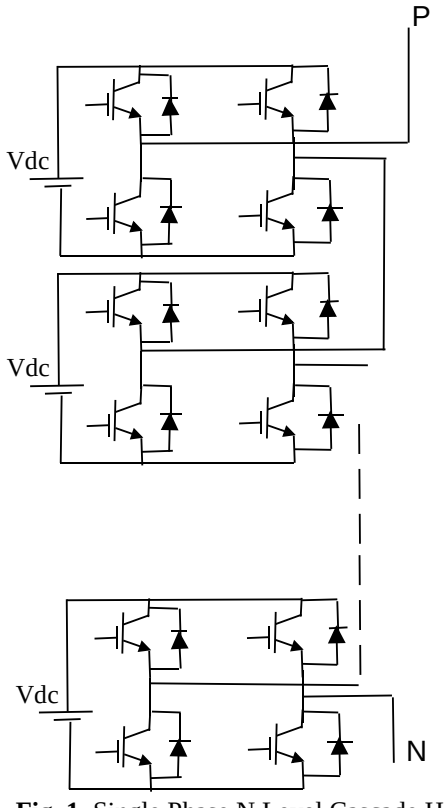

Fig. 1. Single Phase N Level Cascade H-Bridge Inverter.

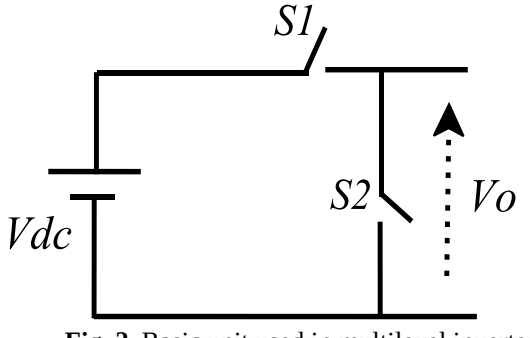

Fig. 2. Basic unit used in multilevel inverter.

Table 1 shows the value of Vo for the feasible state of S1 and S2 switches.

Table 1. Feasible state of switches and their output voltage

State	Switches State		Unit Output Voltage
1	S1	S2	V_{dc}
	1	0	
2	0	1	0

Figure 3 shows the single-phase cascade H-bridge inverter with the proposed base unit.

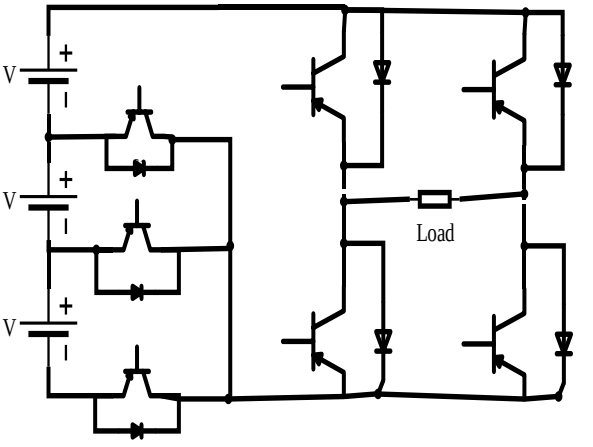

Fig. 3. The single-phase Cascade H-Bridge inverter.

Output voltage for the represented circuit with considering all feasible states of switches was achieved with specifications similar to Figure 4. In this figure all dc voltage sources of each unit are considered with equal values.

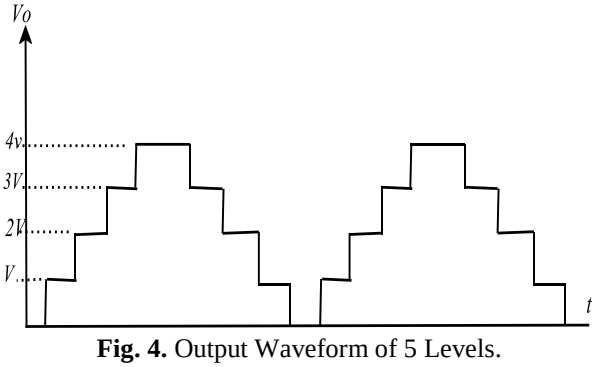

Fig. 4. Output Waveform of 5 Levels.

It could deduce from Figure 4 the wave form for completion need to negative side. it is feasible by adding full bridge topology to the indicated circuit, Figure 5 shows the complete circuit [4].

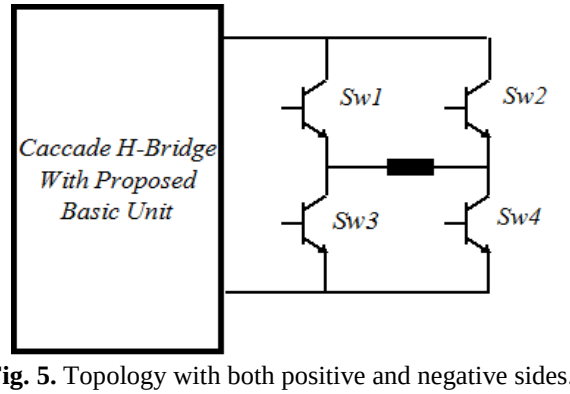

Fig. 5. Topology with both positive and negative sides.

As authors indicate in [3], the needed IGBT's

number in this topology was achieved like below equation [5,6]:

$$N_{step} = m+1$$
$$IGBTS\_Number = 2\times N_{step} - 1 \quad (3)$$

Where:

N_{step} : inverter output levels

m : number of series unit

Figure 6 illustrated the capabilities of the proposed converter in reduction of the number of the switches [7,8].

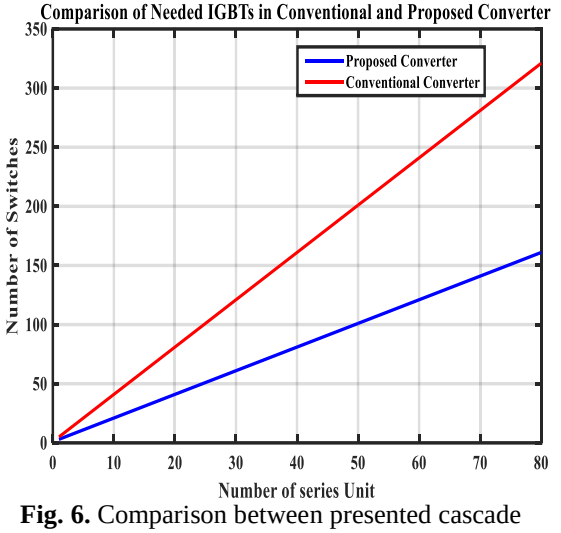

Fig. 6. Comparison between presented cascade multilevel with conventional multilevel inverter.

2. SPACE VECTOR SWITCHING ALGORITHM

There is more kind of switching algorithms including; Sinusoidal pulse width modulation (SPWM), Hysteresis-band current control, and space vector modulation (SVM). All of them have their advantages and disadvantages; they are used in different implementations considering their proper features.

Among all of them, Space vector modulation provides more fundamental outage voltage as compared with other modulation methods. An advantage of the SVM is the instantaneous control of switching states and the freedom for selecting the vectors in order to balance the NP. Space vector modulation is used in three phase voltage source inverters in many applications including induction motors. It provides a constant switching frequency and therefore the switching frequency can be adjusted easily. The determination of the switching instant may be achieved using space vector modulation technique based on the representation of switching vectors in α , β plane.

The concept of space vector is derived from the rotating field of the AC machine which is used for modulating the inverter output voltage. Space vector modulation is used in two levels inverter as demonstrated in many numbers of the literature. However, its application in high-level inverters including three and five levels are difficult because of switching pattern complication.

In next section, space vector modulation for proposed seven levels Cascade H-bridge inverter is described. [9].

3. PULSE GENERATING AND DWELL TIME CALCULATION

As mentioned in previous, in this study, seven space vector is used as switching algorithm. Figure 6 shows the proposed switching algorithm.

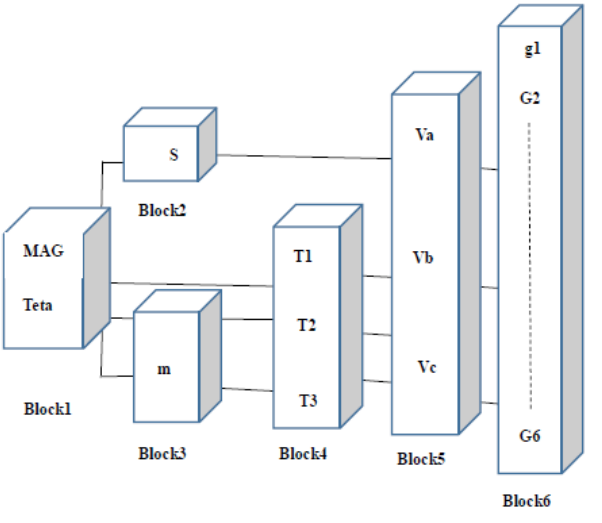

Fig.6. The block diagram of proposed pulse generation method.

At first it is better to describe all blocks in the proposed algorithm. Block 1 decomposes the reference voltage to its magnitude and phase as follow:

$$Mag = \sqrt{V_d^{\,2} + V_q^{\,2}}$$
$$\theta = \tan^{-1}\frac{V_q}{V_d} \quad (4)$$

Block 2 computes each sector of space vector as follow:

$$S = Floor(abs(\frac{\theta}{60})) + 1 \quad (5)$$

Where: θ is phase of reference voltage and *abs* is absolute value.

Parameter m is defined as all the possible states of multilevel inverter. For example, in utilized inverter seven-level inverter, this parameter gets values in range of {-3, -2, -1,0,1,2,3}. For n-level inverter, this parameter is expressed as shown below:

$$\{-(\frac{n-1}{2}),-(\frac{n-1}{2})+1,-(\frac{n-1}{2})+2 ,...,(\frac{n-1}{2})\} \quad (6)$$

Block 4 is represented for calculating dwell time of the space vector. As shown in Figure 7, dwell times were calculated due to reference voltage lying triangular. For example, If the reference vector is lying in $\overset{\Delta}{MNK}$, dwell time is expressed as follow:

$$T_M = (V_{refalpha} - V_{Nalpha}) \times T_s$$
$$T_K = (V_{refbeta} - V_{Nbeta}) \times T_s$$
$$T_N = T_s - T_M - T_K$$

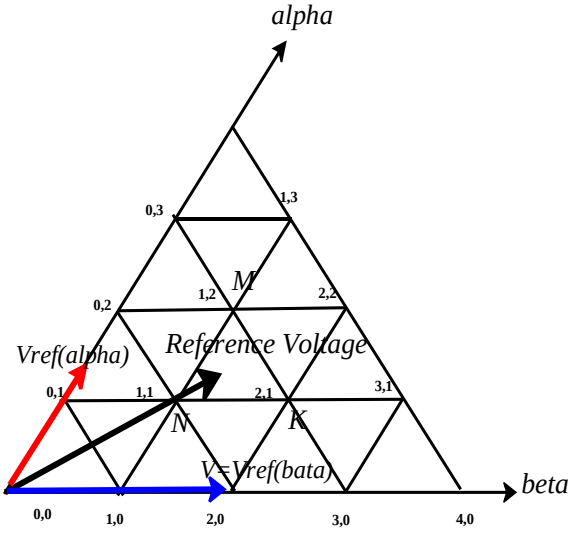

Fig.7. Reference voltage in section (1).

Block 5, is used to create switching states in sections. Table (II) shows these states for each section.

The relationship between space vector and its switching states, is achieved as follow:

$$V_a = -m, -m+1, ..., \mathrm{m}$$
$$\mathrm{V}_b = V_a - alpha$$
$$V_c = V_a - (alpha + beta)$$

Table 2. Switching states in various sectors.

Sector	Switching states			Example Vector
I	V_a	V_b	V_c	[1,-2,-3],[2,-1,-2],[3,0,-1]
II	$-V_b$	$-V_c$	$-V_a$	[2,3,-1],[1,2,-2],[0,1,-3]
III	V_c	V_a	V_b	[-3, 1,-2],[-2,2,-1],[-1,3,0]
IV	$-V_a$	$-V_b$	$-V_c$	[-1,2,3],[-2,1,2],[-3,0,1]
V	V_b	V_c	V_a	[-2,-3,1],[-1,-2,2],[0,-1,3]
VI	$-V_c$	$-V_a$	$-V_b$	[3,-1,2],[2,-2,1],[1,-3,0]

A. CAT SWARM OPTIMIZATION (CSO)

Cat swarm optimization is one of new Meta heuristic algorithm which inspired from cats' behavior. This algorithm consists of two operational modes, known as seeking and tracing modes. Seeking mode, model the cat during a period of resting but being alert. This mode consists of three essential factors which are introduced as follows:

Seeking memory pool (SMP), depicted point which sleeked with cat. Seeking range of selected dimension (SRD) is used to declare the mutative ratio for the selected dimensions. Count of dimension to change (CDC).

The process of seeking mode is described as follow:

Step 1: make j copies of current position of cat_k, where j equal to SMP values. If the value of SPC is true, consider (j=SMP-1).

Step 2: for each copy, according to CDC randomly plus or minus SRD percent the present values and replace the old ones.

Step 3: calculate the fitness values FS of all candidate's point.

Step 4: If all FS are not exactly equal, calculate the selecting probability of each candidate point by equation (2), otherwise set all the selecting probability of each candidate point to 1.

Step 5: Randomly pick the point to move to from the candidate points, and replace the position of Cat_k

$$P_i = \frac{FS_i - FS_b}{FS_{\max} - FS_{\min}} \quad (7)$$

Also, tracing process is described as follow:

Step 1: update the velocity for every dimension $V_{k,d}$

according to equation (3)

Step 2: check if the velocities are in the range of maximum velocity.

Step 3: update the position of Cat_k according to equation (4).

$$V_{k,d} = V_{k,d} + r_1 \times C_1 \times (X_{best,d} - X_{k,d}) \quad where\ d = 1,2,...,m \tag{8}$$

$$X_{k,d} = X_{k,d} + V_{k,d} \tag{9}$$

In this paper, CSO was used for tuning switch pulses in optimal value. Figure 9 shows CSO algorithms flowchart. Objective function (*OF*) in this paper is introduced as reduction of total harmonic distortion (THD). *OF* is expressed by:

$$OF = \int_0^t t \times |THD| dt \tag{10}$$

With setting objective function in minimized value, switches are tuned with best values [13,14,15].

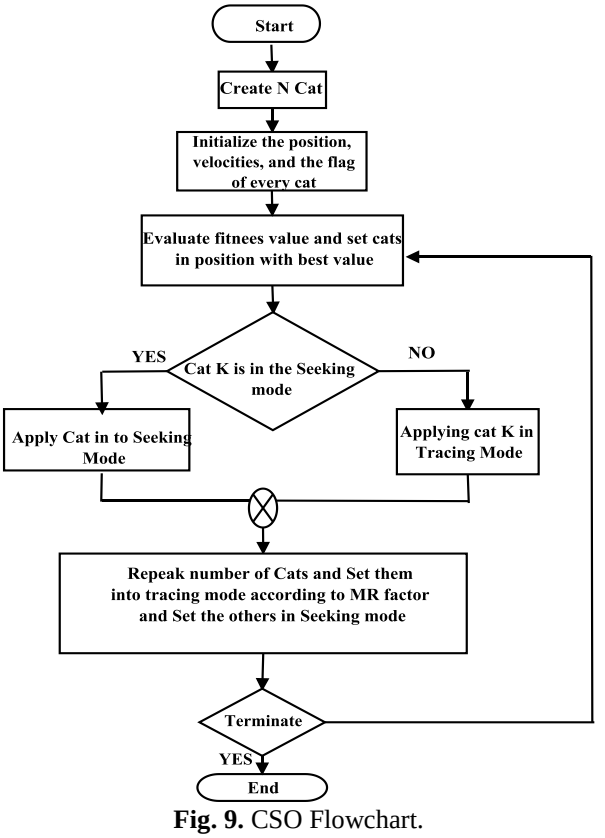

Fig. 9. CSO Flowchart.

B. RESULTS

- Input Data

Parameters of all required devices are illustrated in table (III). Two channel 70 MHz oscilloscope is used as output signal displayer. ATmega2560 AVR is used to program switching method. Due to availability of enough drive, in the experimental work, independent drive is used for each of switches.

Table 3. Input data.

Device	Value
Input voltage	100 v
MOSFET	IRFP450
Gate Drivers	TLP250
R-L Load	100 Ω 10 mH

- Investigation of Simulation Results

In this paper, the main purpose is switching with optimized value. In other words, switching parameters are tuned in best values to minimize total harmonic distortion. As mentioned in previous section, reference voltage angle and magnitude have important role in switching algorithm.

In table 4, angles and size of reference voltage are illustrated with arbitrary value and with optimized value. As seen in table, by adjusting voltage magnitude in 940 V and its phase in 28 degrees, FFT of load voltage achieved 1.67 %.

Table 4. The switching parameters

Optimization Algorithm	Reference voltage value	Reference voltage angle	Value of THD (%)
CSO algorithm	940	28	1.67
Arbitrary value	1010	0	11.57

Figure 10 illustrated output voltage of proposed circuit with arbitrary switching values. The voltage deviation is seen obviously in this figure. Also, the high value of THD could be guessed from this figure. In Figure 11 FFT analyses are shown for respected values. As seen the harmonic in proposed frequency(50Hz) is achieved 11.57%.

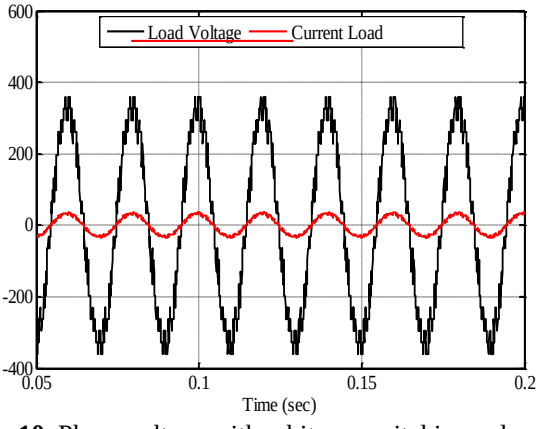

Fig. 10. Phase voltage with arbitrary switching value.

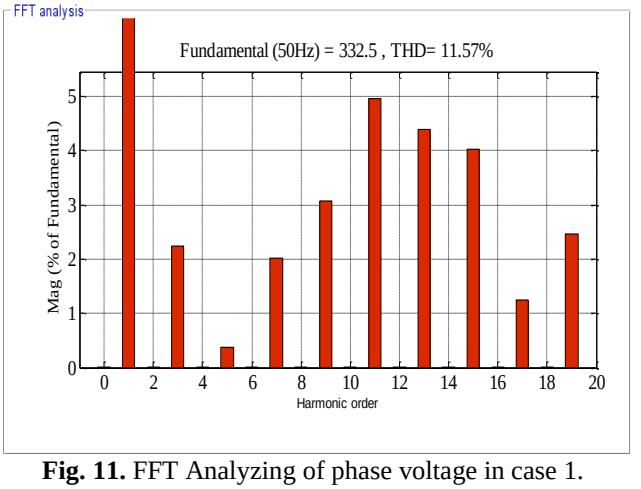

Fig. 11. FFT Analyzing of phase voltage in case 1.

Figure 12 shows output voltage after implementation of the CSO algorithm and adjusting switching parameters (reference voltage in best position). As it could be seen from the figure, it is so close to sinusoidal waveform and will reduce the THD [16,17,18].

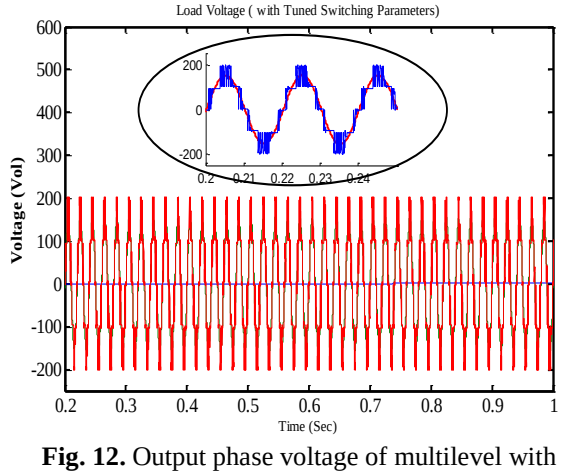

Fig. 12. Output phase voltage of multilevel with optimized tuned switching parameters.

FFT analysis in second condition is shown in Figure 13. It is clear magnitude of fundamental harmonic in optimized condition, is reduced to 1.67%. [19,20].

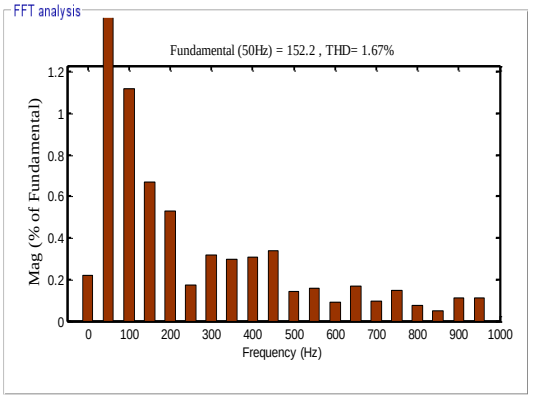

Fig. 13. FFT analyzing of voltage in case 2

D. Experimental Results

In order to validate proposed method, experimental approach is investigated in this section. Value of each input dc voltage source is adjusted in 25 volts. Output voltage of single phase is shown in Figure 14. In addition, Figure 15 shows experimental view of proposed topology. The output of single phase 7 levels inverter is 150 volts.

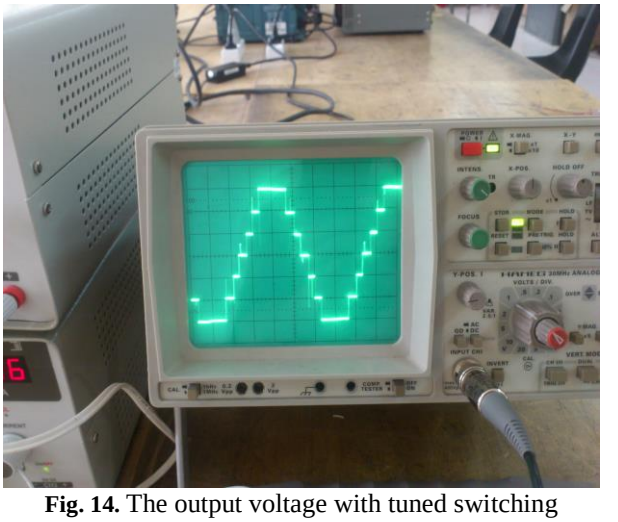

Fig. 14. The output voltage with tuned switching parameters.

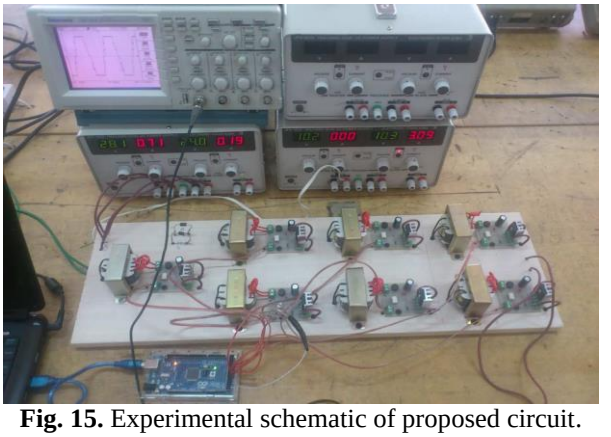

Fig. 15. Experimental schematic of proposed circuit.

4. CONCLUSION

Designing Multilevel inverter with reduced number of switches is one of the main purposes for designers. In these inverters to have output with minimum harmonic, in addition to using proper switching method, adjusting switching parameters in best value is main purpose. Meta heuristic algorithms were designed to fined best solution to optimization issues. In this paper cat swarm optimization (CSO) algorithm was used as a new metaheuristic algorithm to find tune switching parameters. Results verified CSO application in optimizing problems. As seen from the results, by using CSO algorithm, the value of THD was decreased from 11.57% to 1.67%. This improvement in THD value, verifies the impacts of switching values tuning in SVM.

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