Four-Leg VSI Based DSTATCOM for Compensating Nonlinear and Unbalanced Loads

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ABSTRACT:
This paper presents a study on the four-leg VSI based distribution static compensator (D-STATCOM) for compensation of neutral, source & PCC current harmonic distortion, PCC voltage regulation and compensation of unbalanced in current waveform. This solution could be used for three-phase four-wire nonlinear and unbalanced load medium voltage distribution system. The proposed control algorithm is developed based on synchronous reference frame theory with the PI controller. The obtained reference current signal from control algorithm is compared in hysteresis band current controller for a better switching of the D-STATCOM. The performance of the system with implementing the D-STATCOM is also analyzed and compared. The proposed control method is implemented on 11/0.4kv medium voltage distribution system and provided effective compensation for reactive power and harmonic distortion mitigation. The simulation results are obtained using MATLAB/SIMULINK.

KEYWORDS: Distribution Static Compensator (D-STATCOM), Synchronous Reference Frame (SRF) Theory, PI Controller, Voltage Source Inverter (VSI), Hysteresis Current Controller, Harmonic Distortion.

1. INTRODUCTION

In last one decade, power electronic devices are widely used in industrial applications for transferring power in more efficient way [1-3]. The excessive use of power electronic equipments, which represent nonlinear loads, in a distribution network has caused many disturbances in the quality of power such as harmonic pollutions and reactive power problems. As a result, poor power factor, weakening efficiency, overheating of motors and transformers, malfunction of sensitive devices, etc. occur [4-5]. Another power quality problem is the use of single- or three-phase unbalanced and nonlinear loads which causes excess current flowing through neutral wire. In addition, other power quality problems cause excess overload on the neutral wire [6]. The unbalanced in source voltage is also occurred due to unbalanced load. The unbalanced source voltage may generate the lower order harmonic component in the power system and also cause a negative sequence current and torque reduction in case of electric machine drive system [7, 8]. These power quality problems are addressed using custom power devices such as distribution static compensators (DSTATCOM), dynamic voltage restorer (DVR) and unified power quality conditioner (UPQC). In which the distribution static compensators are more suitable for reactive power compensation and harmonic current mitigation in the distribution network compared to other custom power devices [9]. The DSTATCOM operates in two modes such as transformer-based topology and inverter-based topology. In the transformer-based topology, DSTATCOM includes three-leg VSI combined with zig-zag transformer [10] or T-connected transformer [11] or star-delta transformer, etc. In this scheme, the zero sequence component of current is eliminated using transformer and the positive and negative component of current is compensated using three-leg VSIs. In inverter-based topology, DSTATCOM includes three single phases VSI [12], four-leg VSI [13, 14], three-leg VSI with split phase capacitor [15], and three-leg VSI with neutral terminal at the positive or negative of dc bus [16]. From the mentioned methods, most popularly for nonlinear and unbalanced loads current compensation, the three leg VSI with split phase capacitor or the four-leg VSI are used. The split phase capacitor method requires large dc link capacitor voltages because it handles neutral current directly. Another drawback of voltage unbalance across each dc link capacitor is that, it increases stress over semiconductor switches [17, 18]. These problems can be solved by using four-leg VSI. In this paper four-leg VSI based DSTATCOM

topology is used for better neutral and source current compensation as compared to the split phase capacitor method. The performance of four-leg VSI depends on the implemented control strategy. In this paper, SRF Theory with the Proportional Integral (PI) controller technique is used. The tuning of the PI controller is done via the Ziegler-Nichols method. Many authors have proposed and implemented different control algorithms on 400v distribution systems. In practical applications the distribution system is stepped down to 400v using 11/0.4 kv three phase transformer. By connecting DSTATCOM at the PCC harmonic and reactive power is compensated due to linear/nonlinear and balanced/unbalanced loads. In the above proposed method, the effect of transformer (11/0.4kv) is not taken into consideration. In this paper, 11/0.4kv distribution transformer is considered. The harmonic and reactive power compensation before and after transformer is considered and analyzed.

In this paper, SRF theory controlled four-leg VSI DSTATCOM is proposed and implemented on 11/0.4kv distribution system. The performance of the proposed DSTATCOM is analyzed under nonlinear and unbalanced loads conditions in terms of harmonic mitigation, neutral current compensation and voltage regulation at the PCC. The proposed results are validated using MATLAB/SIMULINK software. The paper is organised as follows; section 2 presents system configuration, section 3 represents control strategy, section 4 gives the results & discussion, finally section-5 gives conclusions.

2. SYSTEM CONFIGURATION

Fig.1 shows the system configuration of proposed Distribution static compensator (D-STATCOM) for the three phase four wire distribution system with nonlinear and unbalanced loads. Three phase source voltage of 11kv is stepped down to 400V by using 11/0.4Kv three phase distribution transformers and connected to nonlinear and unbalanced loads. The connected unbalanced nonlinear load introduces harmonic at the PCC. By Connecting DSTATCOM at the PCC, the unbalanced at the PCC and in load voltage wave form is eliminated and also current harmonics are mitigated. The DSTATCOM consist of four-leg voltage source inverter with interface inductor (L_f). Here the dc link capacitor (Cdc) and voltage across the capacitor is Vdc selected as 1.6 times the peak value of the source voltage [19]. The four-leg VSI consists eight IGBT switches. In six IGBTs, switches are used for compensating harmonics and unbalanced in current wave and remaining two IGBTs switches are used for neutral current compensation. The nonlinear load consists of three phase bridge rectifier with R-L load. The fourth leg provides effective neutral current compensation compared to the split phase capacitor method. The unbalanced load consists of three phase loads having three different magnitudes of resistance and inductance values. The rating of the transformer kept 20kva. Here the capacitor filter (cf) is used for eliminating harmonic in voltage wave form. The main advantage of the proposed model is that the requirements of filters are eliminated.

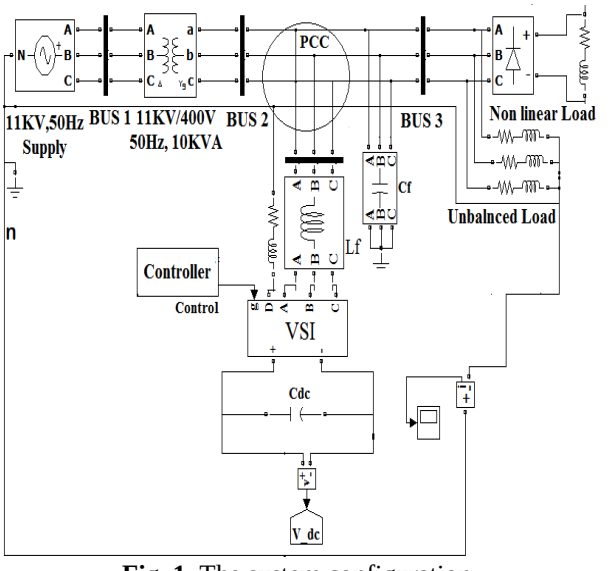


Fig. 1. The system configuration.

3. CONTROL STRATEGY

The block diagram of the proposed SRF control algorithm is shown in Fig 2. The control algorithm is used for extracting the fundamental reference control signals to switching of VSI based DSTATCOM for harmonic and reactive power compensation during unbalanced nonlinear load condition.

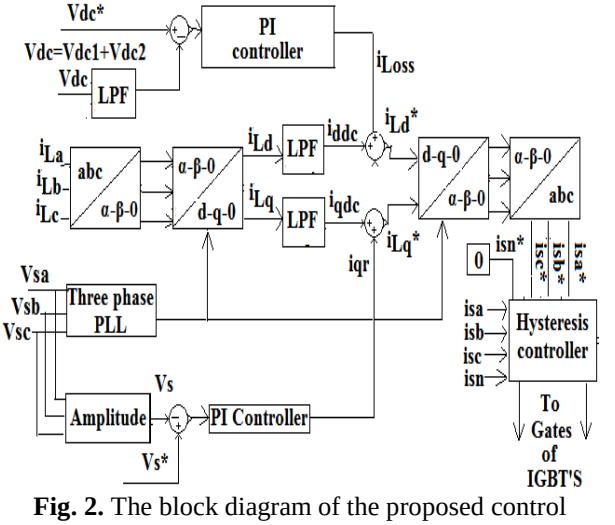


Fig. 2. The block diagram of the proposed control algorithm.

The nonlinear load currents consist of active, reactive and harmonic current in three phase system. In this, the reactive and harmonic components of currents are separated, for compensation. The separation includes converting the instantaneous three phase load currents into two phase stationary α-β-0 axis using Clark's transformation equation given in eq. (1).

$$\begin{bmatrix} i_{L0} \\ i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (1)$$

The stationery α-β-0 current axis components are transformed into d-q-0 (d-direct axis, q-quadrature axis components) rotating reference frame by using below park transformation equation.

$$\begin{bmatrix} i_{L0} \\ i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & \sin\theta \\ 0 & -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{L0} \\ i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \quad (2)$$

Here the θ is the transformation angle. The cosθ and sinθ is obtained from the three phase PLL block (phase locked loop) of voltage source for synchronization of voltage and current. The obtained i_{Ld} and i_{Lq} current components are called instantaneous active and reactive load current components. Each current component has an average value (dc component) and oscillating value (ac component) as given in equation (3) & (4).

$$i_{Ld}=i_{ddc}+i_{dac} \quad (3)$$
$$i_{Lq}=i_{qdc}+i_{qac} \quad (4)$$

Where, $i_{d\ dc}$ and $i_{q\ dc}$ are the average or dc component of i_{Ld} and, $i_{d\ ac}$ and $i_{q\ ac}$ are the oscillating or ac component of i_{Lq}.

The oscillatory component (harmonic) appears like ripples. After eliminating the oscillatory current component by using Low pass filter, the average active and reactive current components are given in Equation (5) & (6).

$$i_{Ld}=i_{ddc} \quad (5)$$
$$i_{Lq}=i_{qdc} \quad (6)$$

In order to maintain the constant DC link voltage and to supply the losses in DSTATCOM, the output current of the PI controller is considered as loss current component, (i_{Loss}) is added to the average active reference current component of d-axis in d-q frame. Then the active reference current component is

$$i_{Ld}{}^{*}=i_{ddc}+i_{loss} \quad (7)$$

The loss reference component of current (i_{LOSS}) is extracted, by comparing the reference dc bus voltage $V_{dc*}$with the actual dc bus voltage V_{dc}($V_{dc}=V_{dc1}+V_{dc2}$) of VSI at the n^{th} sampling instant

$$V_{de(n)}= V_{dc*(n)} - V_{dc(n)} \quad (8)$$

The compared error signal $V_{de(n)}$ is processed through a PI controller to compute the loss component (i_{Loss}) at n^{th} sampling instant, as follows below;

$$i_{Loss(n)}=i_{loss(n-1)} + k_{pd}\,(V_{de(n)} - V_{de(n-1)})+k_{id}\,V_{de(n)} \quad (9)$$

Here the k_{pd} and k_{id} are the proportional and integral gains of PI controller. The output of the PI controller is the loss reference component (i_{Loss}) of the DSTSTCOM. The loss reference current component (i_{loss}) is added to the average active reference component (i_{Ld}) for regulating the active reference component of the current (i_{Ld*}).

The direct axis reference current component (i_{Ld}*) is used for compensation of harmonic and power factor. Similarly for regulating the voltage at the PCC, the source must need to deliver the reactive current (i_{qr}) , to be added to the average reactive reference component of current ($i_{q\ dc}$) of q-axis in d-q frame same as direct current axis component. Then the resultant reactive reference current component is

$$i_{Lq}{}^{*}=i_{qdc}+i_{qr} \quad (10)$$

The reactive current (i_{qr}) is obtained from the PI controller output, the input to the PI controller is obtained by subtracting the voltage amplitude Vs from the reference voltage Vs* and is fed to PI controller. Here the amplitude of the PCC voltage is given as

$$Vs = \sqrt{{}^{2}/_{3}\,(V_{sa}^{2} + V_{sb}^{2} + V_{sc}^{2})} \quad (11)$$

The PI controller output is given as

$$V_{qr(n)}=V_{qr(n-1)}+K_{pq}(V_{te(n)}-V_{te(n-1)})+K_{iq}V_{te(n)} \quad (12)$$

Where $V_{te(n)}$ $=V^{*}_{s}-V_{s(n)}$ is the error between the reference (V^{*}_{s}) and actual(V_s) terminal voltage amplitude at the nth sampling instant. Here K_{pq} and K_{iq} are the proportional and the integral gains of the PI controller. The reactive reference current component (i_{Lq}*) is used for ac voltage regulation and compensation of load reactive power.

The Active and reactive reference current component (i_{Ld}*, i_{Lq}*) are transformed in to α-β-0 frame obtained by using inverse park's Equation (13).

$$\begin{bmatrix} i_{s0}^{*} \\ i_{s\alpha}^{*} \\ i_{s\beta}^{*} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & -\sin\theta \\ 0 & \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{L0}^{*} \\ i_{Ld}^{*} \\ i_{Lq}^{*} \end{bmatrix} \quad (13)$$

The reference currents from the Inverse Park's are transformed into three phase reference current (a-b-c) by using inverse Clark's Equation (14).

$$\begin{bmatrix} i_{sa}^{*} \\ i_{sb}^{*} \\ i_{sc}^{*} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 0 & 1 & 0 \\ 0 & -1/2 & \sqrt{3}/2 \\ 0 & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{s0}^{*} \\ i_{s\alpha}^{*} \\ i_{s\beta}^{*} \end{bmatrix} \quad (14)$$

The obtained three phase reference currents (i_{sa}*, i_{sb}*, i_{sc}*) are compared with the actual compensating filter currents (i_{sa}, i_{sb}, i_{sc}) in hysteresis band controller for better switching of VSI of IGBT's. The main advantage of this hysteresis band controller is that it's easy implementation, better stability, faster response as compared to the other controller like carrier based, bead beat and feed forward etc. [20].

The neutral current compensation is obtained using fourth leg VSI. The gate switching of reaming two IGBTs of fourth leg VSI is obtained by comparing the reference neutral current (i_{sn}*) with actual compensating neutral current (i_{sn}) in hysteresis band controller.

$$I_{sn}=-(i_{sa}+i_{sb}+i_{sc}) \quad (15)$$

$$i_{sn}^{*}=0 \quad (16)$$

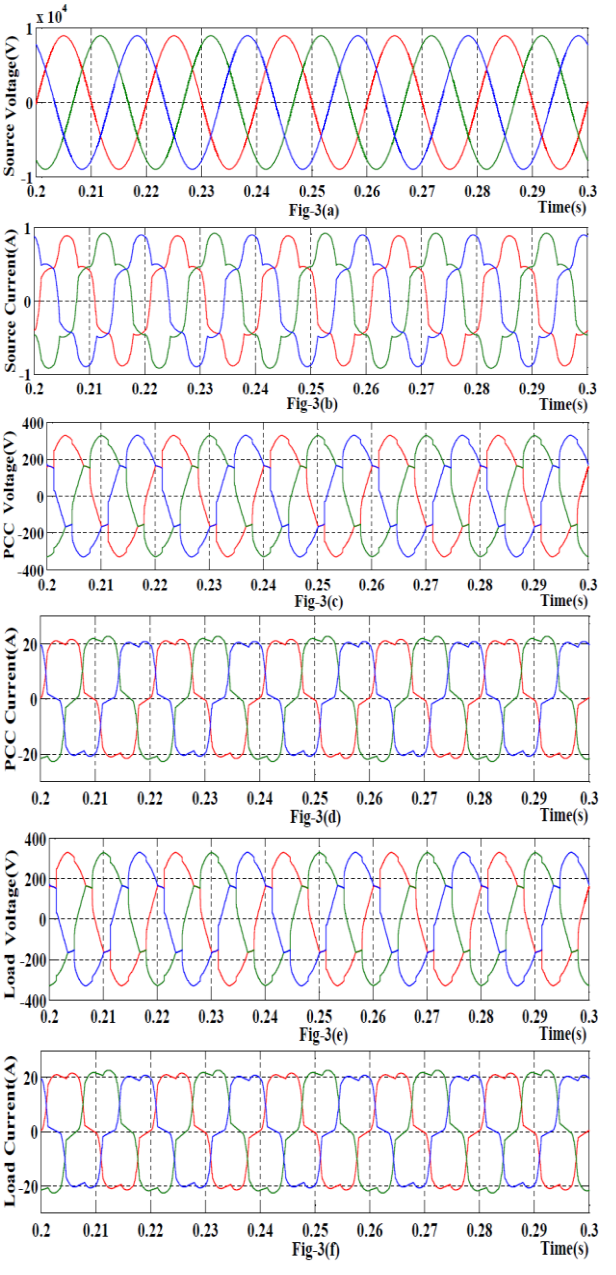
4. RESULTS AND DISCUSSION

The proposed four-leg VSI based DSTATCOM model is implemented in MATLAB/SIMULINK software by using synchronous reference frame control algorithm with PI controller. The model is verified under nonlinear and unbalanced load condition. The proposed model is used for unbalanced compensation, harmonic mitigation, power factor correction at the PCC. The simulation period is taken from 0.2s to 0.3s for the better observation. The A, B, C Phase wave forms are indicated by red, green, blue lines. Neutral wave form is indicated by black line. The performance of DSTATCOM is observed for the following cases:

- Nonlinear and unbalanced without DSTATCOM
- DSTATCOM with PI Controller
- Neutral current compensation
- Power factor improvement
- Reactive power compensation
- THD analysis.

4.1. Nonlinear & Unbalanced without DSTATCOM

When nonlinear & unbalanced load is connected to the proposed distribution system, it causes harmonics and unbalanced in source current (Bus-1) as shown in Fig 3(b). The nonlinear & unbalanced load also introduces harmonics at the PCC voltage & current wave form (bus-2).is shown in Figs 3(c) &3(d). The harmonics current effects the loads connected the PCC. Figs 3(e) & 3(f) shows the load voltage and load current. Fig 3(g) shows the phase current of Phase-A at the PCC.



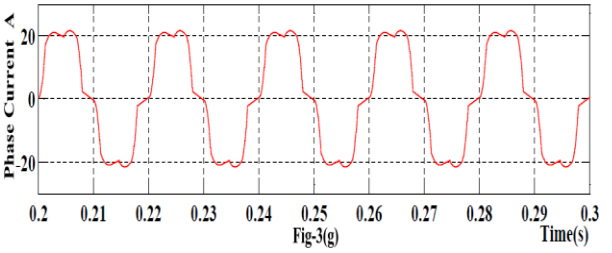
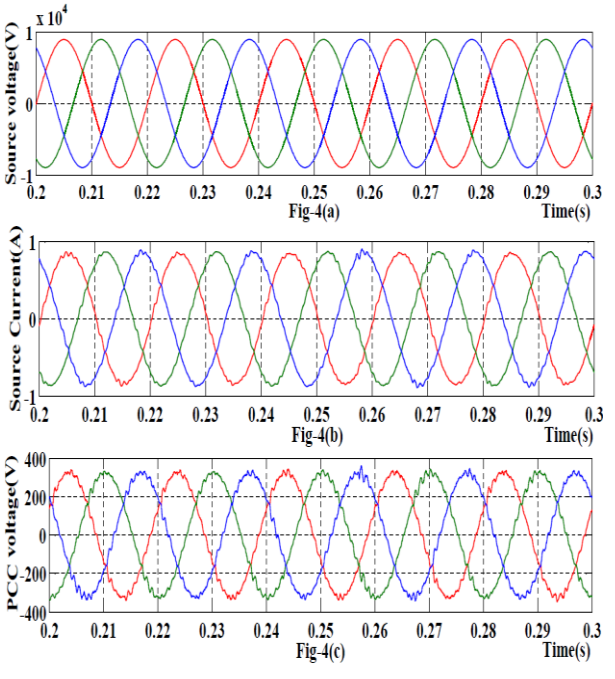


Fig. 3. (a)Source voltage wave form, (b). Source current wave form, (c). voltage waveform at the PCC (Bus-2), (d). Current waveform at the PCC (Bus-2), (e).Load voltage wave form, (f).Load current wave form, (g). Phase current wave form –A at the PCC, during unbalanced nonlinear load without D-STATCOM.

4.2. DSTATCOM with PI Controller

When SRF controlled D-STATCOM is connected at the PCC, the D-STATCOM is injecting the required amount of reactive power for compensation of source and PCC current harmonics and unbalanced in the waveform also. The DC-link voltage is regulated by implementing the PI controller. The compensated source current waveforms are shown in Fig 4(b). Figures 4(c) and 4(d) show the compensated voltage and current waveform at the PCC. Load voltage and current waveform is shown in Fig 4(e) and 4(f). Phase current waveform Phase-A at the PCC is shown in Fig4 (g). The DC-link voltage (Vdc=Vdc1+Vdc2) wave form is shown in Fig 4(h). The compensating filter currents are shown in Fig 4(i).



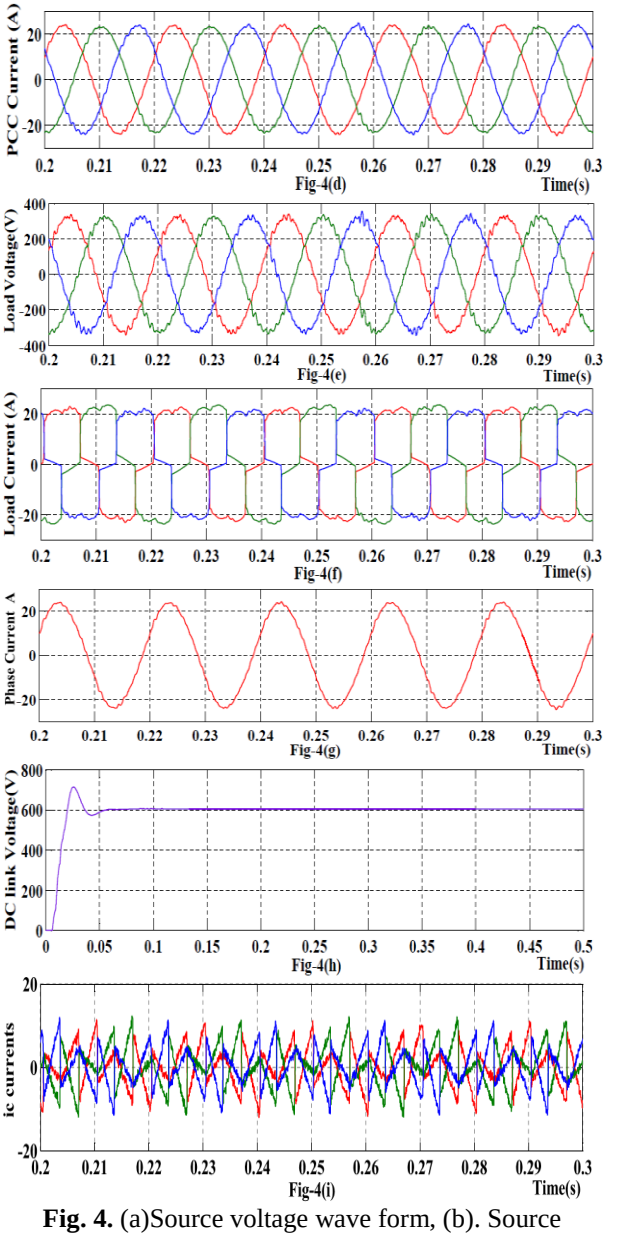


Fig. 4. (a)Source voltage wave form, (b). Source current wave form, (c). voltage waveform at the PCC (Bus-2), (d). Current waveform at the PCC (Bus-2), (e). Load voltage wave form, (g). Phase current wave form of phase-A. at the PCC (h). DC-link voltage form (Vdc), (i) compensating filter currents, with PI controlled D-STATCOM.

4.3. Neutral Current Compensation

The unbalanced loads cause current flowing through the neutral wire. The current flowing through neutral wire during unbalanced load condition is observed as shown in Fig 5(a). By providing appropriate control algorithm with four leg VSI current in supply neutral wire is compensated and is observed as shown in Fig 5(b), with four-leg VSI, which

provides effective compensation for the both neutral current and line currents of the proposed system.

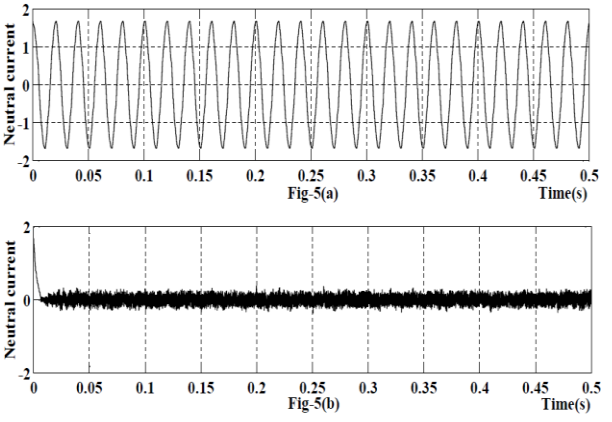


Fig. 5. (a). Neutral current wave form without compensation, (b). Neutral current wave form after compensation.

4.4. Power Factor Improvement

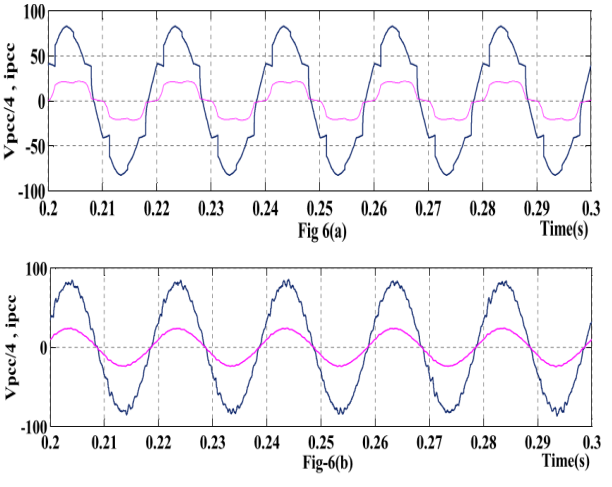


Fig. 6. (a). Voltage and current wave form without compensation, (b). Voltage and current wave form after compensation, R-phase.

Figs 6(a) and 6(b) show that voltage and current waveform of R-phase without and with DSTATCOM for observation of improvement in power factor. The power factor improvement with and without DSTATCOM can be observed from the Table-1.

Table 1. Power factor improvement analysis.

Corresponding BUS	Without DSTATCOM	With DSTATCOM
BUS-1(SOURCE)	0.9514	0.9971
BUS-2 (PCC)	0.9754	0.9998
BUS-3 (Load)	0.9754	0.995

From the Table 1, It is observed that by connecting DSTATCOM at the PCC, power factor is improved at the source side (BUS-1) as well as at the PCC (BUS-2).

4.5. Reactive Power Compensation

The amount of active and reactive power, are transferred from the source to load without compensating device as shown in Fig 7. The Figs 7(a) and 7(b) show the active and reactive power supplied by source. The required load active and reactive power are shown in the Figs 7(c) and 7(d). The compensating device will not inject any active & reactive power to the load.

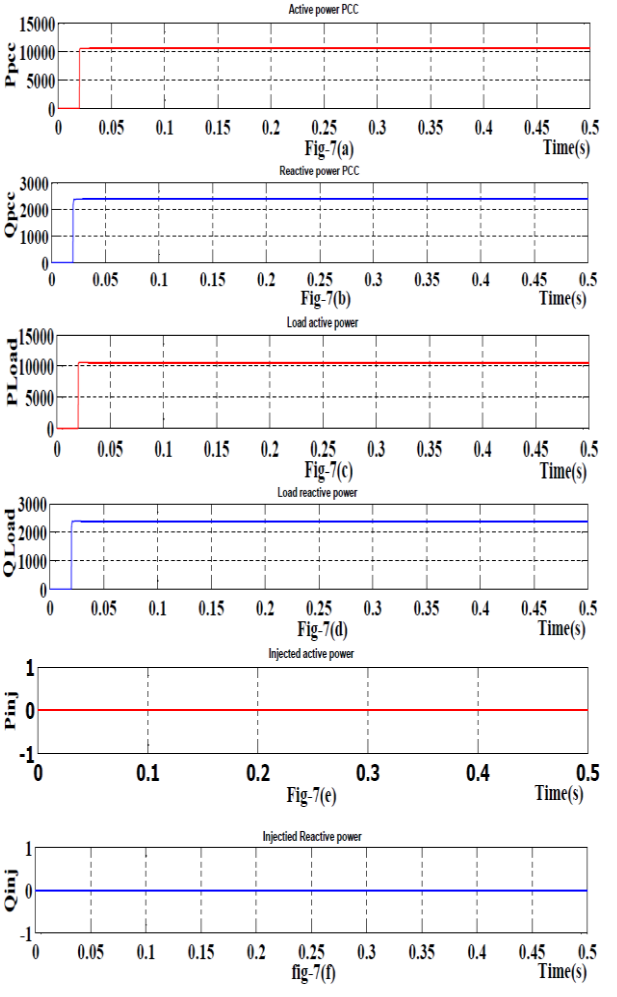


Fig. 7. (a).Source active power, (b). Source reactive power, (c). Load active power (d). Load reactive power, (e). Injected active power, (e). Injected reactive power, without D-STATCOM.

When the DSTATCOM is connected to the proposed system at the PCC. The required amount of reactive power to the load is supplied from the DSTATCOM and the source is not supplying any reactive power which is observed from the Fig 8. The

Figs 8(a) and 8(b) show the active and reactive power supplied by source. The load active and reactive power are shown in Figs 8(c) and 8(d). The injected active and reactive power DSTATCOM at the PCC are shown in Figs 8(e) and 8(f).

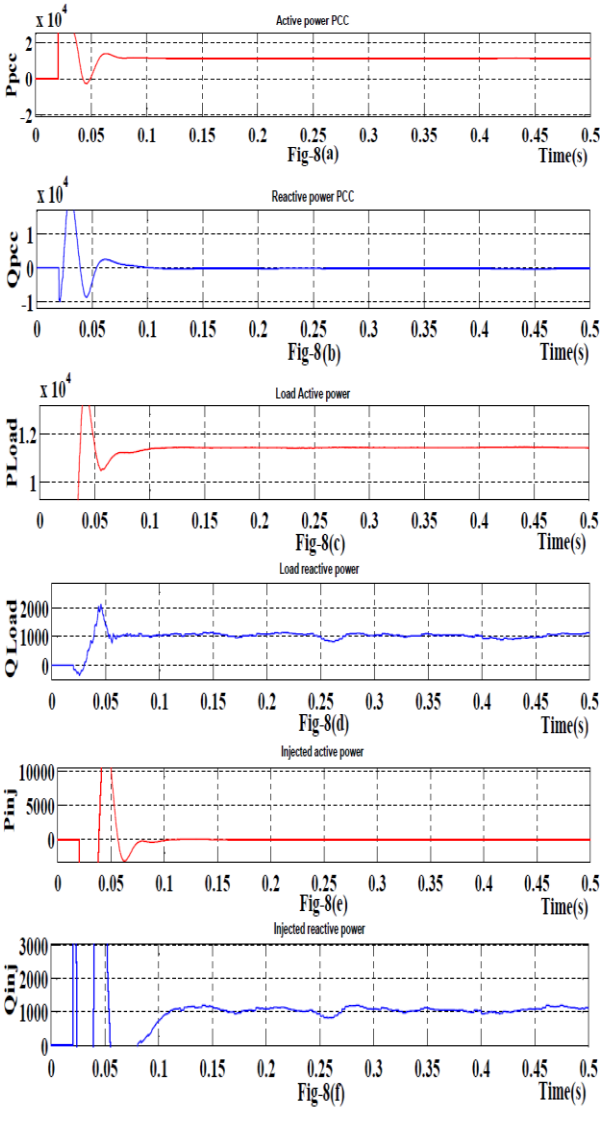


Fig. 8. (a) Active power at the PCC Bus, Fig-(b). the reactive power at the PCC Bus. Fig-(c). Active power at the Load Bus, Fig-(d). the reactive power at the Load Bus. Fig-(e). Injected active power, Fig-(f) . the Injected reactive power.

4.6. Total Harmonic Distortion analysis

The total harmonic distortion of the PCC and source currents wave forms for the proposed system with and without DSTATCOM is discussed here.

a. Nonlinear & unbalanced load without DSTATCOM

The total harmonic distortion of the system by connecting nonlinear and unbalanced load without DSTATCOM is shown in Fig 9. The Current harmonic distortion at the PCC (BUS-2) is observed 19.16% as shown in Fig 9(a). The source current harmonic distortion is 19.32% as shown in Figure 9(b).

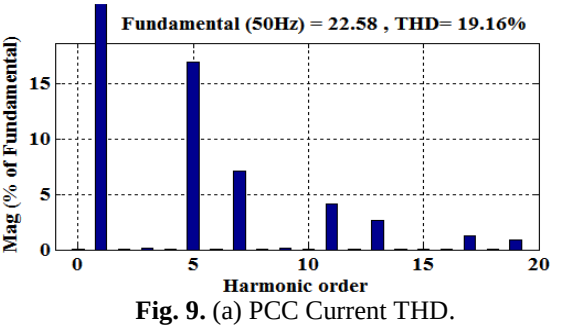


Fig. 9. (a) PCC Current THD.

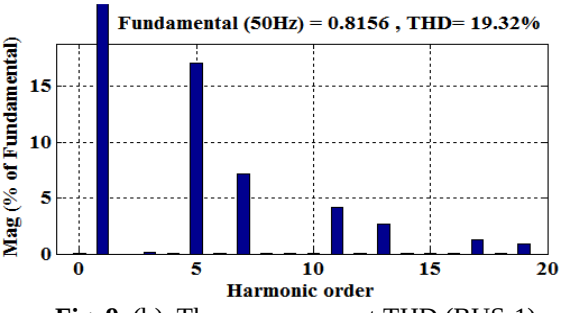


Fig .9. (b). The source current THD (BUS-1).

b. DSTATCOM with PI Controller

BY Connecting DSTATCOM to the proposed system, the current harmonics distortion at the PCC (BUS-2) is reduced to 2.43% as shown in Fig 10 (a). The source current harmonic distortion is reduced to 2.02%, as shown in Fig 10 (b).

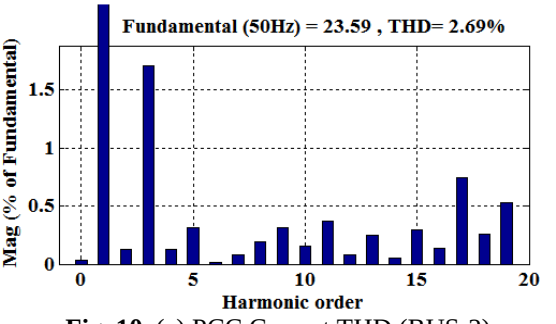


Fig. 10. (a) PCC Current THD (BUS-2).

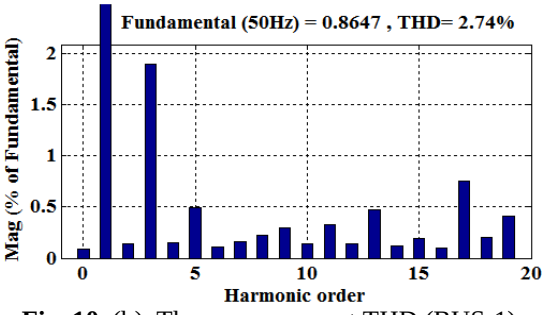


Fig. 10. (b). The source current THD (BUS-1).

Table 2. The THD analysis.

Without DSTSTCOM	i_{Sa}	THD	i_{Sb}	THD	i_{Sc}	THD
	0.82	19.3	0.850	18.44	0.82	19.0
	$V_{pcc\ a}$	THD	$V_{pcc\ b}$	THD	$V_{pcc\ c}$	THD
	319	11.33	317.2	11.48	318.1	11.8
	$I_{pcc\ a}$	THD	$I_{pcc\ b}$	THD	$I_{pcc\ c}$	THD
	22.6	19.16	23.7	18.18	21.8	19.9
	V_{La}	THD	V_{Lb}	THD	V_{Lc}	THD
	319	11.33	317.2	11.48	318.1	11.8
With DSTATCOM	i_{Sa}	THD	i_{Sb}	THD	i_{Sc}	THD
	0.87	2.74	0.85	2.38	0.85	2.27
	$V_{pcc\ a}$	THD	$V_{pcc\ b}$	THD	$V_{pcc\ c}$	THD
	325	4.24	325	4.00	325	3.63
	$I_{pcc\ a}$	THD	$I_{pcc\ b}$	THD	$I_{pcc\ c}$	THD
	23.6	2.69	23.4	2.19	23.4	2.58
	V_{La}	THD	V_{Lb}	THD	V_{Lc}	THD
	325	4.24.	325	4.00	325	3.63

Total harmonic distortion analysis of without and with DSTATCOM for each phase is observed form the Table 2.

5. CONCLUSION

In this paper, the performance of four-leg VSI based DSTATCOM has been analyzed and implemented using synchronous reference frame control algorithm. The four-leg inverter provided better neutral, PCC current compensation compared to other inverter topology performance, and it also reduces the requirements of filters. The dc bus voltage is maintained constant under all disturbance conditions by using PI controller. The control logarithm is simple and provided better compensation for reactive power, harmonic, neutral current, unbalanced in currents and voltage regulation at the PCC in three phase three wire nonlinear and unbalanced load distribution system. The proposed control algorithm on the 11/0.4kv distribution system model is working satisfactory and provided better harmonic compensation at the PCC and source side. The simulation results are obtained using MATLAB/SIMULINK software.

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