A Wide Tuning Range and Low Phase Noise VCO using New Capacitor Bank Structure

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ABSTRACT:
This paper presents a wide tuning range, and low noise voltage controlled oscillator (VCO) based on cross-coupled and colpitts structures. The advantages of this work provide a low-phase noise and robust start-up condition, leading to minimized the dc power. In addition, a new structure of the capacitor bank is used in this structure to achieve a wide range of frequency. The proposed circuit is simulated in 0.18 µm CMOS process. The designed VCO covers the frequency range of 21.95 GHz to 24 GHz with a tuning range of 8.9%. Simulation results show that the phase noise is -120.5 dBc/Hz at 1MHz offset frequency for 23GHz carrier frequency. Also, power consumption of the VCO is 6.34 mW under 1.8 supply voltage, and the figure-of-merit is -191.68 dBc/Hz.

KEYWORDS: Voltage Controlled Oscillator, Capacitor Bank, Low Noise, Wide Tuning.

1. INTRODUCTION

VCOs are one of the main parts of the transceiver systems [1-6]. They are used to generate the alternative signal in order to cover a frequency range. Phase noise, dc power, start-up condition and tuning range are the most important parameters of VCOs. To design VCOs, there is a tradeoff between these parameters. Tuning range is an important parameter because it is used more in broadband wireless applications such as ultra-wideband communication and radar sensor that operate over a high frequency range [7].

cross-coupled pair and Colpitts structures are two common types of oscillators in RF systems [8-11]. Due to their simple configuration and good performance, these VCOs are widely used. Colpitts VCOs consume low dc power but suffer from poor phase noise and difficult start-up condition [7]. cross-coupled VCOs have better phase noise and start-up condition than Colpitts VCOs [7, 12]. In addition to the NMOS cross-coupled pair, a PMOS cross-coupled pair is used to enhance transconductance and swing [7, 13]. Also, it provides oscillation condition with low power consumption.

Several reconfigurable low power and low phase noise VCOs have been presented in [8-15]. In [8] a VCO with differential varactors was presented, but it suffers from poor phase noise and low tuning range. Ref. [15] proposed a VCO with low phase noise at high frequency but its dc power consumption was high. Also, in [10] a low power VCO was presented where its start-up condition had been improved but its tuning range was low.

In this paper a combination of PMOS and NMOS cross-coupled pairs and Colpitts structures was used to achieve better start-up condition and low noise performance, leading to minimized dc power consumption. Moreover, a new capacitor bank structure was added to increase the tuning range of this VCO. The VCO was designed and simulated in TSMC 0.18 µm CMOS.

The remainder of this paper is organized as follows: the proposed VCO is introduced in Section 2. The simulation results are presented and compared with the results of prior works in Section 3. Finally, the conclusion is provided in Section 4.

2. PROPOSED VCO

The circuit topology of the traditional differential VCO which consists of Colpitts and cross-coupled pair structures is shown in Fig. 1. In this structure, transistors $M_{1\text{-}4}$, C_1, and $C_2/2$ were used to provide the negative conductance [14]. Despite this, VCO has low phase noise but it requires a high supply voltage that results in more power consumption. Specially to operate at high

frequency, it consumes more current to provide the start-up condition. To overcome the problem of this VCO, a new technique was presented in this paper as illustrated in Fig. 2. In proposed VCO, using two inductors between the cross-coupled pair and Colpitts structures increased the negative conductance. Also, in this VCO a PMOS pair was located on top of the Colpitts structure to provide better start-up condition with good phase noise performance. Thus, in the proposed VCO the oscillation condition was provided without increasing its power consumption. Moreover, two capacitor banks were added at the top and bottom of the Colpitts structure to achieve wide tuning frequency range. The design considerations of the proposed VCO was presented as follows.

2.1. Transistors Size

The first step in designing of a VCO is to obtain the size of the transistor. To determine the size of the transistor, their currents that provide sufficient transconductance gain should be considered. The size of NMOS and PMOS transistors are defined as follows [16]:

$$\left(\frac{W}{L}\right)_n = \frac{2I_D}{\mu_n C_{ox}\left(V_{GS} - V_{th_n}\right)^2} \quad (1)$$

$$\left(\frac{W}{L}\right)_p = \frac{2I_D}{\mu_p C_{ox}\left(V_{GS} - V_{th_p}\right)^2} \quad (2)$$

Where $\left(\frac{W}{L}\right)_n$ and $\left(\frac{W}{L}\right)_p$ are the size of NMOS and PMOS transistors, I_D is drained current, μ_n and μ_p are the electrons and holes mobility's, V_{th_n} and V_{th_p} are the threshold voltages of NMOS and PMOS transistors, C_{ox} and V_{GS} are the silicon dioxide capacitor and Gate-Source voltage.

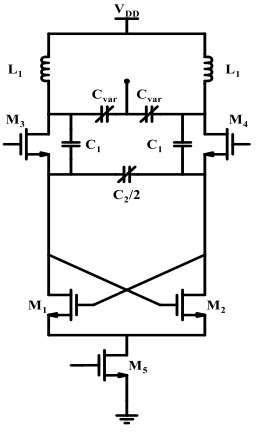

Fig. 1. Schematic of the traditional differential VCO.

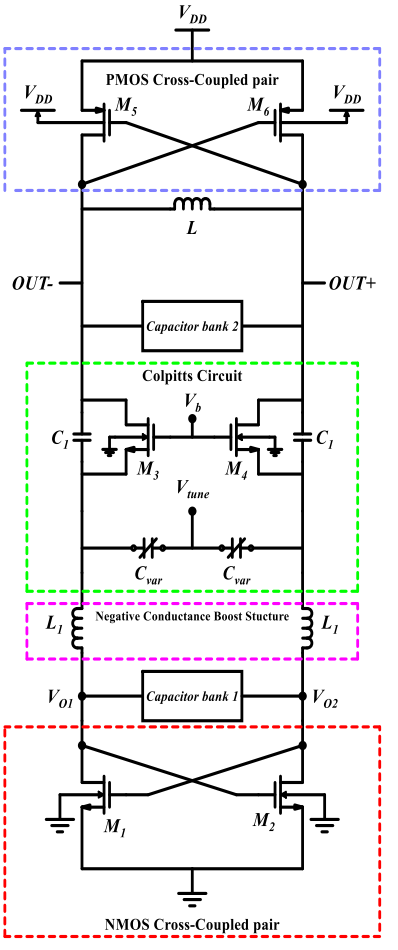

Fig. 2. Schematic of the proposed VCO.

2.2. Capacitor Bank Structure

Since many applications need a wide tuning range VCOs; therefore the frequency changing is one of the most important parameters in these circuits [7]. Frequency changing in VCOs can be performed in two ways; changing the inductor value and changing the value of capacitor with a varactor. However, changing the inductor value demands a larger size; therefore, it is not an appropriate way for frequency setting in the CMOS technology [17]. In the second way, a varactor is used as frequency setting. However, it occupies lower area with respect to the previous way, but it cannot provide a wide tuning range. To solve this problem, a capacitor bank is used to achieve a wide tuning frequency range [13].

In this paper a new capacitor bank structure, capacitor bank 1, was introduced as shown in Fig. 3, which is located at the bottom of the Colpitts structure. This capacitor bank consists of three unequal capacitors and three switches. Also, to cover a wide tuning frequency range, a simple capacitor bank, as illustrated in Fig. 4, was added on the top of the Colpitts structure.

As shown in Fig. 3, turning on/off of switches make four states of capacitors connections in capacitor bank 1. When all of the switches are off, any of the capacitors are not in the path (Fig. 3(a)). While the switch S_1 is on, C_3, C_4 and C_5 are series with together. Another mode happens when the switches S_1 and S_2 are on, in this case, capacitors C_4 and C_5 are short circuited and only, capacitor C_3 remains, as shown in Fig. 3(b). If S_1 and S_3 are on, as shown in Fig. 3(c), the capacitor C_5 remains and capacitors C_3 and C_4 are short circuited. The other state is that all switches are on. In this case, these three capacitors work in parallel as illustrated in Fig. 3(d). To cover a wide frequency range, a simple capacitor bank has been added on the top of the Colpitts structure. The capacitor bank 2 helps to improve the tuning range because there are 20 states of capacitor switching. Table 1 lists covering frequency of these 20 states. As can be observed, some of these states have overlap with each other. This is due to the same total capacitance that exists in these modes. Thus, the repetitious modes are not considered.

According to the results, both capacitor banks covered a frequency range of 21.95-24 GHz. Some states of the frequency range were achieved as follows: if all the switches turned off, the oscillation frequency range was 23.4 GHz - 24 GHz. When S_1, S_4, and S_5 turned on, the frequency range was 22.2 GHz - 22.65GHz. Also, if all of the switches turned on, the oscillation frequency changed from 21.95 GHz - 22.33 GHz.

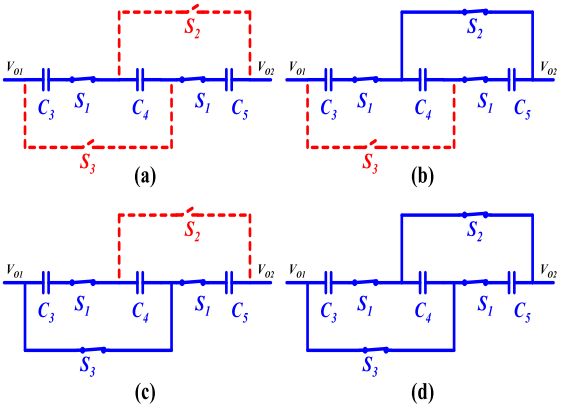

Fig. 3. The structure of capacitor bank 1.

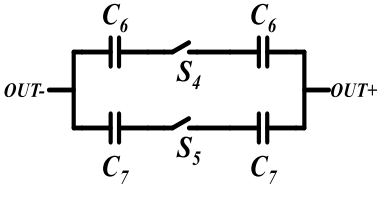

Fig. 4. The structure of bank 2 capacitors.

Table 1. State of switching capacitors and their covering frequency.

$S_1S_2S_3S_4S_5$	Frequency Range (GHz)
00000	23.4 ~ 24
00001	23.01 ~ 23.58
00010	22.7 ~ 23.26
00011	22.33 ~ 22.87
10000	23.24 ~ 23.78
10001	22.85 ~ 23.36
10010	22.54 ~ 23.04
10011	22.18 ~ 22.66
11000	23.2 ~ 23.77
11001	22.8 ~ 23.34
11010	22.46 ~ 23
11011	22.1 ~ 22.6
10100	23.17 ~ 23.73
10101	22.77 ~ 23.31
10110	22.45 ~ 22.97
10111	22.1 ~ 22.57
11100	23.01 ~ 23.52
11101	22.61 ~ 23.08
11110	22.3 ~ 22.73
11111	21.95 ~ 22.33

According to Table 1, by employing capacitor bank 1, the equivalent capacitance, which is seen at the bottom of the Colpitts VCO, was changed leading to an increased frequency range. Also, by adding capacitor bank 2 at the output node, the capacitors affect the output frequency directly and enhance frequency range significantly.

2.3. Start-up Condition Improvement

There is a tradeoff between the consumption power and transconductance gain, resulting in a tradeoff with the start-up condition, in VCOs [7]. In the proposed VCO, two NMOS and PMOS cross-coupled pairs were used to enhance the transconductance gain with low power consumption. Because, by using this structure transconductance gain is driven as follows:

$$g_{m_{total}} = g_{m_{PMOS}} + g_{m_{NMOS}} \quad (3)$$

Where $g_{m\text{-}PMOS}$ and $g_{m\text{-}NMOS}$ are transconductance gain of PMOS and NMOS transistors. As observed in (3), the transconductance gain has been increased and the start-up condition has been improved.

As mentioned the NMOS cross-coupled pair transistors were used at the bottom of the Colpitts structure to generate a negative resistance. To improve the start-up condition, two inductors are used between the Colpitts and cross-coupled pair structures. Using these inductors enhances the interesting gain of cross-coupled due to increase of the total impedance that is seen from

the output node of NMOS cross-coupled pair. Thus, start-up condition can be improved with low power consumption.

2.4. Phase Noise Consideration

It is critical and essential to minimize phase noise for VCO design [1], [10]. Variation of output voltage swing and varactor's common-mode voltage cause a change in the oscillation frequency which degrades the phase noise [9]. The general phase noise of VCOs is defined as [10]

$$L(\Delta f) = \frac{FkT}{2P_{avs}}\left[1+\frac{f_c}{\Delta f}+\left(\frac{f_\circ}{2\Delta f Q_L}\right)^2\left(1+\frac{f_c}{\Delta f}\right)\right] \quad (4)$$

where Q_L, Δf, f_o, f_c, T, P_{avs}, F, and K are quality factor of the inductor, offset frequency, center frequency, the flicker corner frequency of the active devices, temperature, average power through the resonator, noise factor of the devices and Boltzmann constant, respectively. Equation (4) indicates that the phase noise can be improved with a high quality factor, high output power, low noise factor, and low flicker noise.

In the proposed VCO, to understand the devices' noise effects on the output signal, a simple model has been considered for it, as illustrated in Fig. 5. For simplicity, the noise effect of NMOS cross-coupled is eliminated by inductors and the noise effect of inductors L_1 and L_2 are negligible. Thus, the NMOS cross-coupled pair, the inductors L_1 and L_2, the capacitor bank 1 and the varactors were modeled with C_{eq}. Also, the capacitor bank 2 is modeled by $C_{eq'}$. To calculate the noise effect on the output signal, the noise model of the proposed VCO is shown in Fig. 6.

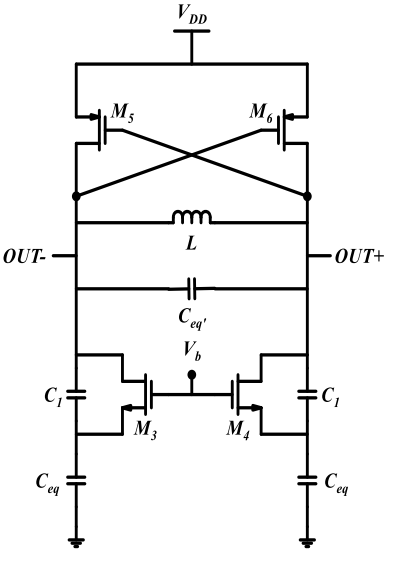

Fig. 5. The simple model of the proposed VCO.

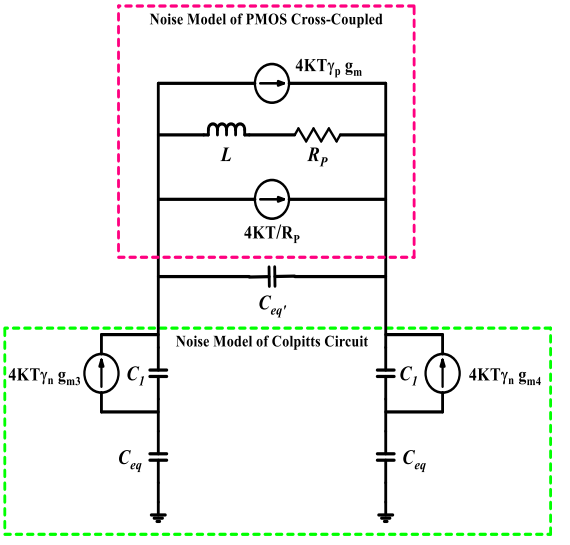

Fig. 6. Noise model of the proposed VCO.

According to Fig. 7, the noise power of the Colpitts circuit can be driven as follows:

$$P_{noise_{Colpitts}} = 4KT\gamma_n g_{m4} \quad (5)$$

Where K, T, γ, and g_{m4} are Boltzmann constant, temperature, channel noise coefficient of the transistor, and transconductance gain of transistor M_4, respectively. The oscillation condition of the Colpitts oscillator is obtained from (6):

$$g_{m4}R_p \geq \frac{C_{eq}}{C_1}+\frac{C_1}{C_{eq}}+2 \quad (6)$$

Where g_{m4} is the transconductance of the transistor, R_p is the equivalent parallel resistor of the inductor, C_{eq1} and C_1 are capacitors of Colpitts VCO.

Assuming $g_m = \frac{1}{R_P}(2+\frac{C_1}{C_{eq}}+\frac{C_{eq}}{C_1})$ and replacing it in (5), the noise power can be given by (7).

$$P_{noise_{Colpitts}} = 4KT\gamma_n\left(\frac{2}{R_P}+\frac{C_1}{R_P C_{eq}}+\frac{C_{eq}}{R_P C_1}\right) \quad (7)$$

By simplifying the (8), the noise power can be driven as (8).

$$P_{noise_{Colpitts}} = 4KT\gamma_n\left(\frac{C_1+C_{eq}}{R_P C_1 C_{eq}}\right)(C_1+C_{eq}) \quad (8)$$

Using the following equations

$$R_p = Q^2 R_S \quad (9)$$

$$Q = \frac{\omega_o L}{R_S} \tag{10}$$

$$\omega_o = \frac{1}{\sqrt{LC_{total}}} = \frac{1}{\sqrt{L\dfrac{C_{eq2}C_2}{C_{eq2}+C_2}}} \tag{11}$$

Equation (8) rewrites to:

$$P_{noise_{Colpitts}} = 4KT\ \gamma_n\ R_S\ \omega_o^2 C_1 C_{eq} \tag{12}$$

After obtaining the noise power of the Colpitts circuit, the noise power of the PMOS cross-coupled pair should be calculated to achieve the total noise power. Thus, the noise power of the PMOS cross-coupled pair can be calculated from Fig.7, as follows:

$$P_{noise_{PMOS}} = 4KT\gamma_p g_{m4} + 4KT\ / R_P \tag{13}$$

The oscillation condition of the cross-coupled oscillator is obtained from (14):

$$g_m R_P \geq 1 \tag{14}$$

Assuming $g_m = \frac{1}{R_P}$ and replacing it in (14), the noise power can be driven as (15)

$$P_{noise_{PMOS}} = \frac{4KT}{R_P}(1+\gamma_p) \tag{15}$$

According to (9)-(11), the noise power of PMOS cross-coupled is obtained from (16).

$$P_{noise_{PMOS}} = 4KT(1+\gamma_p)R_S\ \omega_o^2\ C_{total}^2 \tag{16}$$

Where C_{total} is the total load capacitance at the output node. Thus, the total noise power of the proposed VCO is driven as follows:

$$P_{noise} = P_{noise_{PMOS}} + P_{noise_{Colpitts}} \tag{17}$$

So:

$$P_{noise} = 4KTR_S\omega_o^2\left((1+\gamma_p)C_{total}^2 + \gamma_n C_1 C_{eq1}\right) \tag{18}$$

As shown in (18), in order to reduce the noise power to improve the phase noise performance, the total capacitance of PMOS cross-coupled, Capacitance of Colpitts structure and equivalent resistance series of inductors should be reduced. The value of parasitic capacitors is determined with respect to the size of transistors. To enhance the transconductance gain, it is necessary to increase the size of the transistors, but the transistors with large size produce a big value of parasitic capacitors, resulting in the degraded phase noise performance, according to (18). Thus, there is a tradeoff between phase noise and size of transistors. In this paper, the size of the transistors was calculated, leading to minimized capacitors value to improve the phase noise.

The cross-coupled pair has a good noise performance [1]; employing this structure in VCO improved the phase noise. In addition, the PMOS cross-coupled pair that was used to reduce dc power consumption, can improve phase noise due to its low flicker noise according to (5). Thus, to reach a better phase noise, a PMOS cross-coupled pair was used on the top of the proposed VCO.

2.5. Main Core of VCO

As the main core of the proposed VCO is based on the Colpitts structure; the start-up condition and the oscillation frequency of a Colpitts VCO with differential output are shown in Fig. 7 [7]. These parameters were given by (19) and (20).

$$g_m R_p \geq \frac{C_1}{C_2} + \frac{C_2}{C_1} + 2 \tag{19}$$

$$f = \frac{1}{2\pi\sqrt{LC\dfrac{C_1 C_2}{C_2+C_2}}} \tag{20}$$

Where, g_m is the transconductance of the transistor, R_p is the equivalent parallel resistor of the inductor, C_1, C_2, and L_4 are capacitance and inductance of Colpitts VCO's LC-tank respectively. To calculate the oscillation frequency and start-up condition, it is necessary to consider parasitic capacitors. For this reason, the equivalent half circuit of the proposed VCO that consists of parasitic capacitors is shown in Fig. 8. In this model, $C_{cross\text{-}N}$, $C_{cross\text{-}P}$, C_{eqL2}, and C_{eqL4} are parasitic capacitors of the NMOS pair, PMOS pair, and inductors L_2 and L_4, respectively. Also, C_{GS4} and C_{GD4} are Gate-Source and Gate-Drain capacitors of the transistor M_4. To calculate the oscillation frequency, total capacitance can be represented as follows:

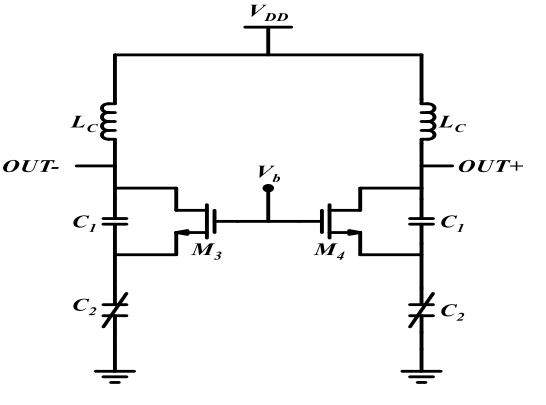

Fig.7. Schematic of the Colpitts VCO.

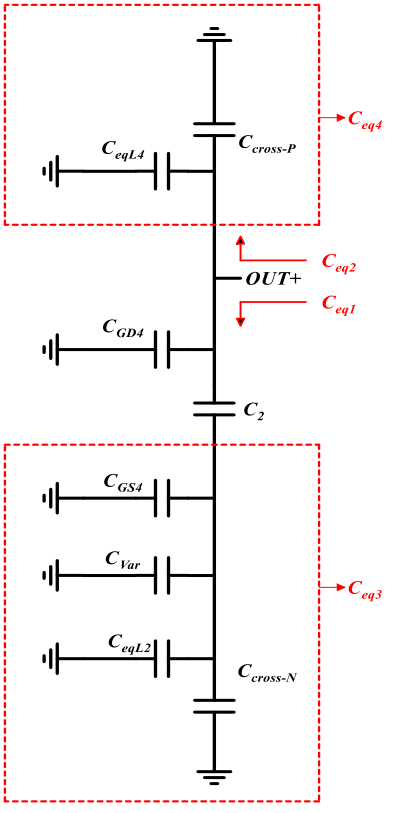

Fig. 8. Capacitors of proposed VCO at the output node.

$$C_{eq3} = C_{cross-N} + C_{eqL2} + C_{var} + C_{GS4} \quad (21)$$

$$C_{eq4} = C_{cross-P} + C_{eqL4} \quad (22)$$

$$C_{eq1} = \frac{C_{eq3} C_2}{C_{eq3} + C_2} + C_{GD4} \quad (23)$$

$$C_{eq2} = C_{eq4} \quad (24)$$

$$C_{Total} = C_{eq1} + C_{eq2} \quad (25)$$

Therefore, according to (9), the oscillation frequency of the proposed VCO (Fig. 2) can be derived as (26).

$$f = \frac{1}{2\pi\sqrt{LC_{Total}}} \quad (26)$$

The circuit parameters of the proposed VCO are listed in Table 2.

Table 2. Circuit parameters of the proposed VCO.

Parameters	Design Value
$\left(\frac{W}{L}\right)_{M1-M4}$	$\frac{22\ \mu m}{0.18\mu m}$
$\left(\frac{W}{L}\right)_{M5-M6}$	$\frac{80\ \mu m}{0.18\mu m}$
L	162 pH
L_1	288 pH
C_1	140 fF
C_{var}	93~120 fF
V_{DD}	1.8 V
V_b	1.8 V

3. SIMULATION RESULTS

The proposed VCO was simulated in TSMC 0.18 µm CMOS technology with Cadence software. The results showed that the power consumption was 6.34 mW at 23GHz from 1.8V supply voltage. Fig. 9 shows the layout of the proposed VCO in TSMC 0.18 µm CMOS technology which occupies 270 μm^2 area.

Fig. 10 demonstrates the frequency changes versus tune voltage in different capacitor banks switching modes. It can be observed that the VCO covers the frequency range of 21.95 GHz to 24 GHz. In fact, the tuning range is approximately 8.9%. The simulated phase noise at 23 GHz frequency is illustrated in Fig. 11. According to Fig. 11, the phase noise is -100 dBc/Hz, -120.5 dBc/Hz and -140 dBc/Hz at 100 KHz, 1 MHz, and 10 MHz frequency offsets, respectively.

The phase noise simulation results for FF, FS, SF, and SS corners are presented in Fig. 12 at 23GHz operation frequency. The corner simulation depicts that the circuit has good performance at different corners. As shown in Fig. 12, the phase noise has not changed much.

The phase noise histogram for 23 GHz at 1 MHz offset frequency by Monte Carlo analysis for 50 samples is demonstrated in Fig. 13. According to the results, the maximum likelihood of happening phase noise is around -122.534 dBc/Hz.

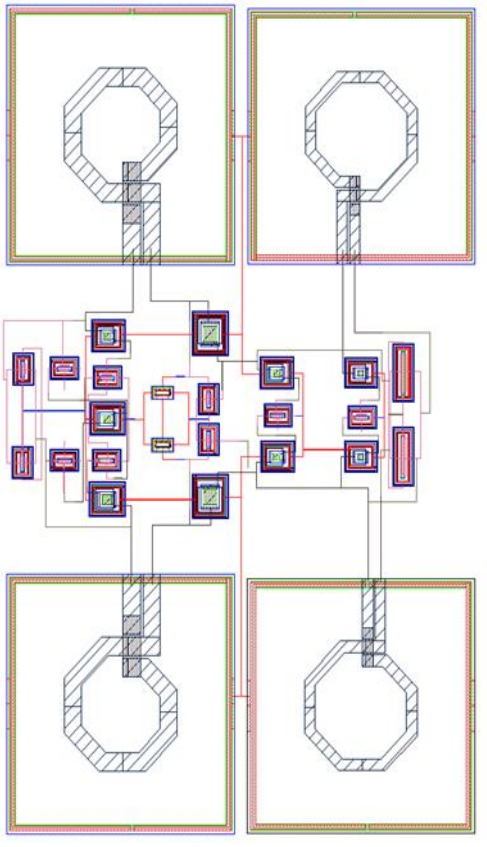

Fig. 9. The layout of the proposed VCO.

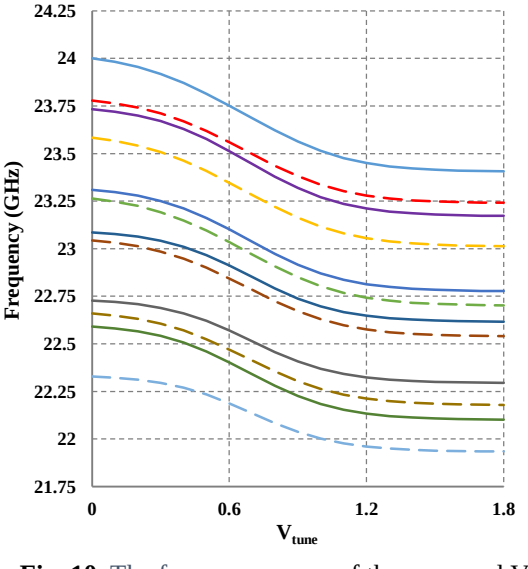

Fig. 10. The frequency range of the proposed VCO.

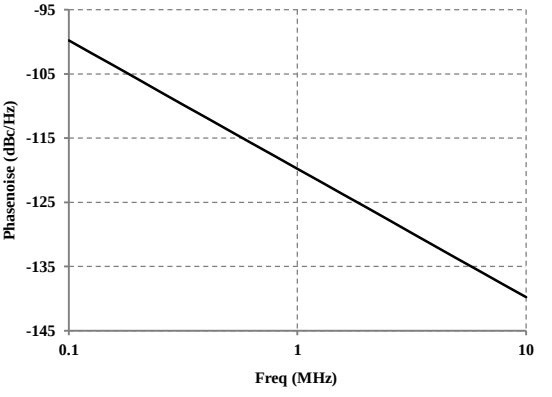

Fig. 11. Simulated phase noise of the proposed VCO at 1 MHz offset frequency.

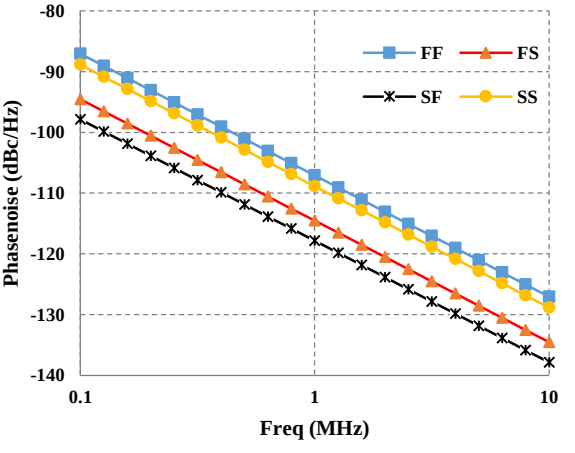

Fig. 12. Corners phase noise simulation of the proposed VCO at 1 MHz offset frequency.

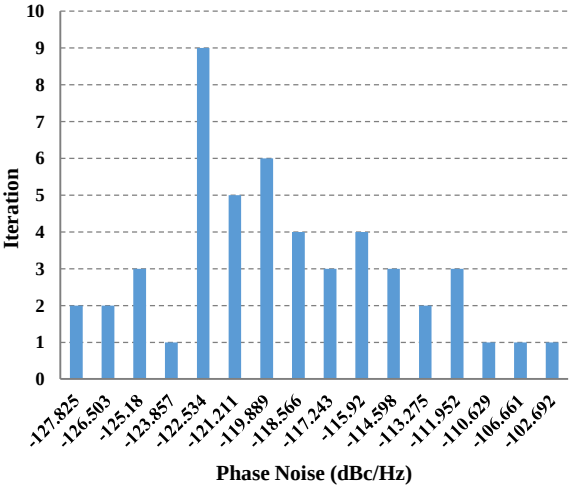

Fig. 13. Histogram of the proposed VCO phase noise at 1 MHz offset frequency.

As for characterizing the VCO performance, the widely used figure of Merit (FOM) is adopted in this work. The FOM is written as [7]

$$FOM = L(\Delta f) - 20\log\left(\frac{f_\circ}{\Delta f}\right) + 10\log\left(\frac{P_{dc}}{1mW}\right) \qquad (27)$$

Where $L(\Delta f)$, Δf, $f_\circ$, and P_{dc} are the VCO phase noise, offset frequency, carrier frequency, and dc power consumption, respectably. The calculated FOM is -91.68 dBc/Hz for 23 GHz center frequency.

Table 3 summarized the results of some published works in designing VCO. It is observed that, due to the using the combination of NMOS and PMOS cross-coupled pairs and Colpitts structures, the designed VCO can achieve low phase noise while operating at high frequency. According to this table, the phase noise has improved compared to the other works. From Table 3, it is found that the tuning range of this work is better than the other works. Also, Table 3 shows that the proposed VCO outperforms the other works in terms of FOM.

4. CONCLUSION

Using the combination of NMOS and PMOS cross-coupled pairs and Colpitts structures in the proposed VCO, the required dc power was reduced and the phase noise performance was enhanced. Moreover, by employing two inductors between Colpitts and NMOS cross-coupled pair, the start-up condition was improved. Also, a new capacitor bank structure increased the tuning range significantly. From the simulation results, it was shown that the proposed VCO is suitable for low power and low phase noise at high frequency applications.

Table 3. The circuit Parameters of the Proposed VCO.

	[8]	**[10]**	**[20]**	**[21]**	**This Work**
Process	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	90 nm CMOS	**0.18 µm CMOS**
Frequency (GHz)	18.95	30.02	23.17	20.8	**23**
Tuning Range (%)	3.6	1.34	1.2	4.8	**8.9**
Phase Noise @ 1-MHz offset (dBc/Hz)	-110.8	-104.1	-109.04	-116.4	**-120.5**
DC Power (mW)	3.3	2.3	11.33	3	**6.34**
FOM (dBc/Hz)	-191	-190	-185.8	-191.6	**-191.68**

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