Power Reduction of the Low Offset Dynamic Comparator with Novel Techniques

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ABSTRACT:
In this paper, dynamic comparators structure, by employing two methods for power consumption reduction with applications in low-power high-speed analog-to-digital converters, have been presented. The proposed comparators have low consumption thanks to power reduction methods. They have the ability for adjusting the offset. The comparators consume 14.3 and 24 μW at 100 MHz, which is equal to 3.7 and 11.8 fJ. The comparators are designed and simulated in 180 nm CMOS. Layouts occupy 210 and 240 μm^2, respectively.

KEYWORDS: Efficiency, Low-Power, Low-Offset, Dynamic Comparator.

1. INTRODUCTION

Global demand in the design of the electronic systems is toward manufacturing systems which have high speed and accuracy, with the low area and power consumption. In modern electronic systems such as mobile communications and data processing units, analog to digital conversion is one of the most important blocks of the digital system [1-4]. Speed, accuracy and power consumption of comparator has a critical role at the overall and proper performance of the ADC. Power consumption, input referred offset and evaluation time, are important specifications of the comparators. Generally, comparators are divided into two major classes: dynamic and static comparators [5]. Because of their higher speed and lower power consumption, dynamic comparators are widely used in the design of high speed ADCs. The input offset problem due to the static mismatch between threshold voltages, the value of μncox and mismatch between parasitic capacitances of the internal nodes, is an important challenge in the design of comparators in modern technologies with small feature sizes. On the other hand, using offset reduction methods increases power consumption. Decreasing input-referred offset without increasing power consumption is a great challenge in the design of comparators [6-8].

Lewis Gray structure is widely used in ADC design [9]. It has a preamplifier stage and a cross-coupled latch pair. In this structure, power consumption is increased to achieve high speed and low input offset. In dynamic comparator shown in Fig.` 1, input offset can be adjusted by the delay generated in clock pulse driving the latch stage [10].

Section 2, describes the structure and the basic operation of the comparator. In Section 3, two power reduction techniques are discussed to improve the energy consumption of the proposed comparator. Equations governing the offset of the comparator are presented in Section 4. Simulation results of the proposed comparator are summarized in Section 5.

2. STRUCTURE AND BASIC OPERATION OF THE COMPARATOR

Fig. 1 shows the structure of the comparator which is composed of two stages [10]. These are the decision stage and hold stage. Comparator operation has three different phases. As shown in Fig. 2, phase 1 is reset, phase 2 is decision or evaluation and the third phase is hold phase which stores the evaluation result for a specific time interval. In reset phase when clk1 is high, transistors M9 and M10 are off while M_7 and M_8 are on. As a result, nodes $V_{i\text{-}n}$ and $V_{i\text{-}p}$ are shorted to ground through M_7 and M_8. When clk1 is low, decision (evaluation) phase is started. In this phase, input signals $V_{i\text{-}n}$ and $V_{i\text{-}p}$ increase the node voltages $V_{o\text{-}n}$ and $V_{o\text{-}p}$. Considering the signal levels of Vip - $Vref_+$ and V_{in} – $V_{ref\text{-}}$, output voltages V_{out+} and V_{out-} will have different speeds. Of two voltages, one that approaches the threshold voltage of the NMOS transistor earlier, connects to V_{dd} through two cross-coupled inverters and another node will be connected to ground. As a result, one of the $V_{o\text{-}p}$ and $V_{o\text{-}n}$ are connected to V_{dd} or Gnd.

After this phase (evaluation time), input signal fluctuations cannot change the output state unless output nodes are reset for the next comparison.

In this structure, the input offset can be managed by the timing of the clock pulse *clk2*. In this structure, power is dissipated in hold phase while CMOS inverters do not need power consumption at this phase. The first stage has power dissipation while with modifying the structure, power consumption in the hold phase can be reduced. With this assumption that after the evaluation phase, output node $V_{o\text{-}p}$ equals to V_{dd}, a current will be drawn from $V_{r\text{-}p}$. The current path is shown in Fig. 3. In this path, transistors M1, M4 and M9 are on. While in hold phase there is no need for this current. With this description about the operation of the comparator, two methods are proposed to alleviate this problem.

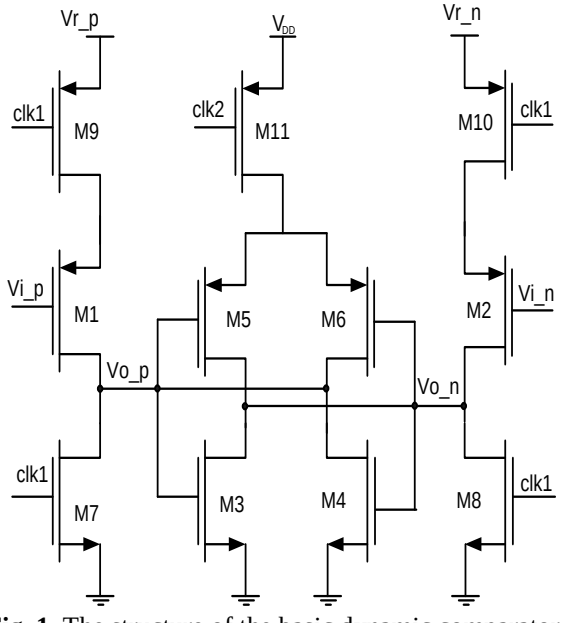

Fig. 1. The structure of the basic dynamic comparator.

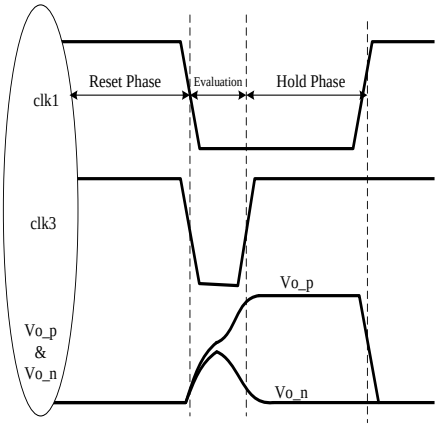

Fig. 2. Time diagrams of clock pulses of the dynamic comparator.

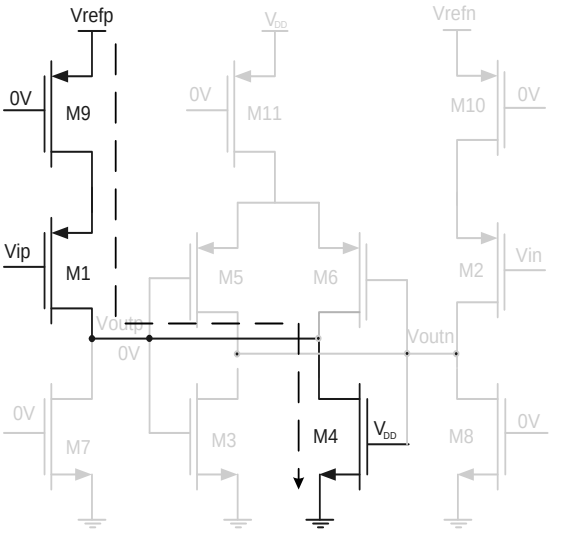

Fig. 3. Power consumption path in comparator when the evaluation is finished (V_{in}>V_{ip}).

3. POWER REDUCTION METHODS

3.1. First Proposed Technique

The structure of the proposed comparator which uses technique 1 is shown in Fig. 4. This is based on using another clock pulse for triggering M_9 and M_{10} transistors. It is going low at the same time with clk1 but after the state of the latch is determined it goes to high, again. In this condition, M_9 and M_{10} are off and no current drawn from Vr-n and Vr-p and no power is dissipated in the evaluation phase. Power is dissipated when clk3 is low, and in reset and evaluation no power is dissipated. Overall power consumption is decreased and energy efficiency can be improved. The important point in the proposed comparator is the length of time that it is in a low state. It must be long enough for the comparator to finish its decision.

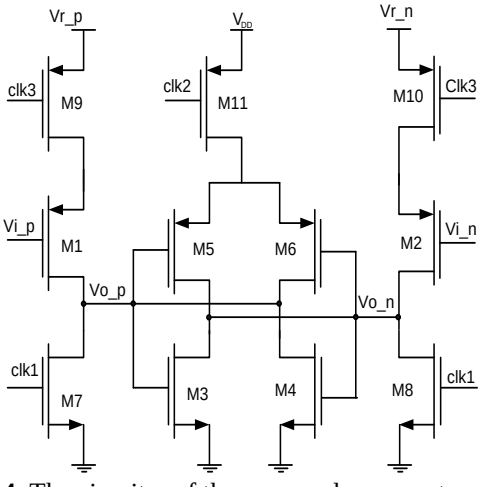

Fig. 4. The circuitry of the proposed comparator using technique 1.

3.2. Second Proposed Technique

The structure of the second comparator is shown in Fig. 5. In this structure, two additional transistors are used. Their function is to cut the current path in the evaluation phase to decrease average power consumption. In the hold phase, $V_{o\text{-}p}$ and $V_{o\text{-}n}$ are complements when one of them is higher than the other one in low and vice versa. This condition can be used for power consumption reduction in the hold phase. They work as follows: when $V_{o\text{-}p}$ is "1", transistor M_{12} cuts the path which causes the current to be drawn from power supply after decision phase while there is no problem in M_{13} being on. Also, when $V_{o\text{-}n}$ is "1", the output $V_{o\text{-}p}$ is "0". In this state, M_{13} is off, and no current is drawn from $V_{r\text{-}n}$, so power consumption will be decreased. In this comparator, the power dissipated in one period is reduced which improves the energy efficiency. M_{12} and M_{13} transistors act as switches and have no serious effect of input-referred offset of the comparator.

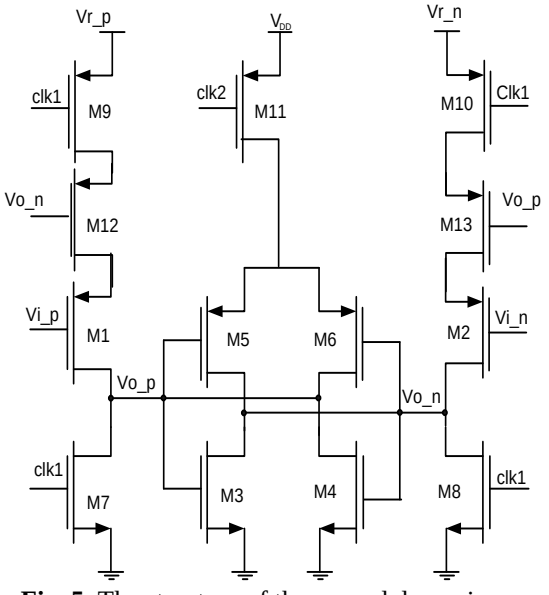

Fig. 5. The structure of the second dynamic comparator.

4. OFFSET ANALYSIS OF THE COMPARATOR

The offset voltage of the comparator includes the dynamic and static offset. Static offset is due to the threshold voltage and $\mu_n C_{ox}$ variations and dynamic offset is the result of the mismatch between parasitic capacitances of the internal nodes of the circuit.

In this section, analysis of the input offset voltage and its equation is discussed. To calculate the input offset voltage, we use the following rule: if there is the mismatch in the circuit that causes wrong decision, how much input voltage is needed to get the right outputs [5]. In this comparator, after reset phase, I_{ip} and I_{in} increase the voltages $V_{o\text{-}p}$ and $V_{o\text{-}n}$ until output voltage approaches the threshold voltages of the M1 and M2 transistors. The values of these currents are:

$$I_{i_p} = 0.5\mu_{p3}C_{ox}\left(\frac{W}{L}\right)_5\left(V_{i_p} - V_{r_p} - V_{tp3}\right)^2 \quad (1)$$

$$I_{i\_n} = 0.5\mu_{p4}C_{ox}(\frac{W}{L})_5(V_{i\_n} - V_{r\_n} - V_{tp4})^2 \quad (2)$$

Also, the currents resulting from M5 and M6 increase the output voltages. The values of these currents are:

$$I_5 = 0.5\mu_{p5}C_{ox}(\frac{W}{L})_5\left(V_{DD} - V_{o\_p} - V_{tp5}\right)^2 \quad (3)$$

$$I_6 = 0.5\mu_{p6}C_{ox}(\frac{W}{L})_5(V_{DD} - V_{o\_n} - V_{tp6})^2 \quad (4)$$

When there is the mismatch between the product of carrier mobility and oxide capacitance ($\mu_n C_{ox}$), also threshold voltages of M3 and M4 transistors and M5 and M6 transistors, charging current of the capacitances at nodes $V_{o\text{-}p}$ and $V_{o\text{-}n}$ will be different. This results in offset. With all other conditions equal, if the mismatch is only due to threshold voltages of M3 and M4, input offset will be:

$$V_{os\_M3,4}^2 = \sigma V_{Tp4}^2 + \sigma V_{Tp3}^2 \quad (5)$$

In these equations, μ_p is the mobility of PMOS transistors and $\sigma\mu_i$ is the coefficient of mobility variation of the *i*th transistor. In calculations, mobility is considered to be independent of the threshold voltage. The value of mobility variation of holes and electrons ($\sigma\mu_p$ and $\sigma\mu_n$) and threshold variation σV_T of PMOS and NMOS transistors depend on the manufacturing technology [11-12]. With all other conditions equal, if the size of M3 and M4 is different, the input offset of the comparator is:

$$V_{os\_3\_4} = \sqrt{\frac{\mu_{p3}C_{ox}(\frac{W}{L})_3}{\mu_{p3}C_{ox}(\frac{W}{L})_4}}V_A - V_A \quad (6)$$

The voltage needed to cancel this match is equal to:

$$V^2{}_{os\_M3,4\_\Delta W} = (\sqrt{1 + \frac{\Delta W_{3,4}}{W_3}} - 1)^2 V_A^2 \quad (7)$$

With the same method, for the mismatch of other parameters, input offset can be calculated. In overall, offset voltage due to all parameters of the M3 and M4 is:

$$V_{os\_M3,4}^2 = \sigma V_{Tp4}^2 + \sigma V_{Tp3}^2 + V_A^2\frac{\sigma\mu_{p3}}{\mu_p} + V_A^2\frac{\sigma\mu_{p4}}{\mu_p} + V^2{}_{os\_M3,4\_\Delta W} \quad (8)$$

Repeating this for the M_5 and M_6, input offset is as follows:

$$V_{os\_M5,6}^2 = \left(\frac{W_5.\sigma\mu_{p5}}{2W_3}\right)^2 \frac{V_B^4}{V_A^4} \quad (9)$$

To calculate the input offset voltage due to the mismatch between node capacitances, we suppose that all devices and voltages are the same. The Current of transistors M1 and M5 charges the output node $V_{o\text{-}p}$ and the current of transistors M2 and M6 charges the output node $V_{o\text{-}n}$.

$$I_{i\_p} = C_L \frac{dV_{o\_p}}{dt} \quad (10)$$

$$I_{i\_n} = (C_L + \Delta C) \frac{dV_{o\_n}}{dt} \quad (11)$$

For voltages $V_{o\text{-}p}$ and $V_{o\text{-}n}$ to be equal their slope must be equal, too. So:

$$\frac{I_{i\_p}}{C_L} = \frac{I_{i_n}}{C_L + \Delta C} \quad (12)$$

$$\left(1 + \frac{\Delta C}{C_L}\right) I_{i\_n} = I_{i\_p} \quad (13)$$

By replacing the current of transistors, at the instant that output voltage approaches the threshold of the transistors, a unit voltage can be calculated needed to cancel the mismatch of the node capacitances. Finally, the result is:

$$\left(1 + \frac{\Delta C}{C_L}\right)(I_{M1} + I_{M3}) = I_{M2} + I_{M4} \quad (14)$$

$$\sigma V_{os\_\Delta C}^2 = \left\{\sqrt{\frac{\left(1+\frac{\Delta C}{C_L}\right) W_1 V_A^2 + W_3 V_B^2 \frac{\Delta C}{C_L}}{W_2}} - V_A\right\}^2 \quad (15)$$

Considering the equations and the analyses, the input voltage can be calculated.

5. SIMULATION RESULTS

The proposed comparator has been designed and simulated in a 180 nm CMOS process. Table 1 summarizes the size of the devices.

Table 1. The size of the devices of the proposed comparator.

Size	W/L
M_1,M_2	5µm/180nm
M_3,M_4	220nm/180nm
M_5,M_6	1µm/180nm
M_7,M_8	7µm/180nm
M_9,M_{10}	1µm/180nm

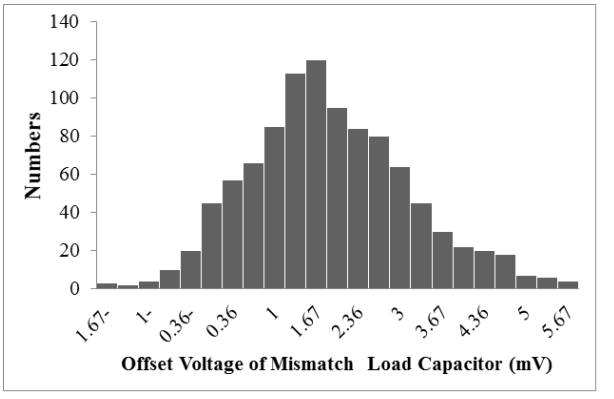

Fig. 6. Histogram of the input offset voltage versus capacitance mismatch for comparator 1.

Considering the input offset analysis of the comparator in previous sections and the Monte-Carlo (1000 points) simulation results which are shown in Fig. 6, input offset resulting from manual calculation is 1.6 mV and from the simulation is 1.9 mV. Fig. 6 shows the results of manual calculation and simulation results versus the mismatch of the transistors. In this figure, the effect of M_1, M_2, M_5 and M_6 on offset has been shown. This figure shows that offset calculations have acceptable convergence with simulations.

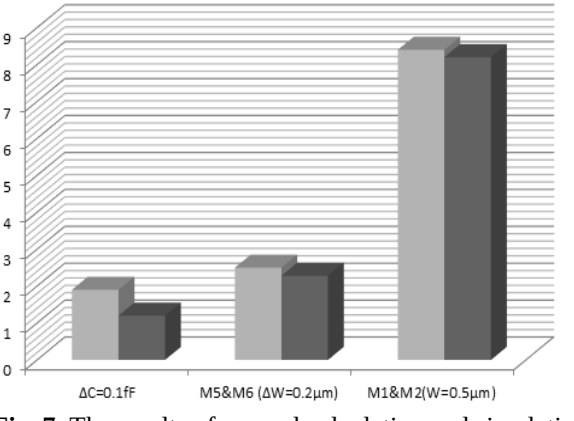

Fig. 7. The results of manual calculation and simulation for input offset due to different parameters.

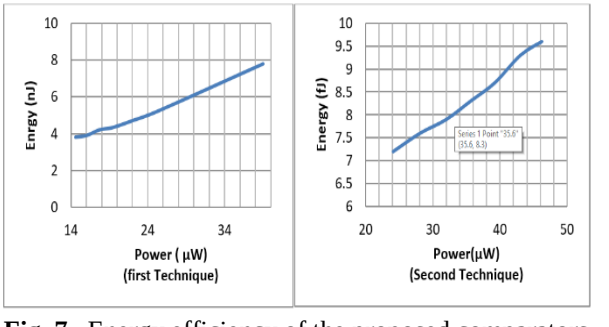

Fig. 7. Energy efficiency of the proposed comparators versus dissipated power.

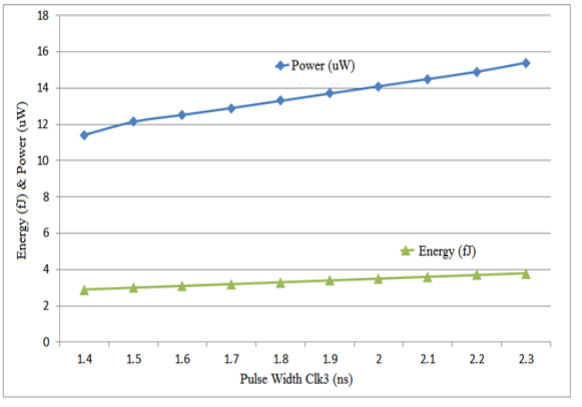

Fig. 9. Energy and power consumption versus *clk3* pulse width in the proposed technique 1.

In Fig. 7, comparator input offset simulation results and simulation results due to the mismatches of the various elements are shown. For manual calculations and simulations, input voltage, output voltage and the threshold voltage of PMOS transistors are all 0.5 V, power supply voltage is 1.2 V and comparison voltage is ±1.2 V at 100 MHz. Fig. 7 shows that the results of manual calculation have the ability to predict the input offset. These results show that the mismatch of input pair transistors M_1 and M_2 has more impact on the offset. Also, as the size ratio of transistors M_3 and M_4 to M_1 and M_2 increases, the input offset will be reduced.

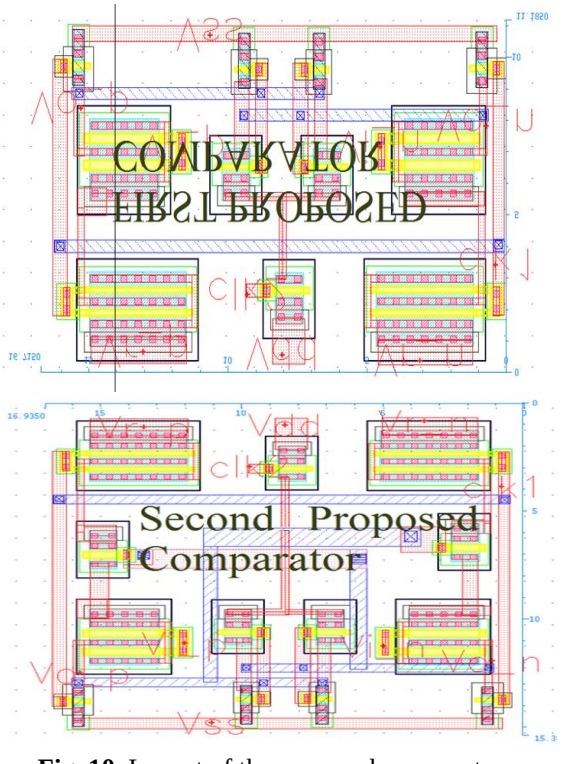

Fig. 10. Layout of the proposed comparators.

Table 2. Comparison of power and energy of different comparators.

Reference	Power(µW)	Delay(ps)	Tech.(nm)	Energy(fJ)
[13]	82	130	180	10.7
[10]	51	152	90	7.8
[8]	116	170	180	19.7
First work	14.2	258	180	3.7
Second work	24	492	180	11.8

In Fig. 8, the energy consumption of the proposed techniques is shown. The improvement achieved by the first techniques is better than the second one. In Fig. 9, the effect of clk3 pulse width on power consumption and energy efficiency has been shown.

Fig. 10 shows the layout of two proposed comparators. Comparator 1 occupies 210 µm^2 same as the basic comparator and the second comparator has 240 µm^2 area. In Table 2, Comparison of power and energy of different comparators is shown.

6. CONCLUSION

In this paper, the basic structure of dynamic comparators employing two techniques for power consumption reduction and energy efficiency improvement has been presented. This comparator is designed and simulated in a 180 nm CMOS process. Equations governing the input offset have been analyzed. Simulation results for offset voltage due to some of the important elements are compared to mathematical calculation. Simulations show that power consumption for two proposed techniques are 14.3 µW and 24 µW, respectively. Energy efficiencies at 100 MHz are 3.7 and 11.8 *f*J, respectively.

7. APPENDIX

$$V_A = V_i - V_r - V_{tp}$$
$$V_{r_n}=V_{r\_p} = V_r$$
$$V_i = V_{r_n} = V_{r_p}$$
$$V_{Tpi} = V_{Tp} + \sigma V_{Tpi}$$
$$\mu_{pi} = \mu_p + \sigma\mu_{pi}$$
$$W_4 = W_3 + \Delta W_{3,4}$$
$$W_5 = W_6 + \Delta W_{5.6}$$
$$V_{os5\_6}^2 = \frac{\Delta W_{5,6}}{2W_3V_A}V_B^2$$

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