

Magnitude Comparison and Sign Detection based on the 4-Moduli Set $\{2^n+1, 2^n-1, 2^n+3, 2^n-3\}$

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ABSTRACT:

The 4-moduli set residue number system (RNS), $\{2^n + 3, 2^n - 3, 2^n + 1, 2^n - 1\}$, with a wide dynamic range, has recently been proposed as a balanced 4-moduli set for utilizing the cases that demand fast calculations such as deep learning and implementation of asymmetric cryptographic algorithms. Up to now, only an unsigned reverse converter has been designed for this moduli set. Thus, there is a need for two separate units, a sign detection circuit, and a comparator to use this set in cases requiring sign and comparison. Nevertheless, the existence of these components demands high hardware that makes the implementation of the RNS impractical. Therefore, this paper presents the design of a sign detection circuit and a signed reverse converter that can overcome this problem by reusing the hardware. To achieve an integrated hardware design, first, we optimized the previous unsigned reverse converter for this 4-moduli set and next, we derived an approach from the structure of the reverse converter for detecting signs and recognizing comparators. Finally, using the sign signals extracted from the reverse converter, we change reverse converter into a unit that perform sign detection and comparison. The simulation has been conducted using ISE Design Suite 14.7 tool and the Spartan6 family technology. Empirical results show that, the proposed multifunctional unit has an approximately identical performance with respect to delay and area compared to the previous reverse converter. Besides, the proposed signed reverse converter relies on a 46% and 28% reduction in area and delay compared to the previous unsigned reverse converter which uses a comparator and also a multiplexer to detect a sign in the output.

KEYWORDS: Residue Number System, Reverse Converter, Computer Arithmetic, Sign Detection.

1. INTRODUCTION

The efficiency of VLSI circuits, including digital signal processing, encryption systems, deep learning, and cases in which excessive and repetitive addition and multiplication operations are needed, is determined based on efficiency of the arithmetic units like adders and multipliers. A suitable representation of numbers increases the efficiency of the functions of arithmetic unit. By increasing the bit width, the calculation speed decreases in the binary number system; this happens because of the possibility of carry propagation from Least Significant Bits (LSB) to Most Significant Bits (MSB). Thus, this limitation has introduced different numerical systems such as the residue number system (RNS) [1]. Residue number system has been recognized as a tool for creating parallelism to perform arithmetic operations such as addition and multiplication

efficiently [2]. Aside from traditional RNS applications including digital signal processing [3] and encryption [4], this technology has been used in emerging applications as in deep learning [5-8], DNA calculations [9], and modern encryptions [10]. The most important point in designing the RNS system is choosing the moduli set [11]. The parallelism degree, the complexity of operations among modules, and the dynamic range depend on the type of moduli set. Accordingly, many specific moduli sets have been presented for RNS and categorized as arithmetic moduli sets (balanced) and conversion-friendly moduli sets (unbalanced) [12-23]. Balance moduli sets are suitable for operations such as encryption and convolutional deep learning, in which the internal addition and multiplication rate is considerably more than the required conversions. One of the remarkable balanced moduli sets is $\{2^n + 3, 2^n -$

$3, 2^n + 1, 2^n - 1$ as it uses the entirely balance moduli, $2^n \pm 1$ and $2^n \pm 3$. However, including the $2^n \pm 3$ moduli leads to more complexities of the inter-modular operations such as reverse conversion, sign detection, and comparison. These problems indicate a limit for using this kind of moduli sets in unsigned applications, whereas most software applications including deep learning require working with signed numbers. In this paper, for the first time, the sign detecting component and comparator for the $\{2^n + 3, 2^n - 3, 2^n + 1, 2^n - 1\}$ moduli set is proposed. First of all, the previous unsigned reverse converter has been optimized for this moduli set to reduce hardware complexity and delay. Next, we derive an algorithm for sign detection and magnitude comparison for this moduli set. The proposed method uses the same reverse converter to extract sign. It is achievable to create a unit that can perform a set of operations, i.e. sign detection, comparison, and signed reverse conversion. Experimental results show the effect of the proposed method. In the rest of paper, Sections 2 and 3 deal with the background and concisely state the formulas and the leading construction of unsigned reverse converter in the $\{2^n + 3, 2^n - 3, 2^n + 1, 2^n - 1\}$ moduli set. Section 4 reports the reverse converter, and sections 5-7 depict the proposed algorithm for sign detection and magnitude comparison. Finally, performance evaluation is presented in sections 8-9.

2. RELATED WORKS

One of the most important obstacles in using RNS is the absence of efficient sign detection and magnitude comparison circuits. Unlike the binary number system, by the value of which sign detection based on bits is carried out, in the residue number system this method is not applicable since the numbers are non-weighted. The sign of a number in RNS is determined according to the division of its dynamic range into two equal parts and also according to this point that the number is located whether in the upper half of the range or in the lower half of that. This operation is usually carried out by a comparator in RNS and is considered difficult and complex. A comparator is normally located in the output of the reverse converter to detect a sign in a conditional operation [24]. A new approach has recently been proposed for improving and increasing the efficiency of reverse converters through which we can achieve the sign inside a reverse converter in order to minimize the area, delay, and energy consumption. Therefore, numerous studies have been conducted towards the field of sign detection and magnitude comparison for conversion-friendly moduli sets [25-29]. Nevertheless, owing to the shortage of extensive dynamic range, such moduli sets are not appropriate for a number of applications which require implementation of high-speed arithmetic such as encryption. Currently, researchers have aimed to find large dynamic range

moduli sets (over three modules) [22-23]. Designing a signed reverse converter for such moduli sets is accompanied with many complexities. Nonetheless, in [31], a new method for designing reverse converters, for a particular class of moduli sets with $\{2^k \cdot 2^p - 1\}$ form, commonly known as C-Class, is presented. Using the above leads to the creation of computational channels that easily process the RNS numbers. The Chinese Remainder Theorem 1 (New-CRT-I) is regarded as one of the options to design a reverse converter for such sets based on the relation $X = x_1 + 2^k Y$. The division of the dynamic range into two parts provides an upper half which is smaller than $M/2$, and a MSB which equals zero and is situated within the spectrum of positive numbers. However, the lower half is bigger than $M/2$ and has a MSB which equals one and is located within the spectrum of negative numbers. The number of $M/2$ with a MSB equal to zero possesses K states, half of which have a MSB equal to zero and are situated within the spectrum of positive numbers, and the rest has a MSB equal to one situated within the spectrum of negative numbers. In [31], the sign is identified through designing a sign detection unit which constitutes a number of logic gates and through analyzing the MSB. In [32-33], another categorization of moduli sets, known as A-Class, with the $\{2^k \cdot 2^p - 1, 2^{2n} - 1\}$ form, is identified by implementing some changes in the previous sign detection unit and by applying the New-CRT-I. In the present study, a similar method alongside with using the MRC algorithm is utilized for detecting the sign.

3. BACKGROUND

The Residue Number System (RNS) is a modular number system that is able to do arithmetic operations in a parallel manner without carry propagating between the residues. The residue number system is designed based on a moduli set whose moduli are pairwise relatively prime such as $\{P_1, P_2, \dots, P_n\}$. Then, weighted binary numbers get converted into the (x_1, x_2, \dots, x_n) form of residues through using the equation $x_i = X \bmod P_i = |X|_{P_i}$. The product of the moduli, namely $M = P_1 \times P_2 \times \dots \times P_n$, defines the dynamic range. The dynamic range displays the spectrum of integers that can be shown in the residue number system. This dynamic range is equal to $D_R = [0, M)$ for unsigned residue number system. Therefore, for the signed residue number system, the dynamic range is divided into two parts (1) and (2):

$$\text{Odd} : \begin{cases} \left[0, \frac{M-1}{2}\right] : \text{Positive} \\ \left[\frac{M+1}{2}, M-1\right] : \text{Negative} \end{cases} \quad (1)$$

$$Even : \begin{cases} \left[0, \frac{M}{2} - 1\right] : Positive \\ \left[\frac{M}{2}, M - 1\right] : Negative \end{cases} \quad (2)$$

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he RNS number can be transformed to regular number using the reverse convertor. This reverse conversion can be based on the Mixed-Radix Conversion (MRC) method or the Chinese Remainder Theorem 1 (New-CRT-I) [20]. For instance, the weighted number X can be achieved based on the residues (x_1, x_2, \dots, x_n) and the moduli set $\{P_1, P_2, \dots, P_n\}$ through using the Chinese Remainder Theorem 1 and (3).

$$X = x_1 + P_1 |k_1(x_2 - x_1) + k_2 P_2(x_3 - x_2) + \dots + k_{n-1} P_2 P_3 \dots P_{n-1}(x_n - x_{n-1})|_{P_2 P_3 \dots P_n} \quad (3)$$

The multiplicative inverses can be obtained using the following relations:

$$|k_1 \times P_1|_{P_2 P_3 \dots P_n} = 1 \quad (4)$$

$$|k_2 \times P_1 \times P_2|_{P_3 \dots P_n} = 1 \quad (5)$$

$$|k_3 \times P_1 \times P_2 \times \dots \times P_{n-1}|_{P_n} = 1 \quad (6)$$

First, the reverse converter can be obtained for the 4-moduli set $\{2^n + 1, 2^n - 1, 2^n + 3, 2^n - 3\}$ using the New-CRT-I. Thus, principle and architectural [22] formulas have been investigated here briefly. At first, two conversions for $\{2^n + 1, 2^n - 1\}$ and $\{2^n + 3, 2^n - 3\}$ moduli sets occur in a parallel and simultaneous manner.

In the first stage, the reverse converter carries out the conversion process for the $\{2^n + 1, 2^n - 1\}$ moduli set, using the New CRT-I algorithm and (7).

$$X_I = x_1 + (2^n + 1) |K_I(x_2 - x_1)|_{2^n - 1} \quad (7)$$

Also, in parallel to this stage, the reverse convertor carries out the conversion process for the $\{2^n + 3, 2^n - 3\}$ moduli set, using the New-CRT-I algorithm and (8).

$$X_J = x_3 + (2^n + 3) |K_J(x_4 - x_3)|_{2^n - 3} \quad (8)$$

Eventually, through using the values obtained from (7) and (8), (X_I, X_J) for the general moduli set $\{2^{2n} - 1, 2^{2n} - 9\}$, using the New-CRT-I algorithm, the value of X is realized by utilizing (9).

$$X = X_J + (2^{2n} - 9) |K(X_I - X_J)|_{2^{2n} - 1} \quad (9)$$

Where the three multiplicative inverses, K_I, K_J , and K, have been proved and calculated in [20].

Thus, the general structure of the reverse converter for the 4-moduli set $\{2^n + 1, 2^n - 1, 2^n + 3, 2^n - 3\}$ is

depicted in Fig. 1. In this structure, operand preparation unit 1 (Opu-I), Opu-J, and Opu-F conduct the required shifts and inversions. Then, the reverse conversion was implemented using the carry-save adder (CSA) and the carry propagate adder (CPA).

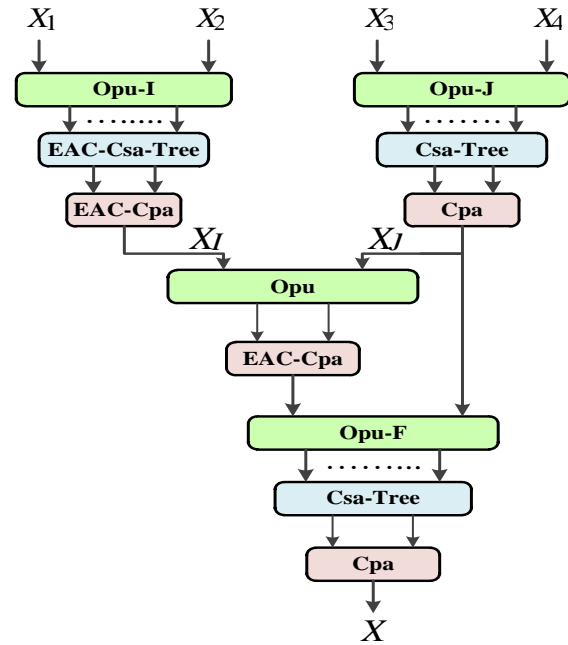


Fig. 1. General overview of the unsigned reverse converter [20].

4. REVERSE CONVERTOR

In this section, by changing the structure of the reverse converter of [22-23] and by using the New-CRT-I and MRC algorithms for the 4-moduli set $\{2^n + 1, 2^n - 1, 2^n + 3, 2^n - 3\}$, we conduct it into a reverse converter with a sign detection and magnitude comparison circuit. In the first stage (section 4.1), by using the New-CRT-I algorithm, the reverse converter for the subset $\{2^n + 1, 2^n - 1\}$ is obtained. In the second stage (section 4.2), by using the New-CRT-I algorithm, the reverse converter for the subset $\{2^n + 3, 2^n - 3\}$ is obtained, and finally, by using the MRC, the reverse convertor for the final moduli set $\{2^{2n} - 1, 2^{2n} - 9\}$ is obtained (section 4.3).

4.1. Reverse Convertor for $I = \{2^n + 1, 2^n - 1\}$

The Reverse Convertor for the $\{2^n + 1, 2^n - 1\}$ moduli set is as follows:

$$X_I = x_3 + (2^n + 1) |K_I(x_4 - x_3)|_{2^n - 1} \quad (10)$$

Therefore, considering the multiplicative inverses $K_I = 2^{n-1}$ and the relation $P_1 |Z|_{P_2} = |P_1 Z|_{P_1 P_2}$, the abovementioned equation can be rewritten follows:

$$X_I = |x_3 + (2^n + 1)2^{n-1}(x_4 - x_3)|_{2^{2n-1}} = |2^{n-1}(2^n + 1)x_4 + 2^{2n-1}x_3 + 2^{n-1}\bar{x}_3 + (2^{n-1} - 1)|_{2^{2n-1}} \quad (11)$$

4.2. Reverse Converter for $J = \{2^n + 3, 2^n - 3\}$

The equation of the reverse converter for the 2-moduli set $\{2^n + 3, 2^n - 3\}$ is based on the same equations presented in [22-23] as shown by (12).

$$X_J = x_2 + (2^n + 3)|K_J(x_3 - x_2)|_{2^{n-3}} \quad (12)$$

Considering that the two moduli, $2^n + 3$ and $2^n - 3$, are relatively prime to each other, the inverse multiplication is calculated as follows:

$$\begin{aligned} |K_J \times (2^n + 3)|_{2^{n-3}} = 1 &\rightarrow K_J = |(2^n + 3)^{-1}|_{2^{n-3}} \rightarrow |k_J \times (2^n + 3)|_{2^{n-3}} = |k_J \times 6|_{2^{n-3}} \\ \rightarrow K_J = \left| \frac{1}{6} \right|_{2^{n-3}} \end{aligned} \quad (13)$$

Therefore, we have:

$$K_J = \begin{cases} \left(\frac{2^{n-1}-2}{-3} \right) = -(2^{n-3} + 2^{n-5} + \dots + 2^1) & \text{even } n \\ \left(\frac{2^{n-1}-1}{3} \right) = (2^{n-3} + 2^{n-5} + \dots + 2^0) & \text{odd } n \end{cases} \quad (14)$$

Now, the value of X_J is expressible using the inverse multiplication calculated in (14) as (15) suggests.

$$X_J = x_2 + (2^n + 3) \left| K_J(x_3 - \overbrace{(3C_n + \hat{x}_2)}^{x_2}) \right|_{2^{n-3}} \quad (15)$$

It should be noted that in the abovementioned equation, the residue value x_2 belongs to the $2^n + 3$ modulo and its bit width is $(n + 1)$.

4.3. Reverse Converter for the $\{2^{2n} - 1, 2^{2n} - 9\}$

The final value of X is calculated using (16) to (19).

$$X = V_1 + V_2P_1 + V_3P_1P_2 + \dots + V_n \prod_{i=1}^{n-1} P_i \quad (16)$$

$$V_1 = x_1 \quad (17)$$

$$V_2 = |(x_2 - V_1)|_{P_1}^{-1}|_{P_2} \quad (18)$$

$$V_3 = |((x_3 - V_1)|_{P_1}^{-1}|_{P_3} - V_2)|_{P_2}^{-1}|_{P_3} \quad (19)$$

Generally, (17) to (19) are expressible as (20).

$$V_n = |(((x_n - V_1)|_{P_1}^{-1}|_{P_n} - V_2)|_{P_2}^{-1}|_{P_n} - \dots - V_{n-1})|_{P_{n-1}}^{-1}|_{P_n} \quad (20)$$

Thus, by using the defined equations, the reverse converter can be expressed for the residue values, (X_I, X_J) , and the moduli set $\{2^{2n} - 1, 2^{2n} - 9\}$ as (21) and (22) propose.

$$V_1 = X_J \quad (21)$$

$$V_2 = |(X_I - V_1)|(2^{2n} - 9)^{-1}|_{(2^{2n-1})}|_{(2^{2n-1})} \quad (22)$$

Now, the inverse multiplication of $|(2^{2n} - 9)^{-1}|_{(2^{2n-1})}$ can be calculated as it is expressed in (23).

$$K = |(2^{2n} - 9)^{-1}|_{(2^{2n-1})} \rightarrow K = -2^{2n-3} \quad (23)$$

Through placing the obtained inverse multiplication value in (23), the (24) can be obtained.

$$\begin{aligned} V_2 &= |(X_I - X_J)(-2^{2n-3})|_{(2^{2n-1})} \rightarrow \\ V_2 &= |(X_J - X_I)(2^{2n-3})|_{(2^{2n-1})} \rightarrow \\ V_2 &= |2^{2n-3}((X_{J,2n-1} \dots X_{J,0}) - \\ & (X_{I,2n-1} \dots X_{I,0}))|_{2^{2n-1}} \rightarrow \\ V_2 &= |(X_{J,2}X_{J,1}X_{J,0}X_{J,2n-1} \dots X_{J,3}) - \\ & (X_{I,2}X_{I,1}X_{I,0}X_{I,2n-1} \dots X_{I,3})|_{2^{2n-1}} \rightarrow \\ V_2 &= (X_{J,2}X_{J,1}X_{J,0}X_{J,2n-1} \dots X_{J,3}) + \\ & (\overline{X_{I,2}X_{I,1}X_{I,0}X_{I,2n-1} \dots X_{I,3}}) \end{aligned} \quad (24)$$

Therefore, in accordance with the MRC formula, X is calculated as (25).

$$\begin{aligned} X &= V_1 + V_2P_1 + V_3P_1P_2 + \dots + V_n \prod_{i=1}^{n-1} P_i \rightarrow (25) \\ X &= V_1 + V_2P_1 \rightarrow \\ X &= X_J + V_2(2^{2n} - 9) = X_J + 2^{2n}V_2 - 2^3V_2 - \\ V_2 &\rightarrow \\ X &= \overbrace{(0 \dots 0}^{2n} \overbrace{X_{J,2n-1} \dots X_{J,0}}^{2n}) + \\ & \overbrace{(V_{2,2n-1} \dots V_{2,0} \overbrace{0 \dots 0}^{2n})}^{2n} - \overbrace{(0 \dots 0 \overbrace{V_{2,2n-1} \dots V_{2,0}}^{2n} \overbrace{000}^3)}^{2n} - \\ & \overbrace{(0 \dots 0 \overbrace{V_{2,2n-1} \dots V_{2,0}}^{2n})}^{2n} \end{aligned}$$

Thus, (25) can be rewritten as (26):

$$\begin{aligned} X &= \overbrace{(V_{2,2n-1} \dots V_{2,0} \overbrace{X_{J,2n-1} \dots X_{J,0}}^{2n})}^{2n} + \\ & \overbrace{((1 \dots 1 \overbrace{V_{2,2n-1} \dots V_{2,0}}^{2n} \overbrace{111}^3) + (1 \dots 1 \overbrace{V_{2,2n-1} \dots V_{2,0}}^{2n}))}^{2n} + \\ & \overbrace{2}^2 \end{aligned} \quad (26)$$

The structure of the proposed reverse converter is shown in Fig. 2.

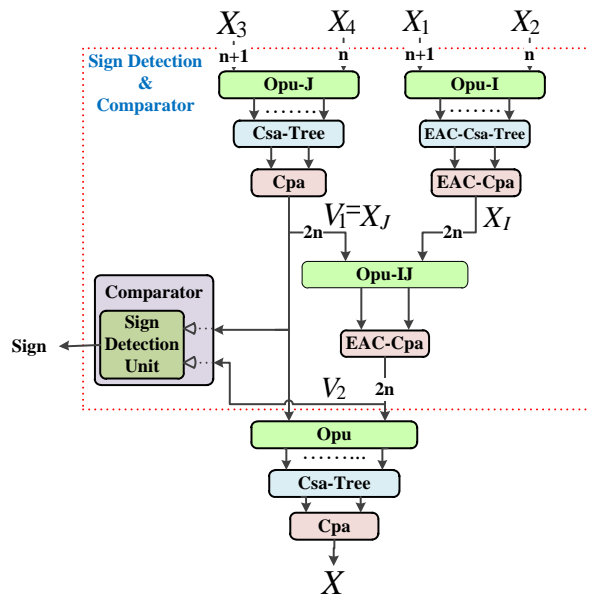


Fig. 2. The structure of the proposed multifunctional unit including reverse convertor, sign detection, and magnitude comparison.

Since detecting the signed numbers is considered a prerequisite for assessing the magnitude of the signed numbers in the RNS, we first discuss sign detection in section 5 and then extend magnitude comparison in section 6.

5. SIGN DETECTION

The reason why the residue number system is not as pervasive and common is that this system contains a number of difficult and complex operations, for instance division, overflow detection, magnitude comparison, and sign detection. Therefore, for the first time for the $\{2^n + 1, 2^n - 1, 2^n + 3, 2^n - 3\}$ moduli set, a sign detection and a magnitude comparison circuit have been presented. However, in [33] using a similar method, a sign detection circuit has been provided for the five-module set $\{2^{2n}, 2^n + 1, 2^n - 1, 2^n + 3, 2^n - 3\}$, to which a comparator circuit has been added. The inspiration for this article is taken from [31-33] and will be further discussed later on.

Generally, the residue number system has been used for unsigned positive numbers and the reverse convertor output generates an unsigned value. Therefore, in order to implement this system for signed numbers, the output of the reverse convertor should be modified. At first, the common method to detect the sign of the number was to compare the output of the reverse convertor with half of the dynamic range of $M/2$, as illustrated in Fig.3.

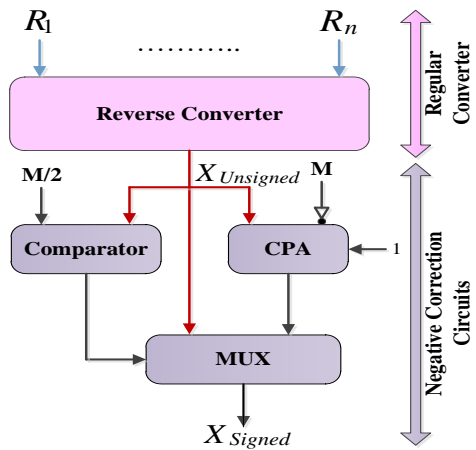


Fig. 3. signed reverse converter using the traditional method [31].

In this section, the target is designing an efficient unit for detecting the sign by using a comparator and multiplexer in the reverse convertor output to detect the sign. Hence, to detect the sign of the 4-moduli set $\{2^n + 1, 2^n - 1, 2^n + 3, 2^n - 3\}$, the presented methods in [31-33] have been utilized. Fig.4 illustrates the spectrum of positive and negative numbers in the 4-moduli set $\{2^n + 1, 2^n - 1, 2^n + 3, 2^n - 3\}$.

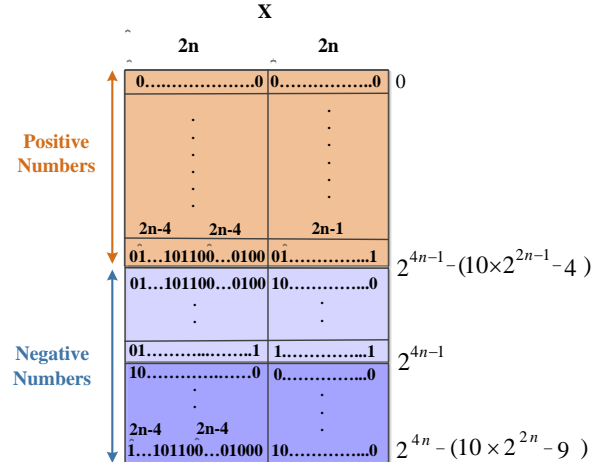


Fig 4. The distribution of the dynamic range.

As illustrated in Fig. 4, the dynamic range is divided into two parts. The numbers within the range of $[0, 2^{4n-1} - (10 \times 2^{2n-1} - 4)]$ have the MSB of zero and they are situated within the spectrum of positive numbers. However, the MSB of the numbers within the range of $[2^{4n-1} - (10 \times 2^{2n-1} - 4), 2^{4n-1}]$ is one and they are situated within the spectrum of negative ones. The numbers within the range of $[2^{4n-1}, 2^{4n} - (10 \times 2^{2n} - 9)]$ also have MSB of one but they are located in the spectrum of negative numbers. In other words, the numbers within the range of $[2^{4n-1} - (10 \times 2^{2n-1} - 4), 2^{4n-1}]$ - which is the range of challenge - have MSB of zero, but they are situated

within the spectrum of negative numbers. Having overcome this challenge, the sign can be calculated.

The structure of the reverse converter allows us to find an effective method to detect the sign. It is worth noting that one method for detecting the sign is to take into consideration the dynamic range, where $X \in [0, M/2)$ or $X \in [M/2, M)$, is an indication of the positive or negative spectrum of the residue number system. When $V_2 \neq \frac{P_1-1}{2}$, the spectrum of the numbers taken into account for V_2 is divided into two parts; the MSB bit value of the upper part is zero and X is situated within the spectrum of positive numbers and the MSB bit value of the lower part is one and X is situated within the spectrum of negative numbers. When $V_2 = \frac{P_1-1}{2}$, we need to put V_1 under scrutiny in order to detect the sign of X . Therefore, when $V_1 > \frac{P_1-1}{2}$, X is situated within the spectrum of negative numbers, otherwise X is situated within the spectrum of positive numbers.

$$V_1 = X_j \quad (27)$$

$$V_1 = x_3 + P_3 |K_j(x_4 - x_3)|_{P_4} \quad (28)$$

$$V_2 = |(X_j - X_l)|_{P_1^{-1}|_{P_2}} \quad (29)$$

$$X = V_1 + P_1 V_2 \quad (30)$$

$$P_N = (2^{2n} - 9) \quad (31)$$

$$P_M = (2^{2n} - 1) \quad (32)$$

Thus, using (27) to (38), we can detect the sign.

$$Sign = (V_{2,2n-1} \vee L) \rightarrow Sign = \begin{cases} 0 & + \\ 1 & - \end{cases} \quad (33)$$

$$L = (L_1 \wedge (L_2 \vee L_3)) \quad (34)$$

$$L_1 = (\bar{V}_{2,2n-1} \wedge V_{2,2n-2} \cdots \wedge V_{2,0}) \quad (35)$$

$$L_2 = (V_{1,2n-1}) \quad (36)$$

$$L_3 = (\bar{V}_{1,2n-1} \wedge V_{1,2n-2} \cdots \wedge V_{1,2}) \quad (37)$$

$$L = (\bar{V}_{2,2n-1} \wedge V_{2,2n-2} \wedge \cdots \wedge V_{2,0} \wedge (V_{1,2n-1} \vee (\bar{V}_{1,2n-1} \wedge V_{1,2n-2} \wedge \cdots \wedge V_{1,2}))) \quad (38)$$

Having detected the sign, if it is negative, we need to modify the output of the reverse converter. Therefore, if a sign detection circuit produces one, the output is negative and it should be modified. If \hat{X} indicates a signed outcome, then the value of \hat{X} can be obtained based on (39) and (40).

$$\hat{X} = X - M \quad (39)$$

$$M = (2^{2n} - 1)(2^{2n} - 9) = (2^{4n} - 10 \times 2^{2n} + 9) \quad (40)$$

The complement of two values of M is a $4n$ bit number that is expressible as (41).

$$2^{4n} - M = 2^{4n} - (2^{4n} - (10 \times 2^{2n} - 9)) = (10 \times 2^{2n} - 9) \quad (41)$$

Now, to modify the output of the reverse converter, if negative, the $(10 \times 2^{2n} - 9)$ value must be added to the output. Hence, if needed, the hardware presented in Fig 5 can be used as the output modifying circuit.

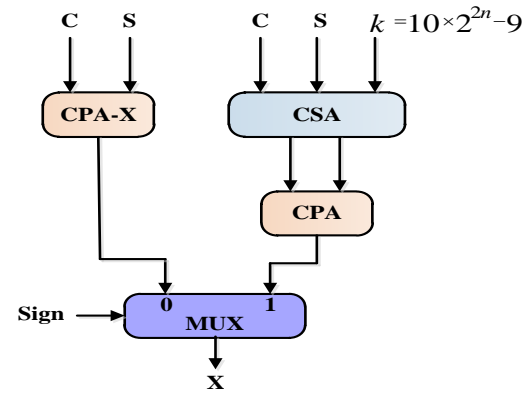


Fig. 5. The output modifier circuit [33].

6. SIGNED COMPARATOR

The residue number system is a non-weighted numerical system. Hence, comparing the numbers in this system is difficult and complicated, especially when the comparison takes place between two signed numbers, unlike the case with the binary numerical system. Here, we show how we compare signed numbers for the selected moduli set based on the formulas of the reverse converter. In sign detection, we have used the parallel method for the operation, therefore, we can also use the parallel method to compare two signed numbers in the residue number system. This method could be used for comparing the two numbers, X and Y , in the residue number system. As it is apparent, we have used the New-CRT-I and the MRC method to detect the signs of these two numbers. Therefore, this method has also been used to compare the two signed numbers. According to the MRC method, $X = V_{1X} + V_{2X}P_j$ and $Y = V_{1Y} + V_{2Y}P_j$ and also $P_j = (2^{2n} - 9)$, the V_{1X}, V_{2X}, V_{1Y} and V_{2Y} values alongside with signs are calculated in a parallel manner. Through an analytical analysis, it becomes apparent that when two numbers have different signs, the positive number is the bigger one in the set, otherwise when the two numbers have the same sign, first V_{2X} and V_{2Y} values should be compared and then the bigger number is considered the biggest. If V_{2X} and V_{2Y} are equal, V_{1X} and V_{1Y} values should be analyzed and compared. The outcome of this analysis determines the bigger number. This means that if V_{1X} and V_{1Y} values are equal, the final product portrays that X and Y values are equal and if V_{1X} is bigger than V_{1Y} , X is bigger than Y and vice versa. Also, this comparator circuit for the signed numbers of the residue number system is expressible using (42) to (44).

$$E = ((Sign(X) \oplus Sign(Y)) \wedge (V_{2X} =$$

$$V_{2Y}) \wedge (V_{1X} = V_{1Y})) \quad (42)$$

$$G = \overline{(\text{Sign}(X) \wedge \text{Sign}(Y)) \vee [(\text{Sign}(X) \oplus \text{Sign}(Y)) \wedge [(V_{2X} > V_{2Y}) \vee [(V_{2X} = V_{2Y}) \wedge (V_{1X} > V_{1Y})]]]} \quad (43)$$

$$L = (\overline{E} \vee G) \quad (44)$$

This operation is shown in Fig. 1 (Algorithm 1). As soon as the signs of the two numbers are detected, this operation becomes calculable. While the method of comparing two signed numbers is obtained with a little delay, it needs a vast area since comparing the two numbers requires two parallel reverse converters (Fig.7).

Algorithm 1 : Signed magnitude comparison

This method can be adapted for the comparison of two RNS numbers, X and Y

function Comparison($X_1, \dots, X_n, Y_1, \dots, Y_n$)

 Compute $\text{Sign}(X), \text{Sign}(Y), V_{1X}, V_{2X}, V_{1Y}, V_{2Y}$;

If ($\text{Sign}(X) = \text{Sign}(Y)$) **Then**

If ($V_{2X} = V_{2Y}$) **Then**

If ($V_{1X} = V_{1Y}$) **Then**

$COMP \leftarrow E$; ▶ ($X = Y$)

Else

If ($V_{1X} > V_{1Y}$) **Then**

$COMP \leftarrow G$; ▶ ($X > Y$)

Else

$COMP \leftarrow L$; ▶ ($X < Y$)

End;

End;

Else

If ($V_{2X} > V_{2Y}$) **Then**

$COMP \leftarrow G$; ▶ ($X > Y$)

Else

$COMP \leftarrow L$; ▶ ($X < Y$)

End;

End;

Else

If ($\text{Sign}(X) = 0$) **Then**

$COMP \leftarrow G$; ▶ ($X > Y$)

Else

$COMP \leftarrow L$; ▶ ($X < Y$)

End;

End;

Return $COMP$;

End Function;

Fig. 6. Algorithm of the comparing two proposed signed numbers.

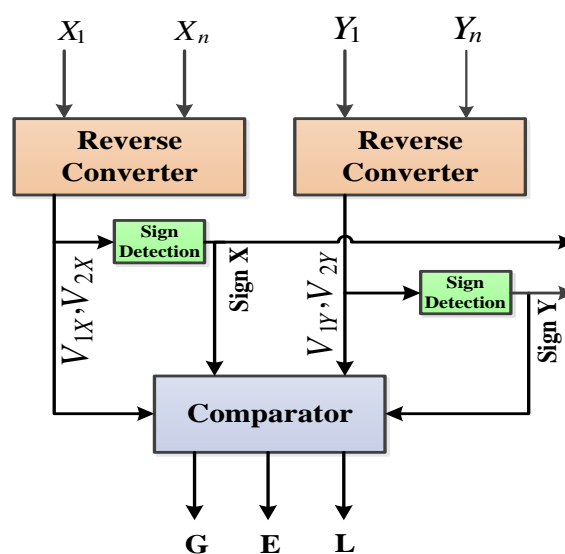


Fig.7. The block diagram of the proposed signed comparator unit.

The presented method for comparing two signed numbers could easily be converted into a sequential method using the two cycles of the clock. The output values get stored in the register and eventually, after producing the second output, the logic of the comparison could be completed.

7. EXAMPLE

This section presents a numerical example. Supposed that we plan to obtain the sign of an RNS number based in the $\{2^n + 1, 2^n - 1, 2^n + 3, 2^n - 3\}$ moduli set. If we consider $n = 3$ for this moduli set, $\{9, 7, 11, 5\}$ values are obtained and the dynamic range equals 3465. Now, suppose that we want to detect the sign of the residue number (5, 4, 6, 3) that is equal to the binary value 1733.

According to the presented definitions, if $X \in [0, 1732]$, then X is positive, and if $X \in [1733, 3464]$, then X is negative. Therefore, the value 1733 is situated within the spectrum of negative numbers, so we have to obtain $1733 - 3465 = -1732$ as the output of the reverse converter in order to modify the output. Thus, the structure of the proposed reverse converter produces the complement of two values of -1732 which is equal to 2364.

$$X = 1733 \xRightarrow{RNS} (5,4,6,3)$$

Therefore, the values X_j, X_l, V_1, V_2 , and Sign are as follows.

$$\begin{aligned} X_j &= 5 + 9|4(4 - 5)|_7 = 32 \\ X_l &= 6 + 11|(3 - 6)|_5 = 28 \\ V_1 &= 28 \\ V_2 &= |(28 - 32)8|_{63} = 31 \end{aligned}$$

$$\frac{P_{J-1}}{2} = 27$$

$$\frac{P_{I-1}}{2} = 31$$

Given the fact that $V_2 = 31$, we need to analyze the value of V_1 in order to detect the sign. Considering that $V_1 = 28$ and $V_1 > 27$, the sign of X is, therefore, negative.

$$L_1 = (\bar{V}_{2.2n-1} \wedge V_{2.2n-2} \cdots \wedge V_{2.0}) = 1$$

$$L_2 = (V_{1.2n-1}) = 0$$

$$L_3 = (\bar{V}_{1.2n-1} \wedge V_{1.2n-2} \cdots \wedge V_{1.2}) = 1$$

$$L = (\bar{V}_{2.2n-1} \wedge V_{2.2n-2} \wedge \cdots$$

$$\cdot \wedge V_{2.0} \wedge (V_{1.2n-1} \vee (\bar{V}_{1.2n-1} \wedge V_{1.2n-2} \wedge \cdots \wedge V_{1.2}))$$

$$L = (L_1 \wedge (L_2 \vee L_3)) = 1$$

$$\text{Sign} = (V_{2.2n-1} \vee L) = 1$$

Now, if the sign of X is negative, we need to modify the output of the reverse convertor. To modify the output, the value $(10 \times 2^{2n} - 9)$ should be added to the output. This operation is shown through the circuit presented in Fig.8.

$$X = 1733, \quad M = 3465 \rightarrow \hat{X} = X - M = 1733 - 3465 = -1732$$

$$\hat{X} = -1732 = -(011011000100)$$

$$\xrightarrow{2's \text{Complement}} (100100111100) = 2364$$

Therefore, the output is 2364.

8. THE ANALYTICAL EVALUATION

In order to analyze performance and efficiency, we compare the proposed hardware with the designs in [22-23], which possesses the greatest efficiency among the presented methods. In this section, we evaluate delay and the area of each design based on its core components including the Full Adder (FA), Half Adder (HA), multiplexer (MUX), and the basic gates (G). Therefore, the time delay and the area of each part is D_{FA} , D_{HA} , D_{MUX} , D_G and A_{FA} , A_{HA} , A_{MUX} , A_G , respectively. The delay and the logic gate level of XOR are $2D_G$ and $3A_G$, respectively. It is worth noting that the logarithmic terms are related to the number of levels or the so-called CSA tree structure. Since some parts of the modeled circuits are identical with the main resource presented in [22-23] and do not include significant changes, it has been taken into consideration with the values of the main resource from a hardware analysis point of view. As Fig.1. and Fig.2. illustrate, inside the internal structure of OPU, rotational operations, shift, and complement of one take place. CSA-n bit area is considered equal to n FAs and its delay equal to one FA; also, the area and delay of one CPA-n bit is considered equal to n FAs. Table 1 and Table 2 present the analytical evaluations of the original [22-23] and proposed designs.

Table 1. Analytical evaluation of [22].

Component	Delay	Area
X_I	N/A (it is not on the critical delay path)	$(2n + 2)A_{FA}$ + $(2n - 2)A_{HA}$ + $(4n - 1)A_G$
X_J	$(3n + \lceil \log 2n \rceil + 2)D_{FA}$	$(2n^2 + 2n + 2)A_{F.A}$ + $(n)A_{HA}$
OPU-II	D_G	$(2n)A_G$
CPA	$(2n)D_{FA}$	$(2n)A_{FA}$
OPU	$(2)D_G$	$(6n)A_G$
CSA Tree	$(2)D_{FA}$	$(4n + 1)A_{FA}$
CPA	$(4n)D_{FA}$	$(4n)A_{FA}$
Total Reverse	$(9n + \lceil \log 2n \rceil + 4)D_{F.A} + (3)D_G$	$(2n^2 + 14n + 5)A_{FA}$ + $(3n - 2)A_{HA}$ + $(12n - 1)A_G$

Table 2. Analytical evaluation of the proposed design.

Component	Delay	Area
X_I	N/A (it is not on the critical delay path)	$(2n + 2)A_{FA}$ + $(2n - 2)A_{HA}$ + $(4n - 1)A_G$
X_J	$(3n + \lceil \log 2n \rceil + 2)D_{FA}$	$(2n^2 + 2n + 2)A_{F.A}$ + $(n)A_{HA}$
OPU-II	D_G	$(2n)A_G$
CPA	$(2n)D_{FA}$	$(2n)A_{FA}$
Sign Detection	$(\lceil \log 4n \rceil + 1)D_G$	$(4n + 3)A_G$
Total Sign	$(5n + \lceil \log 2n \rceil + 2)D_{FA}$ + $(\lceil \log 4n \rceil + 2)D_G$	$(2n^2 + 6n + 4)A_{FA}$ + $(3n - 2)A_{HA}$ + $(10n + 2)A_G$
OPU	D_G	$(8n)A_G$
CSA Tree	$(2)D_{FA}$	$(4n + 1)A_{FA}$
CPA	$(4n)D_{FA}$	$(4n)A_{FA}$
Total Reverse And Sign	$(9n + \lceil \log 2n \rceil + 4)D_{F.A}$ + $(\lceil \log 4n \rceil + 3)D_G$	$(2n^2 + 14n + 5)A_{FA}$ + $(3n - 2)A_{HA}$ + $(18n + 2)A_G$

Since the main aim of this work is to present a method for extracting the sign and comparing the magnitude of two numbers inside the reverse convertor, we extract the sign using the comparator and reverse convertor in [22] and compare it with the extracted sign in the proposed method. Therefore, through analytical

evaluation, the occupancy area and the delay for the [22] reverse converter, using (45) to (53), are considered.

$$A_{Sign_Regular} = A_{Reverse_Converter} + A_{Comparator} + A_{Cpa} + A_{Mux_{2 \times 1}} \quad (45)$$

$$A_{Reverse_Converter} = (2n^2 + 14n + 5)A_{FA} + (3n - 2)A_{HA} + (12n - 1)A_G \quad (46)$$

$$A_{Comparator} = (12n - 2)A_{And} + (4n - 1)A_{Or} + (4n - 1)A_{Xor} \quad (47)$$

$$A_{Cpa} = (4n)A_{FA} \quad (48)$$

$$A_{Sign_Regular} = \frac{A_{Reverse_Converter} + A_{Cpa}}{(2n^2 + 18n + 5)A_{FA} + (3n - 2)A_{HA} + (12n - 1)A_G + A_{Comparator}} + \frac{(12n - 2)A_{And} + (4n - 1)A_{Or} + (4n - 1)A_{Xor} + A_{Mux_{2 \times 1}}}{(6n)A_{Mux_{2 \times 1}}} \quad (49)$$

IT should be noted that the delay of comparator overlaps with the CPA delay, an due to this it has not been taken into consideration.

$$D_{Sign_Regular} = D_{Reverse_Converter} + D_{Cpa} + D_{Mux_{2 \times 1}} \quad (50)$$

$$D_{Reverse_Converter} = (9n + [\log 2n] + 4)D_{FA} + (3)D_G \quad (51)$$

$$D_{Cpa} = (4n)D_{FA} \quad (52)$$

$$D_{Sign_Regular} = \frac{D_{Reverse_Converter} + D_{Cpa}}{(13n + [\log 2n] + 4)D_{FA} + (3)D_G + D_{Mux_{2 \times 1}}} + D_{Mux_{2 \times 1}} \quad (53)$$

The occupancy area and the delay of the proposed design are also expressed using (54) to (57).

$$A_{Sign_Proposed} = A_{X1} + A_{V1} + A_{V2} + A_{Sign} \quad (54)$$

$$D_{Sign_Proposed} = D_{X1} + D_{V1} + D_{V2} + D_{Sign} \quad (55)$$

The occupancy area and the delay for the proposed design are obtained based on (54) and (57). Nonetheless, since $D_{Sign} \cong D_{V1} + D_{V2}$ and that the value of D_{Sign} overlaps with the calculation of D_{V2} and that its delay is insignificant against the calculation of the value of D_{V2} , we disregard it.

$$A_{Sign_Proposed} = \frac{A_{X1} + A_{V1} + A_{V2}}{(2n^2 + 6n + 4)A_{FA} + (3n - 2)A_{HA} + (6n - 1)A_G + A_{Sign}} + (4n + 3)A_G \quad (56)$$

$$D_{Reverse_Converter} = \frac{D_{X1} + D_{V1} + D_{V2}}{(5n + [\log 2n] + 2)D_{FA} + D_G + D_{Sign}} + ([\log 4n] + 1)D_G \quad (57)$$

9. THE EXPERIMENTAL EVALUATION

In this section, we analyze and evaluate the important circuits parameters in designing a signed reverse converter and a magnitude comparator for 4-moduli set $\{2^n + 3 \cdot 2^n - 3 \cdot 2^n + 1 \cdot 2^n - 1\}$. Considering that this work is proposing the signed reverse converter and magnitude comparator for this moduli set for the first time, its evaluation takes place in comparison with the unsigned reverse converter proposed in [22]. We have utilized the ISE Design Suite 14.7 tool, and the results of this analysis are presented in Tables 3 and 4 using the Spartan6 family technology. In this work, [22] which is the latest work presented in this context, has been used for comparison purposes.

Table 3. The Delay of different designs (ns).

n	[22] With Sign	[22] With Sign & Magnitude	Proposed With Sign	Proposed With Sign & Magnitude
3	24.40	31.03	15.72	23.18
4	29.41	35.70	21.11	28.72
5	34.29	42.94	26.47	31.30
6	38.66	50.37	30.99	36.18
7	43.50	55.98	35.01	39.80
8	47.97	61.13	39.47	42.54

Table 4. The Area of different designs (LUT).

n	[22] With Sign	[22] With Sign & Magnitude	Proposed With Sign	Proposed With Sign & Magnitude
3	102	227	61	155
4	153	323	98	222
5	198	421	122	277
6	238	501	151	348
7	272	578	168	394
8	316	664	201	475

According to the evaluations presented in Tables 3 and 4, the delay and area of the proposed circuits are compared with the initial design, in which two numbers should be taken out of the reverse converter. These also bring about an improvement in the Area-Delay-Product (ADP), as shown in Fig.8.

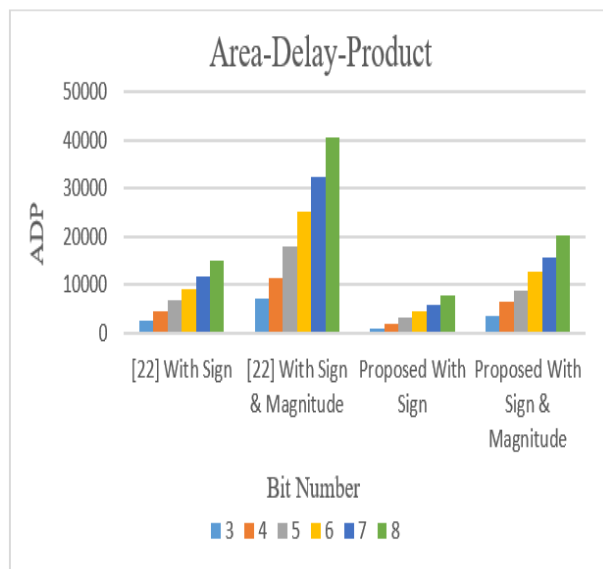


Fig. 8. The ADP Evaluation.

10. CONCLUSION

In this paper, the signed reverse converter and the magnitude comparator for the 4-moduli set $\{2^n + 3, 2^n - 3, 2^n + 1, 2^n - 1\}$ have been proposed for the first time. The proposed unit utilizes a hardware that works in a parallel manner with the converter and extracts and produces the signed outcome and perform magnitude comparison of numbers from the inside of the reverse converter. We have also presented the first sign detection unit and the magnitude comparator of two numbers for the moduli set. The evaluation results indicate a considerable improvement in the proposed method compared with the typical reverse converter [22] that uses a comparator in the output of the reverse converter to detect the sign. Experimental results show that the proposed converter, alongside with the sign detection circuit and the magnitude comparator of two numbers, possesses 46% and 37% improvement in terms of area and 28% and 30% improvement in terms of delay compared with the unsigned reverse converter [22] that requires the exclusion of two numbers in order to detect the sign and compare, respectively. Currently, the proposed model cannot appear scalable for other similar moduli sets. In addition, multiplicative inverses for this moduli set result in complicating the hardware and overloading the converter. Also, further studies could perhaps propose a model that entails a component including a sign detecting circuit, a comparator, and scaling for a particular group of moduli sets in the $\{2^p - 1, 2^{2n} - \delta\}$ form.

11. APPENDIX

The full list of symbols used throughout the paper is shown in Table 5.

Table 5. The list of symbols used in the paper.

Symbol	Description
RNS	Residue number system
CRT	Chinese remainder theorem
MRC	Mixed radix conversion
D_R	Dynamic range
OPU	Operand preparation unit (Shift & Route)
CSA	Carry save adder
CPA	Carry propagate adder
EAC	End around carry
FA	Full adder
HA	Half adder

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