A 57-64 GHz High-gain Amplifier using Ultra-wideband Inductors in the IMNs and Optimization by PCA and SDSM

Ahmadali Ashrafian[1], Mahmoud Mohammad-Taheri [2*], Mohammad Naser-Moghaddasi[1], Mehdi Khatir[1], Behbod Ghalamkari[1]

1- Department of Electrical and Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran.
Email: ahm.ashrafian@iauctb.ac.ir, mn.moghaddasi@srbiau.ac.ir, m-khatir@srbiau.ac.ir, ghalamkari@srbiau.ac.ir

2- School of Electrical and Computer Engineering, College of Engineering University of Tehran, Tehran, Iran.
Email: mtaheri@ut.ac.ir (Corresponding author)

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ABSTRACT:
In this paper, the design and optimization of a cascaded common source four-stage millimeter wave amplifier in a 130 nm CMOS technology has been presented. First, Pi-shaped wideband impedance matching networks (IMNs) were used in the Input/Output Impedance Matching Networks (IOIMNs) and inter-stages. Next, single stubs were converted to symmetrical double stubs in the IOIMNs, and an ultra-wideband inductor replaced each stub. Ultra-wideband inductors were also used in series in the inter-stage IMNs to achieve a higher gain in the wider frequency bandwidth. Then, the impedance matrices of IOIMNs and inter-stage were calculated using Planar Circuit Analysis (PCA), which is based on the planar waveguide model and Segmentation/Desegmentation Methods (SDSMs). Finally, by optimizing the length and characteristic impedance of each segment of microstrip line in the IMNs through using an intelligent optimization algorithm in MATLAB, the excellent IMNs were designed, which resulted in an amplifier with $S_{11\min} = -25.3dB$, $S_{22\min} = -20.6\,dB$, and $S_{21\max} = 30.5\,dB$ in the frequency range of 57- 64 GHz. With this design method, in addition to incorporating the effect of discontinuities, the fringing fields at the edges of the microstrip as well as the conductor and dielectric losses, the effect of dispersion would be minimized by choosing a substrate whose thickness is much smaller than the wavelength and its relative permittivity is low.

KEYWORDS: Millimeter-Wave Amplifier, Impedance Matching Networks, Planar Circuit Analysis, Segmentation, Desegmentation, Discontinuity Effect, Dispersion Effect.

1. INTRODUCTION

With attention to the daily increasing in mobile users and the use of smartphones, tablets, etc., for watching videos, photo sharing, and browsing the Internet, the transferring of information with high data rate and large capacity are the internet's main requirements. To fulfill such need, the millimeter-wave spectrum is used in the fifth generation Internet (5G). The millimeter-wave amplifiers are one of the circuits required for this frequency spectrum. In the design of these amplifiers, by the appropriate input/output and inter-stage impedance matchings, the returned power decreases, and the transmitted power increases, which in turn increases the gain. The transmission line impedance matching networks for millimeter-wave amplifiers have been implemented in low noise amplifier [1-7], high-gain low noise amplifier [8], wideband low noise amplifier [9], distributed amplifier for ultra-wideband application [10], ultra-low power low noise amplifier [11], low-power high-gain amplifier [12], low power amplifier [13], power amplifier [14-18], wideband power amplifier [19-21], and millimeter-wave amplifiers [22-25]. However, only the simulated results have been provided in these references, and no solutions were proposed analytically to optimize the networks.

In this paper, after the proper design of Pi-shaped wideband input/output and inter-stage impedance matching networks with minimum lumped elements and their implementation with microstrip lines, to achieve a wider bandwidth, the ultra-wideband inductor [26] is used instead of the usual transmission line stub [3], [12], [23], [27] or spiral inductor [15], which were used in most previous articles. Then, using the planar circuit analysis approach based on the planar waveguide model and SDSMs, the overall impedance

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matrix of matching networks is analytically calculated with high accuracy and minimum computation time. Finally, by optimizing the effective parameters in the impedance matrix of matching networks such as, length and characteristic impedance of each rectangular segment by an intelligent optimization algorithm in MATLAB [26], we were able to achieve the main goal of this paper, which is to design an amplifier with a gain of more than 30 dB (S21max = 30.5dB) in the frequency range of 57 to 64 GHz, and as well excellent input impedance matching (S11min = -25.3dB) and output impedance matching (S22min = -20.6). It should also be noted that the 57 to 64 GHz bandwidth is an IEEE 802.11 wireless networking standard for WiGig networks. Full-wave numerical methods used in commercial HFSS and ADS simulators to calculate the transfer functions of impedance matching networks have not been used in this paper because the numerical methods are time-consuming, and this makes it impossible to optimize transfer functions using an algorithm in a limited and appropriate time.

The input/output impedances of the transistor in a 130 nm CMOS technology in the frequency range of 60 GHz are capacitive. Impedance matching networks with the minimum number of elements that to be used for the input /output impedance matchings of a transistor to a 50Ω source and a 50 Ω load, respectively, are L-shaped impedance matching networks. Since these matching networks are designed with two elements, they occupy little space and minimize the conductor and dielectric losses.

The L-shaped matching networks used at the input with gate-source capacitor and the output with drain-source capacitor form Pi-shaped wideband matching impedance networks. Since the Pi-shaped matching networks designed at the input/output are terminated to a 50-ohm source and a 50-ohm load, respectively, the Q-factor of these networks is low, which makes them wideband.

To achieve the maximum gain in the desired bandwidth after the realization of L-shaped impedance matching networks with microstrip lines at the input and output of the amplifier, first the single stubs are converted to the symmetric double stubs. These stubs are then replaced with ultra-wideband inductors[26]. To optimize the obtained impedance matching networks, it is necessary to calculate their overall impedance matrix analytically, with high accuracy and minimum computation time. By selecting a substrate whose dielectric constant is small and its thickness is much less than the wavelength, while minimizing the dispersion effect, the overall impedance matrix of IOIMNs can be calculated analytically with high accuracy and in a very short time using PCA [28], which is based on the planar waveguide model [29], segmentation [30-32] and desegmentation [33] methods. Using this design method, the effect of fringing fields at the edges of microstrip lines, conductor and dielectric losses and the effect of discontinuities between microstrip line segments are also taken into account. Finally, by optimizing the parameters that play an essential role in the transfer function of impedance matching networks, such as length and characteristic impedance of each microstrip rectangular segment through an intelligent optimization algorithm, the amplifier with excellent IOIMNs is designed.

In the design of inter-stage impedance matching networks, since the output impedance of each stage and the input impedance of the next stage are capacitive, by adding a piece of microstrip line that has inductive performance in series with them, a Pi-shaped impedance matching network is formed. In this way, higher gain and wider frequency bandwidth can be achieved than the matching networks between the stages used in [12], [15], and [23], which have used a stub parallel to the input and output of the stages.

In this paper, to achieve a wider frequency bandwidth, instead of one piece of the microstrip line, an ultra-wideband inductor consists of three cascaded rectangular microstrip line segments in non-equal and variable characteristic impedances is used. Then, the overall impedance matrix of three segments is calculated using PCA and SDSMs. Finally, the length and characteristic impedance of each rectangular piece is optimized using an intelligent algorithm in MATLAB.

It should be noted that using PCA and SDSMs applied to the equivalent planar waveguide model, the impedance matrix of impedance matching networks can be calculated analytically. Since the impedance matrix calculation results obtained analytically are accurate and the calculation time is very short, through an intelligent algorithm, we can optimize parameters such as the length and characteristic impedance in each segment of the microstrip line that play an essential role in the design of the matching network. This optimization has been done to realize a millimeter wave amplifier with the maximum gain in the frequency range of 57 to 64 GHz. However, this optimization is not possible in commercial full-wave simulators such as HFSS and ADS, because the analysis of impedance matching networks is done using numerical methods that require a relatively long time.

The proposed method can be used in the design and optimization of various millimeter-wave circuits such as amplifiers (low noise, high efficiency, wideband, power, etc.), modulators (PSK, QPSK, etc.), mixers, and types of filters (lowpass, bandpass, bandstop, etc.).

2. DESIGN OF IMPEDANCE MATCHING NETWORKS

In the following sections, the design and optimization of input/output and inter-stage impedance matching networks are examined.

2.1. Design of Amplifier Input Impedance Matching Network

Using a piece of microstrip transmission line and a stub as shown in Fig. 1a, the input impedance of the amplifier, consisting of intrinsic parameters of R_{gs} and C_{gs} can be matched to a 50-ohm source. To achieve an impedance matching network with a wider frequency bandwidth, two symmetric stubs instead of one stub can be used, as shown in Fig. 1b.

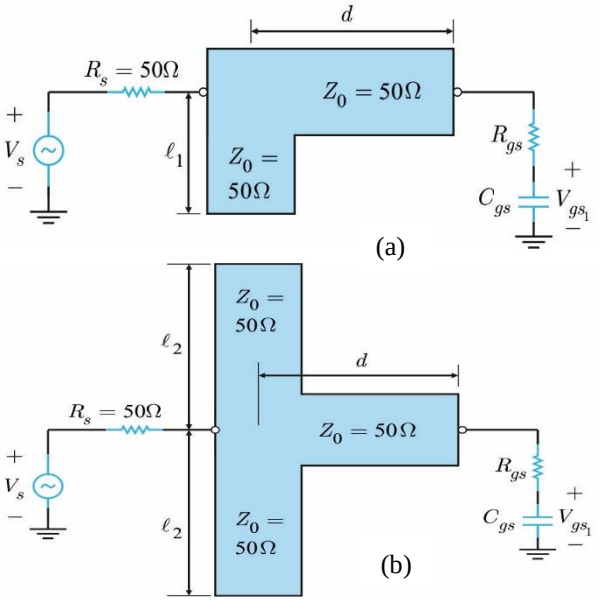

Fig. 1. Input impedance matching network using (a) a piece of microstrip transmission line and a stub (b) two symmetric stubs instead of one stub.

To calculate and optimize the transfer function of the input matching network, a matching network impedance matrix shown in Fig. 1b is required. To calculate the impedance matrix, the Green‘s function of this set is required, which is not available, so first, it is necessary to decompose the matching network of Fig. 1b into rectangular segments whose Green‘s function is available (see Fig. 2a). Next, using Green's function of each rectangular segment, the impedance matrix of that segment can be calculated.

Since in operating frequency of 57 to 64 GHz, the width of each coupling port is comparable to the wavelength, each port is divided into three subports so that the injected current in each subport width can be assumed to be uniformly (see Fig. 2a). Then, considering the location of the subports, the impedance matrix is calculated for each rectangular segment.

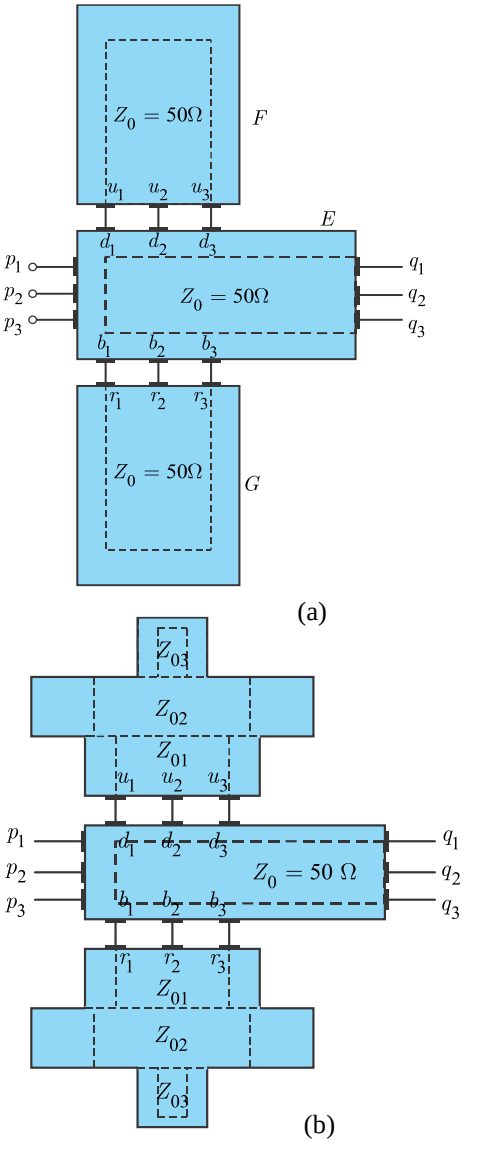

Fig. 2. (a) Segmentation of configuration of Fig. 1b into regular segments (b) replacing stubs F and G with ultra-wideband inductor realized by three-segment microstrip.

The impedance matrix of the rectangular segment E ($\overline{Z}_E$), which has 12 subports, and the symmetric stubs of F $(\overline{Z}_F)$, and G $(\overline{Z}_G)$, which have three subports, as shown in Fig. 2a, are expressed in the following general form as[26]:

$$\bar{Z}_E = \begin{matrix} \bar{Z}^E_{pp} & \bar{Z}^E_{pb} & \bar{Z}^E_{pd} & \bar{Z}^E_{pq} \\ \bar{Z}^E_{bp} & \bar{Z}^E_{bb} & \bar{Z}^E_{bd} & \bar{Z}^E_{bq} \\ \bar{Z}^E_{dp} & \bar{Z}^E_{db} & \bar{Z}^E_{dd} & \bar{Z}^E_{dq} \\ \bar{Z}^E_{qp} & \bar{Z}^E_{qb} & \bar{Z}^E_{qd} & \bar{Z}^E_{qq} \end{matrix},$$

$$\bar{Z}_G = \bar{Z}^F_{uu},\ \bar{Z}_F = \bar{Z}^G_{rr} \tag{1}$$

The impedance matrix of the amplifier input matching network for subports p and q, with $\bar{i}_r = -\bar{i}_b$, $\bar{i}_u = -\bar{i}_d$, $\bar{v}_r = \bar{v}_b$, $\bar{v}_u = \bar{v}_d$ and expressing $\bar{i}_b$, $\bar{i}_d$ in terms of $\bar{i}_p$, $\bar{i}_q$ in segmentation method is calculated as:

$$[\bar{Z}_t] \begin{matrix} \bar{Z}^E_{pp} & \bar{Z}^E_{pq} & \bar{Z}^E_{pb} & \bar{Z}^E_{pd} \\ \bar{Z}^E_{qp} & \bar{Z}^E_{qq} & \bar{Z}^E_{qb} & \bar{Z}^E_{qd} \\ -(\bar{Z}^G_{rr} + \bar{Z}^E_{bb}) & & -\bar{Z}^E_{bd} & \\ -\bar{Z}^E_{db} & & -(\bar{Z}^F_{uu} + \bar{Z}^E_{dd}) & \end{matrix}^{-1} \begin{matrix} \bar{Z}^E_{bp} & \bar{Z}^E_{bq} \\ \bar{Z}^E_{dp} & \bar{Z}^E_{dq} \end{matrix} \tag{2}$$

To calculate the overall impedance matrix $(\bar{Z}_i)$ of the input matching network with one port at the input and one port at the output, it is necessary to first calculate the admittance matrix $(\bar{Y}_t)$ by inversing the input impedance matrix $(\bar{Z}_t)$ as follows:

$$[\bar{Y}_t] = [\bar{Z}_t]^{-1} = \begin{matrix} \bar{Y}^t_{pp} & \bar{Y}^t_{pq} \\ \bar{Y}^t_{qp} & \bar{Y}^t_{qq} \end{matrix} \tag{3}$$

Where,

$$\bar{Y}^t_{pq} = \begin{matrix} y^t_{14} & y^t_{15} & y^t_{16} \\ y^t_{24} & y^t_{25} & y^t_{26} \\ y^t_{34} & y^t_{35} & y^t_{36} \end{matrix},\ \bar{Y}^t_{pq} = \begin{matrix} y^t_{14} & y^t_{15} & y^t_{16} \\ y^t_{24} & y^t_{25} & y^t_{26} \\ y^t_{34} & y^t_{35} & y^t_{36} \end{matrix},$$

$$\bar{Y}^t_{qp} = \begin{matrix} y^t_{41} & y^t_{42} & y^t_{43} \\ y^t_{51} & y^t_{52} & y^t_{53} \\ y^t_{61} & y^t_{62} & y^t_{63} \end{matrix},\ \bar{Y}^t_{qq} = \begin{matrix} y^t_{44} & y^t_{45} & y^t_{46} \\ y^t_{54} & y^t_{55} & y^t_{56} \\ y^t_{64} & y^t_{65} & y^t_{66} \end{matrix}$$

Then, the overall admittance matrix $(\bar{Y}_i)$ of the input matching network, with one port at the input and one port at the output, can be obtained by combining the subports p and q as follows:

$$\bar{Y}_i = \begin{matrix} y^i_{11} & y^i_{12} \\ y^i_{21} & y^i_{22} \end{matrix} \tag{4}$$

where,

$$y^i_{11} = \sum_{i=1}^{3}\sum_{j=1}^{3} y^t_{ij},\ y^i_{12} = \sum_{i=1}^{3}\sum_{j=4}^{6} y^t_{ij},$$

$$y^i_{21} = \sum_{i=4}^{6}\sum_{j=1}^{3} y^t_{ij},\ y^i_{22} = \sum_{i=4}^{6}\sum_{j=4}^{6} y^t_{ij}$$

By inversing $\bar{Y}_i$, the input matching network impedance matrix $(\bar{Z}_i)$ is calculated as follows:

$$\bar{Z}_i = [\bar{Y}_i]^{-1} = \begin{matrix} Z^i_{11} & Z^i_{12} \\ Z^i_{21} & Z^i_{22} \end{matrix} \tag{5}$$

To improve the impedance matching networks for a wider frequency bandwidth, the ultra-wideband inductors [26] (three rectangular segments of the microstrip line with different characteristic impedances) are used instead of the symmetric stubs in Fig. 2a, as shown in Fig. 2b. Using the impedance matrix of the ultra-wideband inductors instead of the impedance matrix of the stubs F and G in equation (1), the overall impedance matrix of the input matching network is calculated then optimized by an intelligent algorithm.

2.2. Design of Inter-Stage Impedance Matching Networks

Since the input impedance of each stage and the output impedance of the previous stage are capacitive, as shown in Fig. 3a, so the input impedance of each stage can be matched to its previous stage using a piece of microstrip transmission line which acts as an inductor for inter- stage matching networks. To achieve a wider frequency bandwidth, three rectangular microstrip line pieces in non-equal and variable characteristic impedances have been used instead of a

rectangular microstrip line piece in Fig. 3a, as shown in Fig. 3b.

To analyze the impedance matching network in Fig. 3b, it is first necessary to decompose it into three rectangular segments for which the Green's function is available. Each segment has six subports, three subports at the input, and three subports at the output, as in Fig. 4 shows. Then, the impedance matrix of each rectangular segment that has six subports with available Green's function is calculated [26], [30-32]. It should be noted that the impedance matrix of a segment that is wider than its adjacent segments, is necessary to be calculated using the desegmentation method applied to equivalent planar waveguide model [26], [33, 34]. When using this method, in addition to considering the effect of fringing fields, created at the edges due to the discontinuity of the wider segment with its adjacent segments in calculating the impedance matrix of the wider segment, the actual length of the wider segment can also be calculated. Finally, having the impedance matrix of each rectangular segment and applying the segmentation method, the overall impedance matrix of the circuit shown in Fig. 4 whose input and output are at subports p q respectively, is calculated.as follow.

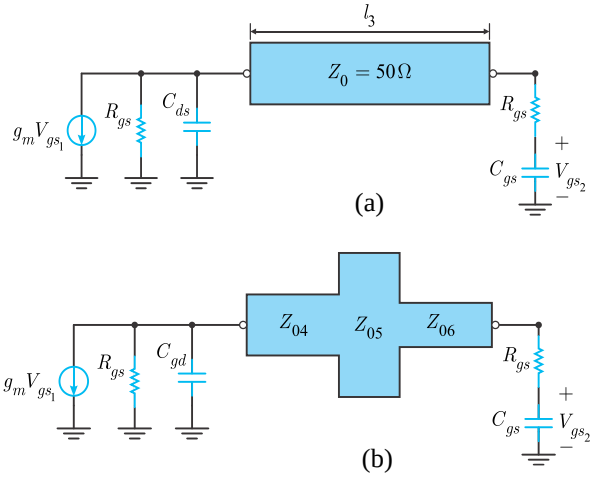

Fig. 3. Inter-stage impedance matching network using (a) microstrip line (b) using three segments with different characteristic impedances instead of one segment for wideband matching.

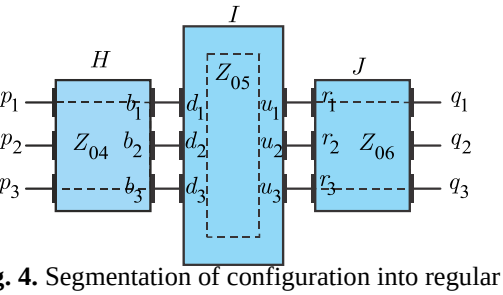

Fig. 4. Segmentation of configuration into regular segments and subports nomenclature.

The impedance matrices of rectangular segments H, I, and J with three subports at the input and three subports at the output as shown in Fig. 4, are expressed in the following general form:

$$\bar{Z}_H = \begin{matrix} \bar{Z}^H_{pp} & \bar{Z}^H_{pb} \\ \bar{Z}^H_{bp} & \bar{Z}^H_{bb} \end{matrix}, \quad \bar{Z}_I = \begin{matrix} \bar{Z}^I_{dd} & \bar{Z}^I_{du} \\ \bar{Z}^I_{ud} & \bar{Z}^I_{uu} \end{matrix},$$

$$\bar{Z}_J = \begin{matrix} \bar{Z}^J_{rr} & \bar{Z}^J_{rq} \\ \bar{Z}^J_{qr} & \bar{Z}^J_{qq} \end{matrix} \tag{6}$$

The overall impedance matrix of segments H and I $(\bar{Z}_{HI})$ considering, $\bar{i}_d = -\bar{i}_b$, $\bar{v}_d = \bar{v}_b$, and expressing $\bar{i}_b$ in terms of $\bar{i}_p$ and $\bar{i}_u$ in segmentation method is calculated as:

$$\bar{Z}_{HI} = \begin{matrix} \bar{Z}^{HI}_{pp} & \bar{Z}^{HI}_{pu} \\ \bar{Z}^{HI}_{up} & \bar{Z}^{HI}_{uu} \end{matrix} \tag{7}$$

Where,

$$\bar{Z}^{HI}_{pp} = \bar{Z}^H_{pp} + \bar{Z}^H_{pb}(\bar{Z}^H_{bb} + \bar{Z}^I_{dd})^{-1}(-\bar{Z}^H_{bp}),$$
$$\bar{Z}^{HI}_{pu} = \bar{Z}^H_{pb}(\bar{Z}^H_{bb} + \bar{Z}^I_{dd})^{-1}\bar{Z}^I_{du},$$
$$\bar{Z}^{HI}_{up} = \bar{Z}^I_{ud}(\bar{Z}^H_{bb} + \bar{Z}^I_{dd})^{-1}\bar{Z}^H_{bp},$$
$$\bar{Z}^{HI}_{uu} = \bar{Z}^I_{uu} + (-\bar{Z}^I_{ud})(\bar{Z}^H_{bb} + \bar{Z}^I_{dd})^{-1}\bar{Z}^I_{du}$$

Then, having the impedance matrices $\bar{Z}_{HI}$ and $\bar{Z}_J$, and reusing the segmentation method, the overall impedance matrix of the three segments is calculated with three subports p at the input and three subports q at the output as:

$$\bar{Z}_{HIJ} = \begin{matrix} \bar{Z}_{pp}^{HIJ} & \bar{Z}_{pq}^{HIJ} \\ \bar{Z}_{qp}^{HIJ} & \bar{Z}_{qq}^{HIJ} \end{matrix} \quad (8)$$

where,

$$\bar{Z}_{pp}^{HIJ} = \bar{Z}_{pp}^{HI} + \bar{Z}_{pu}^{HI}(\bar{Z}_{uu}^{HI} + \bar{Z}_{rr}^{J})^{-1}(-\bar{Z}_{up}^{HI}),$$
$$\bar{Z}_{pq}^{HIJ} = \bar{Z}_{pu}^{HI}(\bar{Z}_{uu}^{HI} + \bar{Z}_{rr}^{J})^{-1}\bar{Z}_{rq}^{J},$$
$$\bar{Z}_{qp}^{HIJ} = \bar{Z}_{qr}^{J}(\bar{Z}_{uu}^{HI} + \bar{Z}_{rr}^{J})^{-1}\bar{Z}_{up}^{HI},$$
$$\bar{Z}_{qq}^{HIJ} = \bar{Z}_{qq}^{J} + (-\bar{Z}_{qr}^{J})(\bar{Z}_{uu}^{HI} + \bar{Z}_{rr}^{J})^{-1}\bar{Z}_{rq}^{J}$$

By combining subports p at the input and subports q at the output, in the same way as explained in section 2.1., the matching network impedance matrix shown in Fig. 3b is calculated with one port at the input and one port at the output and is shown as follows:

$$\bar{Z}_{m1} = \begin{matrix} Z_{11}^{m1} & Z_{12}^{m1} \\ Z_{21}^{m1} & Z_{22}^{m1} \end{matrix} \quad (9)$$

In the same way, the impedance matching network between the other stages of the amplifier are designed, and their impedance matrices are calculated as follows:

$$\bar{Z}_{m2} = \begin{matrix} Z_{11}^{m2} & Z_{12}^{m2} \\ Z_{21}^{m2} & Z_{22}^{m2} \end{matrix} \quad (10)$$

$$\bar{Z}_{m3} = \begin{matrix} Z_{11}^{m3} & Z_{12}^{m3} \\ Z_{21}^{m3} & Z_{22}^{m3} \end{matrix} \quad (11)$$

2.3. Design of Amplifier Output Impedance Matching Network

Since the output impedance of the amplifier consists of the intrinsic parameters R_{ds} and C_{ds} in parallel, to match it to a 50-ohm load, an impedance matching network similar to that of input, mentioned in Section 2.1 is required.

In the same way that mentioned in sections 2.1, the output impedance matching network is designed, and its impedance matrix is calculated and shown as follows:

$$\bar{Z}_{o} = \begin{matrix} Z_{11}^{o} & Z_{12}^{o} \\ Z_{21}^{o} & Z_{22}^{o} \end{matrix} \quad (12)$$

3. FOUR-STAGE AMPLIFIER FREQUENCY RESPONSE

Fig. 5 shows a cascaded four-stage amplifier with Input/output and inter-stage impedance matching networks designed by microstrip lines. In this design of amplifier, a 130 nm CMOS technology has been used. The intrinsic parameters of this transistor for the model shown in Fig. 5 are extracted as $R_{gs} = 3.9\Omega$, $C_{gs} = 94.5fF, R_{ds} = 102\Omega \, and \, C_{ds} = 71.7fF$

The four-stage amplifier transfer function is calculated using the impedance matrix of Input/output impedance matching networks and inter-stage obtained in equations (5), (9), (10), (11), and (12) as follows:

$$H_t(j\omega) \quad v_o / i_i \quad H_i(j\omega) \quad H_{m1}(j\omega) \quad H_{m2}(j\omega) \quad H_{m3}(j\omega) \quad H_o(j\omega) \quad (13)$$

Where,

$$H_i(j\omega) = v_{gs1} / i_i = Z_{21}^{i}(1 / j\omega C_{gs}) / (Z_{22}^{i} + R_{gs} + 1 / j\omega C_{gs})$$
$$H_{m1}(j\omega) = v_{gs2} / v_{gs1} = -g_m(Z_{11}^{m1} + Z_{12}^{m1}A_I^{m1})A_V^{m1} / (1 + j\omega R_{gs}C_{gs})$$
$$H_{m2}(j\omega) = v_{gs3} / v_{gs2} = -g_m(Z_{11}^{m2} + Z_{12}^{m2}A_I^{m2})A_V^{m2} / (1 + j\omega R_{gs}C_{gs})$$
$$H_{m3}(j\omega) = v_{gs4} / v_{gs3} = -g_m(Z_{11}^{m3} + Z_{12}^{m3}A_I^{m3})A_V^{m3} / (1 + j\omega R_{gs}C_{gs})$$
$$H_o(j\omega) = v_o / v_{gs4} = \frac{-g_m(Z_{21}^{o} + Z_{22}^{o}A_I^{o}) / (Z_{11}^{o} + Z_{12}^{o}A_I^{o})}{1 / R_{ds} + j\omega C_{ds} + 1 / (Z_{11}^{o} + Z_{12}^{o}A_I^{o})}$$

in which,

$$A_I^{m1} = \frac{-Z_{21}^{m1}}{(R_{gs} + 1 / j\omega C_{gs}) + Z_{22}^{m1}},$$
$$A_V^{m1} = \frac{Z_{21}^{m1} + Z_{22}^{m1}A_I^{m1}}{Z_{11}^{m1} + Z_{12}^{m1}A_I^{m1}},$$
$$A_I^{m2} = \frac{-Z_{21}^{m2}}{(R_{gs} + 1 / j\omega C_{gs}) + Z_{22}^{m2}},$$
$$A_I^{m3} = \frac{-Z_{21}^{m3}}{(R_{gs} + 1 / j\omega C_{gs}) + Z_{22}^{m3}},$$

$$A_V^{m3} = \frac{Z_{21}^{m3} + Z_{22}^{m3} A_I^{m3}}{Z_{11}^{m3} + Z_{12}^{m3} A_I^{m3}} \quad and$$

$$A_I^o = \frac{-Z_{21}^o}{50 + Z_{22}^o}$$

Using the impedance matrices of the input and output matching networks, the input impedance and output of the amplifier are calculated as follows:

$$Z_{in} = Z_{11}^i - \frac{Z_{12}^i Z_{21}^i}{(Z_{22}^i + R_{gs} + 1 / C_{gs})} \tag{14}$$

$$Z_{out} \quad Z_{22}^o \quad Z_{21}^o \; Z_{12}^o / [Z_{11}^o + 1 / (1 / R_{ds} + j\omega C_{gs})] \tag{15}$$

Using equations (13), (14), and (15), the amplifier scattering parameters (S) are calculated as follows [35]:

$$S_{11} = (Z_{in} - 50) / (Z_{in} + 50) \tag{16}$$

$$S_{21} = \frac{100 H_t(j\omega)}{[(Z_{in} + 50)(Z_{out} + 50)]} \tag{17}$$

$$S_{22} = (Z_{out} - 50) / (Z_{out} + 50) \tag{18}$$

By optimizing the length and characteristic impedance of each rectangular segment of the matching networks shown in Fig. 5 using an algorithm in MATLAB, an amplifier was designed with $S_{11\min} = -25.3\,dB$, $S_{22\min} = -20.6dB$, and $S_{21\max} = 30.5dB$ in the frequency range of 57 to 64 GHz, as shown in Figs 6.

Table 1 compares parameters such as frequency bandwidth (BW), maximum gain($S_{21\max}$) and minimum reflectance coefficient at the input($S_{11\min}$) and output ($S_{22\min}$) of the four-stage source-common amplifier designed in this paper with other references.

4. COMPARISON

Due to the lack of manufacturing facilities in our laboratory to fabricate the designed amplifier at the millimeter-wave frequencies, we could not validate our results with those of measurement. However, to validate our proposed method, the scattering parameters for the designed four-stage amplifier obtained from PCA, have been compared with those obtained from the full-wave analysis (ADS), see Fig. 6.

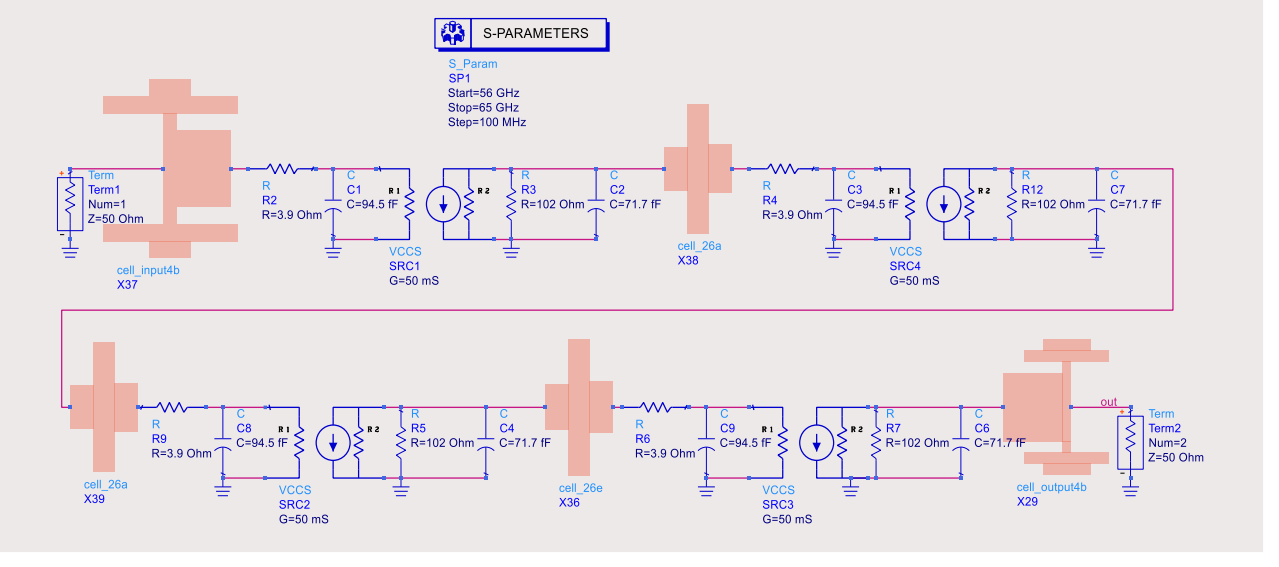

Fig. 5. Four-stage amplifier with impedance matching networks using microstrip lines at input, inter-stages, and output.

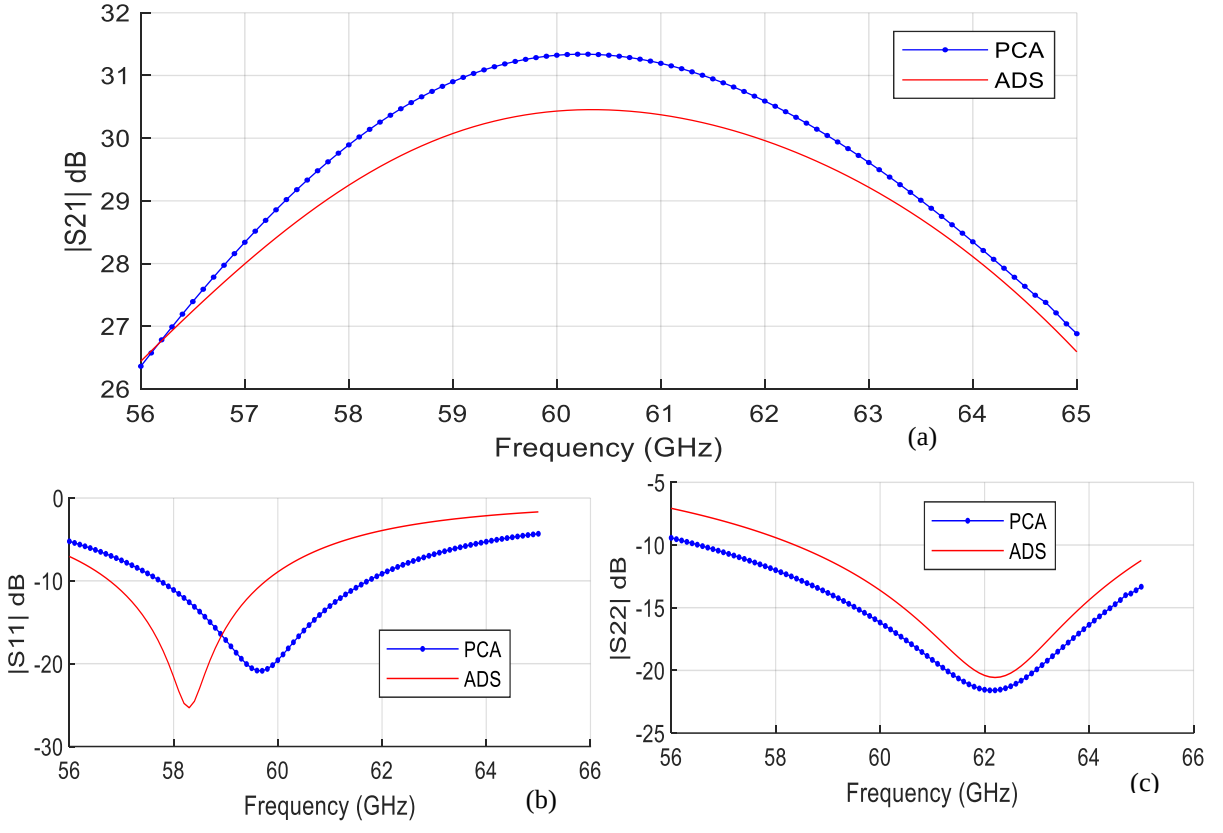

Fig. 6. Scattering parameters of four-stage amplifier shown in Fig. 5. (a) |S21| (b) |S11| (c) |S22|.

Table 1. Comparison of the performance of the designed amplifier with other references.

Technology Topology	BW (GHz)	$Gain$ (dB)	$S_{11\min}$ (dB)	$S_{22\min}$ (dB)	Reference
$130nm\ CMOS$ $4-Stage\ CS$	7 $59-66$	14.7	-15 $at\ f=65.7GHz$	-15 $at\ f=65.7GHz$	[22]
$65nm\ CMOS$ $3-Stage\ Cascode$	14.1 $\simeq 53.9-68$	20.6	-25 $at\ f\simeq 52GHz$	-12 $at\ f\simeq 54GHz$	[8]
$130nm\ CMOS$ $3-Stage\ Cascode$	4.5 $51.3-55.8$	20	-18 $at\ f\simeq 64GHz$	$\simeq -27.5$ $at\ f\simeq 54GHz$	[11]
$65nm\ CMOS$ $3-Stage\ CS$	$\simeq 8.5$ $\simeq 51.5-60$	18.3	$\simeq -16$ $at\ f\simeq 56GHz$	$\simeq -10$ $at\ f\simeq 54GHz$	[17]
$90\ nm\ CMOS$ $2-Stage\ CS$	12 $45-57$	7.2	$\simeq -17.5$ $at\ f\simeq 52GHz$	$\simeq -27.5$ $at\ f\simeq 60GHz$	[12]
$130nm\ SiGe\ BiCMOS$ $2-Stage\ Cascode$	>6 $62-68$	15.2	-15 $at\ f\simeq 66.2GHz$	$-$	[7]
$130\ nm\ CMOS$ $4-Stage\ CS$	7 $57-64$	30.5 $f_o=60.3GHz$	-25.3 $at\ f=58.3GHz$	-20.6 $at\ f=62.2GHz$	This work

5. CONCLUSION

In this paper, a cascaded common source four-stage millimeter wave amplifier was designed in a 130 nm CMOS technology. The designed amplifier has high gain and excellent IOIMNs and inter-stages. First, the Pi-shaped wideband IOIMNs and inter-stags were designed with microstrip line segments. Then, single stubs were converted to symmetrical double stubs in the IOIMNs, and an ultra-wideband inductor replaced each stub. Ultra-wideband inductors were also used in series in the inter-stage IMNs to achieve a higher gain in the wider frequency bandwidth. Finally, the impedance matrices of these matching networks were calculated using PCA, which is based on a planar waveguide model and SDSM. To minimize the dispersion effects, a substrate with low thickness and small permittivity was selected. By optimizing variables such as the length and characteristic impedance of each microstrip rectangular segment of the IMNs using an algorithm in MATLAB, an amplifier, was designed with $S_{11\min} = -25.3\ dB$, $S_{22\min} = -20.6\ dB$, and $S_{21\max} = 30.5\ dB$ in the frequency range of 57 to 64 GHz.

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