Body Current Optimization using Threshold-Voltage-Adjust-Implant Engineering in 45nm SOI MOSFET

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ABSTRACT:
In this paper, for the first time, Threshold-voltage-adjust-implant is engineered to optimize body current in 45 nm Silicon-on-Insulator (SOI) MOSFET. The peak value and peak position concentration of the Gaussian implant under the gate oxide in the silicon body are varied in order to optimize the body current in SOI technology. The variations affect the devices' threshold voltages. In order to make a fair comparison, the gate work function is changed to obtain the same threshold voltage within the entire simulated devices and operating regime. The body current is monitored while the it is swept from 0 V to 1.5 V. The maximum of the body current is observed at V_{DS}=1.5 V. The concentration of Threshold-voltage-adjust-implant peak value is changed from 1.7E17 cm^{-3} to 7E18 cm^{-3}. The peak position of the implant is varied from 0 nm right under the gate oxide to 20 nm below the gate oxide and silicon surface. It is observed that the body current is minimized at the peak value concentration of 7E17 cm^{-3} and peak position of 0 nm. This occurs by proper choice of the gate work function and gate material. The minimization of body current leads to the less requirement for the number of body contacts and smaller gate parasitic capacitance which, in turn, concludes higher operating frequency and larger f_T.

KEYWORDS: Threshold-Voltage-Adjust-Implant, Unity-Gain Cut-Off Frequency, Silicon-On-Insulator, MOSFET.

1. INTRODUCTION

SOI CMOS circuit design is the mainstream technology for RF solutions. The wide application of SOI in RF leads to enhanced circuit overall performance and figure of merits [1]. Addition of smart cut manufacturing methods to the processes, enables fabrication of wide structures of SOI CMOS from Partially Depleted (PD) SOI to Ultra-Thin Body (UTB) SOI and Ultra-Thin Body and BOX (UTBB) SOI [2]. PD SOI which is the core technology for RF applications better known as RF SOI is a promising solution for 5G and mmWave operating regime. The Kink which is inherent in the technology results in output nonlinearities [3].

Floating body effects (FBE) which are observed in PD SOI is inherited to RF SOI and the methods which was used in suppressing the FBE must be incorporated. The well-known solution is using body contacts to connect the floating body in RF SOI to ground and avoid the circuit mismatch undesired behavior [4,5]. The H-gate layout method is common to connect the body to an external source of voltage and making a path for the impact ionization generated holes in the channel to sweep out [6].

However, the H-gate introduces the undesired gate parasitic capacitances [7]. Therefore, there is a trade-off between the number of body contacts and FBE suppression. The former introduces parasitic gate and substrate capacitances and the latter is dominated by the intense of the hole generations in the high-field region of the device channel, i.e. body current.

The body current is dominated by the impact ionization process in the channel pinch–off region and any methods to lower the impact ionization current results in lower number of the required body contacts. The impact ionization current is a high nonlinear function of the Quasi Fermi level gradient [8]. Therefore, the impurity concentrations in the channel has a direct impact on the impact ionization current.

Threshold-voltage-adjust-implant is common to CMOS fabrication processes to adjust the threshold voltage of the devices to the desired value [9]. It is usually a low energy shallow implant beneath the silicon interface to the gate insulator. It affects the impurity concentration in the channel, hence, the Quasi Fermi level gradient in that area.

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In this paper, by Threshold-voltage-adjust-implant engineering, the impact ionization current is minimized and the gate work function is adjusted accordingly to adjust the device threshold voltage. The paper is organized as the following: In section 2, the Threshold-voltage-adjust-implant and the impact ionization model is described, the device simulation results are shown in section 3, followed by a section on conclusion in section 4.

2. THRESHOLD-VOLTAGE-ADJUST-IMPLANT DESCRIPTION AND IMPACT IONIZATION MODEL

During a normal CMOS fabrication process flow, a Threshold-voltage-adjust-implant is introduced to control the threshold voltage of the devices to the desired value [9]. Precise control of impurities leads to wide spread application of the process step. The implant is usually shallow and introduces a spike-like impurity concentration in the silicon near the surface. Fig. 1 shows a typical Gaussian profile for the concentration.

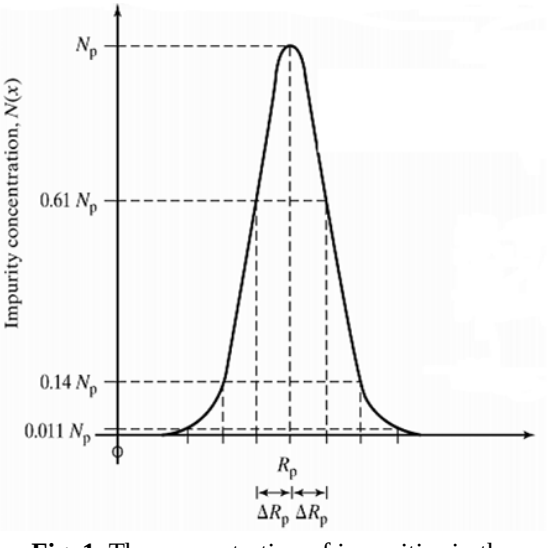

Fig. 1. The concentration of impurities in the Threshold-voltage-adjust-implant

As can be seen, the Gaussian profile is described by two main parameters: 1- the maximum or peak value N_P and 2- the maximum or peak position R_P. In the conventional CMOS fabrication, R_P is small and the peak position is kept close to the silicon surface. The peak value N_P is varied to adjust the threshold voltage. While this is a precise controlled method for threshold voltage adjustment, it affects the Quasi Fermi level gradient of carriers in the channel while the device is in strong inversion. Therefore, this study concentrates on the effect of the implant on impact ionization generated current.

The impact ionization is derived largely by the high electric field. The electron in the conduction band gains enough energy in the high field region near the drain in the device saturation regime that impacts an electron-hole pair in the valence band and causes the electron to jump to the conduction band and leaves behind a hole in the valence band. In the following the electron-hole generation rate in the high electric field is explained.

The electron-hole generation process is characterized by a high threshold electric field and acceleration path. Therefore, within the silicon lattice, a free space and large distance is required. If the distance is larger than the mean free path, the electrical breakdown occurs. The mean free path is demonstrated by α and is named as the impact ionization coefficient. By using α, the electron-hole generation rate is as follows [8]:

$$G^{||} = \alpha_n n v_n + \alpha_p p v_p \qquad (1)$$

where α_n and α_p describes electron and hole impact ionization coefficients, n and p shows electron and hole concentrations, v_n and v_p defines the electron and hole drift velocities, respectively. The impact ionization process is a random phenomenon, and it is characterized by experimental measurements and procedures. We chose the following experimental model [8]:

$$\alpha(F) = a \cdot \left(1 - c(T - T_0)\right) \cdot F^{\gamma} \cdot e^{-\left(\frac{b[1+d(T-T_0)]}{F}\right)^{\delta}} \qquad (2)$$

where T_0= 300 K, T defines the lattice temperature and F shows the driving force calculated from Quasi Fermi level gradient. a, b, c, d, γ, δ are constant parameters that are material dependent and differs their values for electrons and holes.

As can be seen from Eq. 1 and the subsequent Eq. 2, the impurity concentration in the channel strongly impacts the Quasi Fermi level gradient and the resultant electron-hole generation rate. Consequently, the electron-hole generation rate and the body current is influenced by the Threshold-voltage-adjust-implant impurities.

3. DEVICE SIMULATION RESULTS

A PD 45 nm NMOS device is designed such that the body current can be measured during the simulation. The structure of the transistor is the same as in [5,10]. The following simulation models in DESSIS is incorporated: Drift-diffusion transport equations; carrier saturation dependence to electric field, doping and temperature; Augur recombination; Okuto-Crowell impact ionization. The bulk contact is kept at 300 K.

Several peak values and peak positions are chosen. For each peak value and peak position, the following procedure is repeated to obtain the predefined threshold voltage. The threshold voltage is defined as the gate

voltage for which the electron concentration in the channel exceeds the background doping. The gate contact voltage is swept from 0 V to 1.2 V and the electron concentration in the channel is monitored. Once the threshold voltage is measured, the gate work function is adjusted to obtain the predefined threshold voltage.

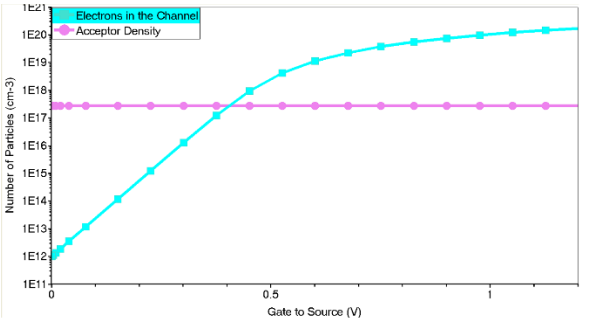

Fig. 2. Electron and Acceptor concentration in the channel with respect to the gate voltage. V_{DS}= 0 V.

As can be seen from Fig. 2, the electron concentration in the channel exponentially grows with the gate voltage and as the device enters the strong inversion, the electron concentration growth slows down. The threshold voltage as defined by the physics of the device is obtained. The above procedure is repeated until the threshold voltage is adjusted and the simulation converges to a unique gate work function.

The above procedure is repeated for all the peak values and peak positions considered and all the devices are adjusted to have the equal threshold voltage.

The next step is to sweep the drain voltage from 0 V to 1.5 V and measure the body current.

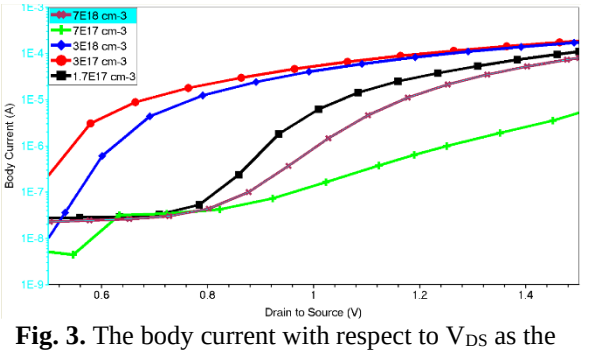

Fig. 3. The body current with respect to V_{DS} as the peak position is at the Silicon interface to the oxide. V_{GS} = 1.2 V.

Fig. 3 shows the body current VS. drain to source voltage at the peak value is varied. The peak position is at the silicon to oxide interface. As it can be seen, the body current grows exponentially with the drain voltage. The minimum of the body current at the highest drain voltage occurs at N_P=7E17 cm^{-3}. For other N_P values, the body current at the highest drain voltage is larger.

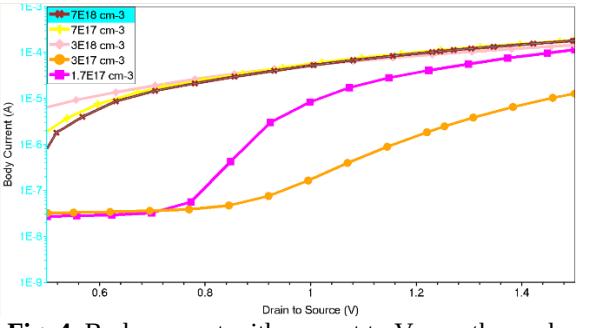

Fig. 4. Body current with respect to V_{DS} as the peak position is 10 nm below the silicon to oxide interface. V_{GS}=1.2 V

Fig. 4 shows the body current VS. V_{DS} where R_P=10 nm. As it can be seen, the body current at the highest V_{DS} is almost one order of magnitude smaller at N_P=3E17 cm^{-3} than the next smallest value N_P=1.7 E17 cm^{-3}. Therefore, for the peak position of 10 nm, the smallest number of body contacts occur at the N_P=3E17 cm^{-3}.

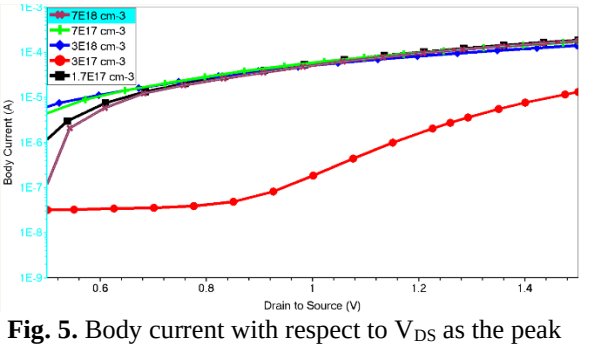

Fig. 5. Body current with respect to V_{DS} as the peak position is 15 nm below the silicon to oxide interface. V_{GS}=1.2 V.

Fig. 5 shows the body current VS. V_{DS} for R_P= 15 nm at V_{GS}=1.2 V. As it can be seen, the variations of Body current below V_{DS}= 0.5 V is negligible and it is not shown in the graphs. The body current grows exponentially as the drain voltage increases and the highest number of body current occurs at N_P=3E17 cm^{-3} and an order of magnitude less than N_P=3E18 cm^{-3}.

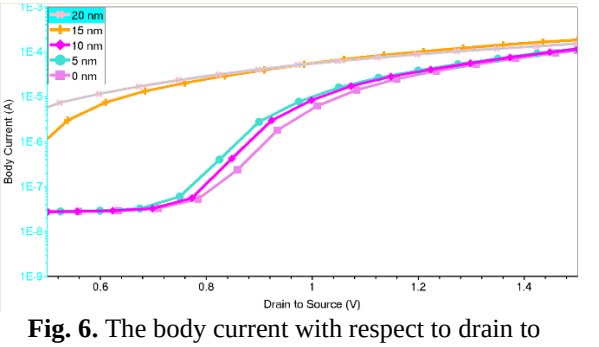

Fig. 6. The body current with respect to drain to source voltage as R_P varies. V_{GS}=1.2 V and N_P=1.7E17 cm^{-3}

Fig. 6 shows the drain current VS. drain voltage as R_P varies from 0 nm to 20 nm while N_P=1.7E17 cm^{-3}. The Body current blow V_{DS}=0.5 V is negligible and it is not shown. As it can be seen, the minimum of body current occurs at R_P=0 nm while V_{DS}=1.5 V. As the peak positions move further away from the silicon to oxide interface, the body currents get larger. The gate to source voltage is 1.2 V.

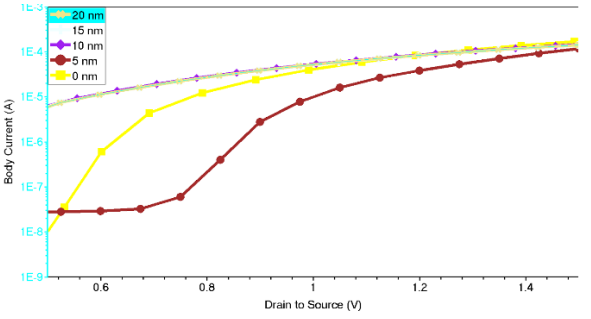

Fig. 7. The Body current with respect to drain to source voltage at V_{GS}= 1.2 V and N_P=3E18 cm^{-3} as R_P varies.

Fig. 7 shows the body current graph VS. drain to source voltage as R_P varies from 0 nm to 20 nm. As it can be seen, the minimum of body current at V_{DS}=1.5 V occurs at R_P=5 nm.

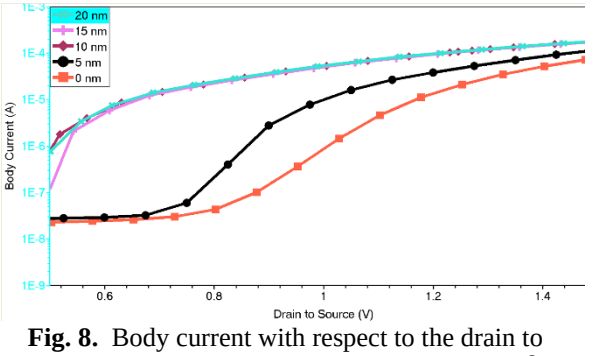

Fig. 8. Body current with respect to the drain to source voltage at V_{GS}=1.2 V and N_P=8E18 cm^{-3}.

Fig. 8 shows the body current VS. V_{DS} for N_P=8E18 cm^{-3}. As it can be seen, the body currents grow as the drain to source voltage increase and the minimum of body current at V_{DS}=1.5 V occurs at R_P=0 nm.

Therefore, from Figs. 3, 4, 5, 6, 7 and 8 deduce that both the values of R_P and N_P influence the minimum of body current and different values obtain when these values vary.

Table 1 summarizes the results obtained from the device simulations. As it can be seen, the minimum of body current is 3μA at the peak concentration of 7E17 cm^{-3} and peak position of 0 nm. This is the optimized value of body current. From Table 3 it also can be seen that by un-optimized choice of the Threshold-voltage-adjust-implant parameters, the minimum value of the body current can be 23 times higher than the optimized value and it occurs at N_P=7E18 cm^{-3} and R_P=0 nm. Thus, by Threshold-voltage-adjust-implant engineering and proper choice of the N_P and R_P, the body current is optimized and the resultant number of body contacts required to suppress floating body effects are minimized.

Table 1. Minimum body current obtained from device simulations at the maximum operating V_{DS}=1.5 V.

$N_P(cm^{-3})$	R_P(nm)	Body Current(μA)
7E17	0	3
3E17	10	4
3E17	15	8
1.7E17	0	60
3E18	5	30
7E18	0	70

This is done through the proper choice of the gate material to adjust the gate work function, hence, device threshold voltage. Therefore, the inherent gate parasitic capacitance due to the layout extension of the gate to make the body contacted is smaller in the optimized device. Consequently, the larger unity-gain cut-off frequency is obtained for RF SOI applications to meet the emerging requirement of the new technologies.

4. CONCLUSION

Threshold-voltage-adjust-implant engineering is incorporated to optimize the body current in RF SOI MOSFETs. Using the proper gate material and adjusting the gate work function, equal threshold voltage devices are obtained. Device simulations for various parameters of Gaussian profiles of Threshold-voltage-adjust-implant are performed. The impurity concentration in the channel of the devices influence the Quasi Fermi level gradient and exponentially impacts the hole generation during impact ionization. Thus, body current is minimized by Threshold-voltage-adjust-implant engineering. The optimization results in smaller number of body contacts and reduced number of gate layout extension. Therefore, the reduction of parasitic gate capacitance increases the unity-gain cut-off frequency of RF SOI MOSFET, make it a profound device to meet the requirement of the emerging technologies.

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