

A Novel High Voltage Gain Buck-Boost Converter with Dual Mode Boost

Mustafa Okati, Mahdiyeh Eslami*, Mahdi Jafari Shahbazzadeh

Department of Electrical Engineering, Kerman Branch, Islamic Azad University, Kerman, Iran.

Email: m.okati@iauzabol.ac.ir

Email: m.eslami@iauk.ac.ir (Corresponding author)

Email: mjafari@iauk.ac.ir

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ABSTRACT:

This paper focuses on introducing a transformerless DC/DC converter with low total switching device power in dual working modes including step-up and step-up/down modes. The proposed converter is analysed in terms of the continuous conduction mode, steady state, and efficiency with the replacement of parasitic resistance effects. The proposed converter in the step-up mode has a high voltage gain ratio and a continuous input current. Then, the other working mode of the proposed converter with relevant DC/DC converters is compared. By this comparison, the proposed converter has a high voltage gain ratio. Also, the converter characteristics such as voltage stress on power switches and charge pump capacitors are in a good condition in this mode. Finally, the experimental results from a laboratory made prototype and the obtained waveforms from the simulation in PLECS are presented for validation such as higher voltage gain ratio, lower total switching device power and better efficiency.

KEYWORDS: Continuous Input Current, Step-Up/Down Mode, Parasitic Parameters, Dual Mode, Switching Device Power (SDP).

1. INTRODUCTION

In recent years, renewable energy resources such as fuel cells and photovoltaic (PV) have attracted a huge deal of attention, for several domestic and industrial applications to present cost-effective electrical energy. By each of these sources, electricity is generated with various features of current and voltage, seriously restricting their applicability. For example, to integrate them with the grid, their voltage should be increased while controlling the energy flow to the grid. However, to use them as the energy source for some home tools, their voltage should be decreased to prevent any overvoltage-caused damage [1-6]. Fossil fuel is an easily accessible and common electrical energy generation resource, as the primary reason for the issues mentioned earlier. Therefore, the gathering energy from renewable resources is an auspicious solution to fix such issues because these sources are environmentally friendly, and more cost-competitive as a result of developments in power electronics. Furthermore, they meet the future demands in the electrical power [7], [8]. Hence, power loss is reduced by installation of a DC-DC converter near photovoltaic panels as a solar power optimizer (SPO) thus increasing the system efficiency [9]. Previous literature presents many buck-boost DC-DC converters, most of which are

based on conventional DC/DC converters such as buck, boost, buck-boost, CUK, SEPIC, and ZETA converters [10], [11]. Some topologies apply switched capacitor multipliers to enhance voltage gains with no increased duty cycle. However, due to switching parallel capacitors, these topologies produce high current stress and charging/discharging losses [12], [13]. The approach can be extended to any number of Voltage Multiplier Cells (VMC) although the static gain can be increased further. The voltage stress in active switches is also reduced in [14, 15]. For alternate energy applications, [16] used SEPIC with many elements to augment the voltage gain while diminishing the voltage stress on the main switch. In this system, SEPIC is coupled with two voltage multipliers and an inductor. It is a good alternative for sustainable and renewable energy applications due to its uninterrupted input current. In another study [17], the converter employs a switched-capacitor/inductor within the conventional buck-boost converter, which offers quadratic voltage gain while suffering from a negative output voltage and discontinuous input current. In the new quadratic buck-boost converter proposed in [18], the voltage stress on elements has reduced while with a low voltage gain ratio and discontinuous input current. In addition, a novel step-up/down DC converter was provided by

combining the KY model [19], which can realize the discontinuous current port of input, and two switches are employed in this converter. It is noteworthy that the voltage gain ratio of this converter is low. An extended multi-cell buck-boost converter in terms of the conventional SEPIC converter is also provided in [20], which needs high numbers of components while having limited voltage gain. A new buck-boost converter has been presented by [21] with a similar voltage gain provided in [20] while with a discontinuous input current and negative output. One of the well-known conventional DC-DC converters is the ZETA converter, which has recently been proposed in [22]. This converter employs an energy storing cell of switched capacitors/inductors within the conventional ZETA converter. The voltage gain of this converter is just twice that of the conventional ZETA converter. However, it requires a greater number of components compared to its origin. A new quadratic converter was further introduced in [23]. Only one low voltage stress switch has been used in this converter. In addition, there are inductive filters at the input and output of this converter solving the power discontinuous problem in its input and output. Conversely, there exist many components, and the input/output polarities are reversed. Additionally, some studies proposed quadratic buck-boost converters with two power switches, requiring two gate drivers, resulting in increased complexity of the control system [24], [25]. The converter demands two floating switches. In some studies [26, 27], quadratic buck-boost converters were considered with a wide voltage ratio and continuous input current. Some studies [28] have designed negative-output boost converters with voltage gain, but this gain is not high enough. Moreover, a novel transformer-less inverter has been prototyped with dual modes in only one phase [29]. With its simple structure, this single-phase inverter is capable of providing a variety of voltage gain ratios to overcome the shortcomings of modern dual-mode inverters. The different types of non-isolated DC-DC converters are depicted in Fig.1. To overcome the shortages, this paper presented a non-isolated buck-boost and boost converter, which has a wide range of conversion ratios and a continuous input current in the step-up mode, making it suitable for renewable energy applications. The structure of this paper is as follows.

First, the proposed converter is introduced, followed by performing steady-state evaluation and theoretical analyses in Section 2. The advantages of the proposed converter are compared with other converters in Section 3. Section 4 provides the results of the PLECS simulation. Further, the experimental results of the laboratory-made prototype of the proposed

converter are discussed in Section 5. Finally, the main findings are presented in Section 6.

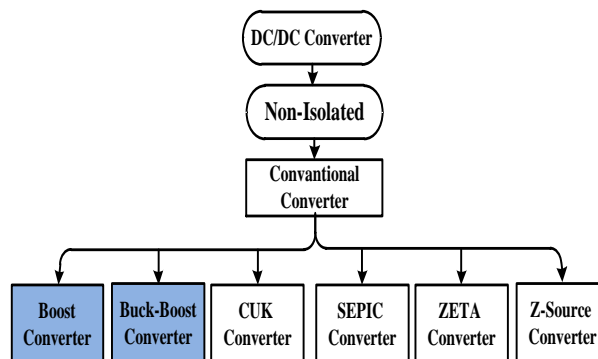


Fig. 1. Types of DC-DC converters [11].

2. PROPOSED CONVERTER

Among the most vital properties of DC-DC converters used in photovoltaic (PV) inverters are their continuous input current, cost-effectiveness, low counterpart, high efficiency, and low input ripple current. According to Fig. 2, the presented converter is claimed to be employed greatly in PV applications.

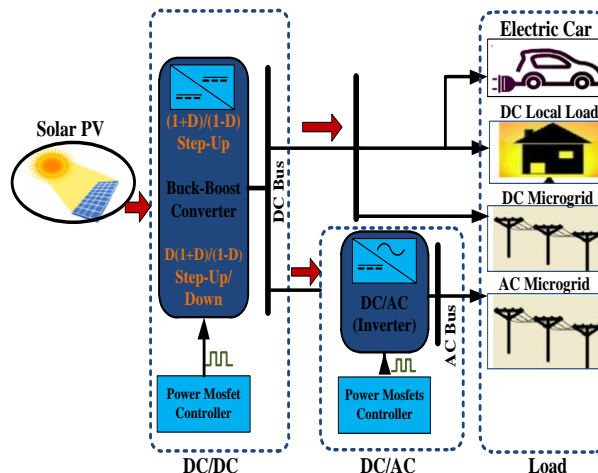


Fig. 2. DC/DC converter applications.

Steady state calculations for variables, such as voltage, current, efficiency, and voltage ripples will be explained here. Moreover, the proposed converter structure is presented in Fig.3 integrating two inductors (L_1, L_2), three capacitors (C_1, C_2, C_o), two switches (S_1, S_2), three diodes (D_1, D_2, D_3), and resistive load to obtain buck-boost and boost converters. It is worth noting that prior to assessing the proposed converter's performance; the two points are made to obtain further simplicity. First, components are considered to be ideal and second all capacitors are huge sufficient that voltage over each capacitor can be considered nearly constant. Moreover, the calculations for the proposed

converter are conducted in CCM and steady-state condition. For the converter in the CCM, three main operating states are determined (Fig.4).

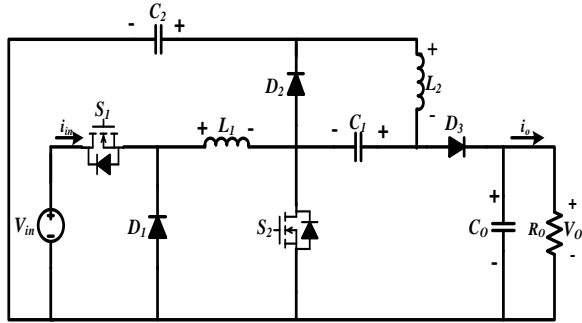
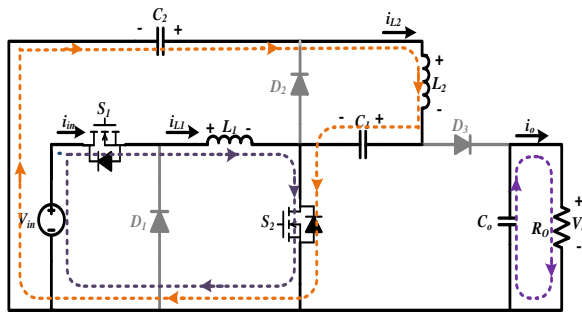
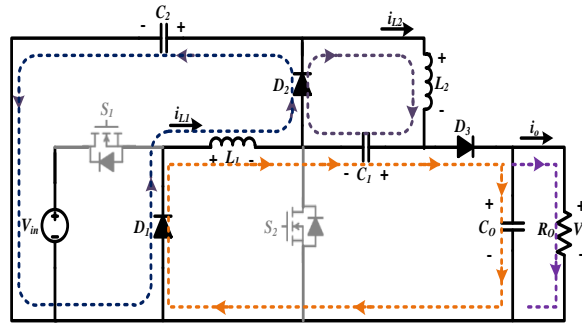


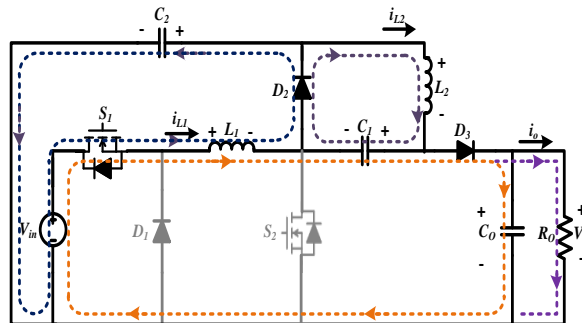
Fig. 3. Structure of the proposed converter.



(a)



(b)



(c)

Fig. 4. Operating modes of the proposed converter.

Structure I (step-up/down Mode):

State 1 [$0 \leq t \leq DT_s$]: In this mode, the power switches are ON, while the three diodes D_1 , D_2 and D_3

are reversed-biased. Here, the inductor L_1 is charged by the input dc power V_{in} . Meanwhile, discharging the energy of the capacitors C_1 , C_2 , is performed to inductor L_2 , though the output load R_o is fed by C_o . It is indicated that the linear increase in the inductor voltage is associated with releasing the capacitor energy into the circuit. The relevant circuit is presented in Fig.4 (a). For this mode, corresponding equations are achieved via the KVL, as follows:

$$\begin{cases} V_{L_1} = V_{in} \\ V_{L_2} = V_{C_2} - V_{C_1} \end{cases} \quad (1)$$

State 2 [$DT_s \leq t \leq T_s$]: In this mode, the power switches are OFF, however, the three diodes D_1 , D_2 and D_3 are conducted. Capacitors C_1 , C_2 in this time interval, are charged by releasing the stored energy in inductors L_2 and L_1 through D_2 and D_1 , respectively. Moreover, the energy stored in the inductor L_1 charges C_1 , C_o and resistive output load R_o via diode D_3 , for which the relevant circuit is presented in Fig.4 (b). For this mode, the corresponding voltages are achieved through the KVL as follows:

$$\begin{cases} V_{L_1} = V_{C_1} - V_o = -V_{C_2} \\ V_{L_2} = -V_{C_1} \end{cases} \quad (2)$$

Structure II (step-up Mode):

State 1 [$0 \leq t \leq DT_s$]: This step is similar to state 1 in structure I of the proposed converter.

State 2 [$DT_s \leq t \leq T_s$]: Here, the power switch S_1 is turned on and S_2 is turned off. This mode has different case of diodes, with diode D_1 reversed-biased and diodes D_2 and D_3 as conducting. Capacitors C_1 , C_2 are charged in this time interval, through releasing the stored energy in inductors L_2 and L_1 via D_2 , respectively. Moreover, the energy stored in the inductor L_1 charges C_1 , C_o and resistive output load R_o through diode D_3 . The relevant circuit is presented in Fig.4(c). For this mode, the corresponding voltage equations are obtained as follows through the KVL:

$$\begin{cases} V_{L_1} = V_{in} - V_{C_1} - V_o \\ V_{L_2} = V_{C_2} - V_o = -V_{C_1} \end{cases} \quad (3)$$

The charge and discharge periods of structures are clearly shown with waveform of samples in the time domain (Fig. 5).

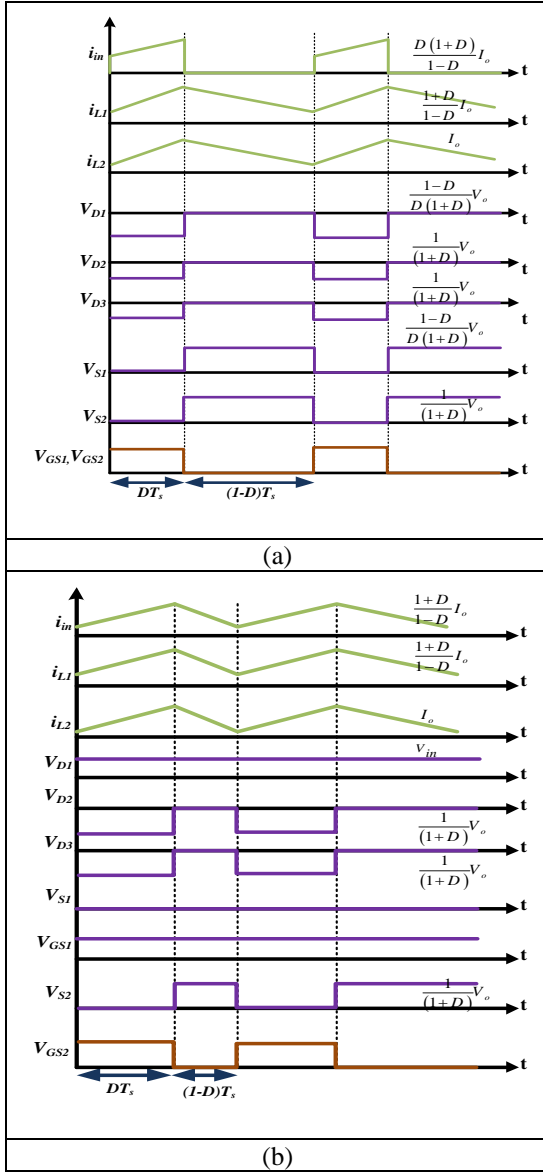


Fig. 5. Switching sequence and sample time domain waveforms. (a) Structure I. (b) Structure II

2.1. Calculations of Voltage Gain and Capacitor Voltage in Step-up/down Mode

Considering structure I of the step-up/down mode, the gain ratios and voltage values of the converter presented in this work can be achieved (Figs.4 (a) and (b)). To calculate the average voltage value of all capacitors, the volt-second balance principle of inductors L_1 and L_2 within the charge-discharge periods is considered. Hence, D is assumed as the duty cycle, and the average voltages of capacitors C_1 and C_2 are represented as V_{C1} and V_{C2} :

$$\begin{cases} V_{C1,step-up/down} = \frac{D^2}{1-D} V_{in} = \frac{D}{1+D} V_o \\ V_{C2,step-up/down} = \frac{D}{1-D} V_{in} = \frac{1}{1+D} V_o \end{cases} \quad (4)$$

The transfer function of the dc voltage (M_{CCM}) of the converter proposed is seen:

$$M_{CCM} = \left(\frac{V_o}{V_{in}} \right)_{Step-up/down} = \frac{D(1+D)}{1-D} \quad (5)$$

In structure I, the proposed converter works in step-down mode for $D < 0.414$, while it works in step-up mode for $D > 0.414$.

2.2. Calculations of the Inductor Currents and Current Gain in Step-up/down Mode

The assumption of the lack of power loss in the system, i.e. the total transfer of input power to output power, is derived as follows:

$$\begin{aligned} P_{in} &= P_o \\ V_{in} I_{in} &= V_o I_o \end{aligned} \quad (6)$$

Since I_{in} shows the input current, the transfer function for the converter dc current will be as follows:

$$\left(\frac{I_{in}}{I_o} \right)_{Step-up/down} = \frac{D(1+D)}{1-D} \quad (7)$$

The ampere-second balance principle of capacitors C_1 , C_2 and C_o is used to calculate the mean voltage value of all inductor currents. Therefore, I_{L1} and I_{L2} currents will be equal to:

$$\begin{cases} I_{L1} = \frac{1+D}{1-D} |I_o| \\ I_{L2} = |I_o| \end{cases} \quad (8)$$

2.3. Electrical Stress on Semiconductor Components in Step-up/down Mode

For power switches S_1 and S_2 , the voltage and average current stresses are calculated in off and on-state of operation as follows:

$$\begin{cases} V_{S1} = V_{in} = \frac{(1-D)}{D(1+D)} V_o \\ V_{S2} = \frac{D}{1-D} V_{in} = \frac{1}{1+D} V_o \end{cases} \quad (9)$$

$$\begin{cases} I_{S1-avg} = DI_{L1} = \frac{D(1+D)}{1-D} |I_o| \\ I_{S2-avg} = D(I_{L1} + I_{L2}) = \frac{2D}{1-D} |I_o| \end{cases} \quad (10)$$

Furthermore, the voltage and average current stress of each diode are calculated as follows:

$$\begin{cases} V_{D1} = -V_{in} \\ V_{D2} = -\frac{D}{1-D} V_{in} \\ V_{D3} = -\frac{D}{1-D} V_{in} \end{cases} \quad (11)$$

$$\begin{cases} I_{D1-avg} = (1+D) |I_o| \\ I_{D2-avg} = |I_o| \\ I_{D3-avg} = |I_o| \end{cases} \quad (12)$$

2.4. Calculations of step-up mode (structure II)

According to Figs.4 (a) and (c), the currents and voltage of step-up mode of the proposed converter can be determined in structure II. Utilizing the following equations, inductors current, capacitors voltage, voltage and current of semiconductor diodes and switches, as well as voltage gain ratio can be determined for the proposed converter as follows:

$$\begin{cases} V_{C1} = \frac{D}{1-D} V_{in} = \frac{D}{1+D} V_o \\ V_{C2} = \frac{1}{1-D} V_{in} = \frac{1}{1+D} V_o \end{cases} \quad (13)$$

$$\begin{cases} I_{L1} = \frac{1+D}{1-D} |I_o| \\ I_{L2} = |I_o| \end{cases} \quad (14)$$

$$\begin{cases} V_{S1} = 0 \\ V_{S2} = \frac{1}{1-D} V_{in} = \frac{1}{1+D} V_o \end{cases} \quad (15)$$

$$\begin{cases} V_{D1} = V_{in} \\ V_{D2} = \frac{1}{1-D} V_{in} \\ V_{D3} = \frac{1}{1-D} V_{in} \end{cases} \quad (16)$$

$$\begin{cases} I_{S1-avg} = I_{L1} = \frac{1+D}{1-D} |I_o| \\ I_{S2-avg} = D(I_{L1} + I_{L2}) = \frac{2D}{1-D} |I_o| \end{cases} \quad (17)$$

$$\begin{cases} I_{D1-avg} = 0 \\ I_{D2-avg} = |I_o| \\ I_{D3-avg} = |I_o| \end{cases} \quad (18)$$

$$M_{CCM} = \left(\frac{V_o}{V_{in}} \right)_{Step-up} = \frac{1+D}{1-D} \quad (19)$$

2.5. Efficiency Calculation

In this part, the amount of losses of each circuit component is considered according to the circuit shown in Fig. 6.

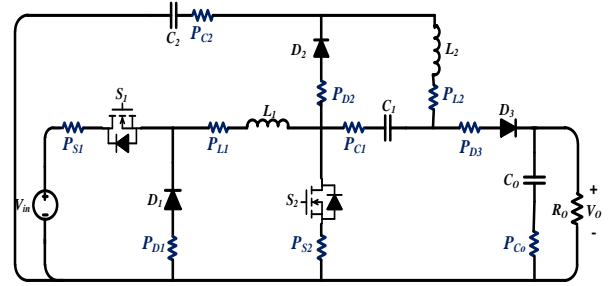


Fig. 6. The equivalent circuit considering the parasitic elements.

First, the *RMS* value of the switches and diodes current are obtained using equations (17)-(18):

$$I_{S1-rms} = \sqrt{\frac{\int_0^{DT_s} i_{L1}^2 dt}{T_s}} \approx \frac{\sqrt{D}(1+D)}{(1-D)} |I_o| \quad (20)$$

$$I_{S2-rms} = \sqrt{\frac{\int_0^{DT_s} (i_{L1} + i_{L2})^2 dt}{T_s}} \approx \frac{2\sqrt{D}}{(1-D)} |I_o|$$

$$I_{D1(ms)} \approx \frac{(1+D)I_o}{\sqrt{(1-D)}} \quad (21)$$

$$I_{D2,3(ms)} \approx \frac{I_o}{\sqrt{(1-D)}}$$

Also, the *RMS* value of inductors and capacitors current of the circuit are calculated as follows:

$$I_{L1-rms} = \sqrt{\frac{\int_0^{T_s} i_{L1}^2 dt}{T_s}} \approx \frac{(1+D)}{(1-D)} |I_o| \quad (22)$$

$$I_{L2-rms} = \sqrt{\frac{\int_0^{T_s} i_{L2}^2 dt}{T_s}} \approx |I_o|$$

$$I_{C1(ms)} = \sqrt{\frac{\int_0^{DT_s} i_{C1}^2 dt + \int_{DT_s}^{T_s} i_{C1}^2 dt}{T_s}} \approx \sqrt{\frac{D}{(1-D)}} I_o \quad (23)$$

$$I_{C_2(ms)} = \sqrt{\frac{\int_0^{DT_s} i_{C_2}^2 dt + \int_{DT_s}^{T_s} i_{C_2}^2 dt}{T_s}} \approx \sqrt{\frac{D}{(1-D)}} I_o$$

$$I_{C_o(ms)} = \sqrt{\frac{\int_0^{DT_s} i_{C_o}^2 dt + \int_{DT_s}^{T_s} i_{C_o}^2 dt}{T_s}} \approx \frac{D^{1/2}}{(1-D)^{1/2}} I_o$$

The total power losses of the switches ($P_{S1,2}$), are defined as sum of the conducting power dissipations (P_{R-DS}) and switching losses (P_{S-L}). With the R_{DS} value as conduction resistance of the power switch, as follows:

$$P_{S_{1,2}-Total} = P_{R-DS} + P_{S-L} \quad (24)$$

Where,

$$\left\{ \begin{array}{l} P_{R-DS_1} = R_{DS_1} I_{s_1(ms)}^2 = R_{DS_1} \left(\frac{\sqrt{D}(1+D)}{(1-D)} \right)^2 I_o^2 \\ P_{R-DS_2} = R_{DS_2} I_{s_2(ms)}^2 = R_{DS_2} \left(\frac{2\sqrt{D}}{(1-D)} \right)^2 I_o^2 \\ P_{S-L_1} = f_s C_{s_1} V_{s_1}^2 = f_s C_{s_1} V_{in}^2 \\ P_{S-L_2} = f_s C_{s_2} V_{s_2}^2 = f_s C_{s_2} \frac{D^2}{(1-D)^2} V_{in}^2 \end{array} \right. \quad (25)$$

Moreover, the overall losses of the diodes may be computed as the sum of the forward bias losses (P_{DF}) and the reverse bias losses (P_{RF}) by considering R_{DF} being the forward conduction resistance of the diode and V_{DF} as its forward bias voltage as follows:

$$P_{D-Total} = P_{DF} + P_{RF} = \sum_{i=1}^{i=3} (R_{DF} I_{Di-ms}^2) + \sum_{i=1}^{i=3} (V_{DFi} I_{Di}) \quad (26)$$

Considering R_L and R_C , equivalent series resistance (ESR) values of inductors and capacitors and power losses of each can be calculated as follows:

$$P_{L-Total} = \sum_{i=1}^{i=2} (P_{Li}) = \sum_{i=1}^{i=2} (R_{Li} I_{Li-ms}^2) \quad (27)$$

$$P_{C-Total} = \sum_{i=1}^{i=3} (P_{Ci}) = \sum_{i=1}^{i=3} (R_{Ci} I_{Ci-ms}^2) \quad (28)$$

The total losses of the circuit components may be summed up as shown here:

$$P_{loss-Total} = P_s + P_D + P_L + P_C \quad (29)$$

Finally, the equation for efficiency of the proposed converter can be calculated according to the following equations:

$$\eta_{Step-up/down} = \frac{P_o}{P_{loss} + P_o} = \frac{V_o I_o}{P_s + P_D + P_L + P_C + V_o I_o}$$

$$\eta_{Step-up} = \frac{V_o I_o}{P_{S1(on)} + P_{S2} + P_{D1(off)} + P_{D2,3} + P_L + P_C + V_o I_o} \quad (30)$$

2.6. Determination of the Amount of Ripple

The amount of ripple inductors current of the proposed converter can be obtained from Fig. 4 (a):

$$\Delta i_{L_{1,2}} = \frac{DV_{L_{1,2}}}{L_{1,2} f_s} \quad (31)$$

The value of each inductor can be calculated with the switching frequency (f_s) and current ripples' values. The process of calculating capacitors' voltage ripples is similar to the process of inductors' current ripple calculation as follows:

$$\left\{ \begin{array}{l} \Delta V_{C_{1,2}} = \frac{Di_{C_{1,2}}}{C_{1,2} f_s} \\ \Delta V_{C_o} = \frac{Di_{C_o}}{C_o f_s} \end{array} \right. \quad (32)$$

2.7. Selection Inductance and Capacitance

The current ripples of inductors are used for the purpose of their inductor value design in the proposed converter. The peak-to-peak current is shown in Fig. 4 (a) and assuming the current ripples inductors of (31), the required rate of ripple inductors current and inductances are:

$$\Delta i_{L_{1,2}} \leq \alpha \% I_{L_{1,2}} \quad \alpha \leq 30\% \quad (33)$$

$$L_{1,2} = \frac{DV_{L_{1,2}}}{\alpha \% \Delta i_{L_{1,2}} f_s} \quad (34)$$

$$\begin{cases} L_1 = \frac{D(1-D)^2}{\alpha\%(1+D)^2} \times \frac{R_o}{f_s} \\ L_2 = \frac{D(1-D)}{\alpha\%(1+D)} \times \frac{R_o}{f_s} \end{cases} \quad (35)$$

Where, R_o represents the value of output resistive load. In addition, voltage ripple of capacitors is employed for the purpose of their selection. According to (32), the voltage ripples of conventional and peak-to-peak capacitors and capacitances are calculated as follows:

$$\begin{cases} \Delta v_{C_{1,2}} \leq \beta\% V_{C_{1,2}} & \beta \leq 5\% \\ \Delta v_{C_o} \leq \delta\% V_o & \delta \leq 0.2\% \end{cases} \quad (36)$$

$$\begin{cases} C_1 = |(1+D)| \times \frac{1}{\beta\% R_o f_s} \\ C_2 = |D(1+D)| \times \frac{1}{\beta\% R_o f_s} \\ C_o = \frac{D I_o}{\delta\% \Delta V_o f_s} \end{cases} \quad (37)$$

3. ADVANTAGES OF THE PROPOSED CONVERTER IN DUAL MODE

The features of structures I and II of the proposed converter in step-up and step-up/down modes are provided in Fig.7 (block diagram) and Table 1. The voltage gain ratio and number of semiconductor elements of structure II are higher and fewer than compare to [29], respectively (Table 1). As seen in Table 1, under continuous input current condition, better voltage gain ratio and SDP of proposed converter are obtained compared to converter in [29], making it more appropriate for PV application (appendix). Consequently, to have the lowest overall voltage stress in the converter and at the same time to increase the voltage gain, the structure I during the step-down mode and the structure II during the step-up mode are chosen. The number of components and properties of the proposed converter are compared with other boost and buck-boost converters, which are presented in Tables 2 and 3. The input current type is the primary factor distinguishing the proposed converter and converter presented in [29],[25],[27], from other topologies. Unlike other topologies, these converters draw continuous current from the input port. Moreover, the supremacy of the proposed converter can be categorized as follows:

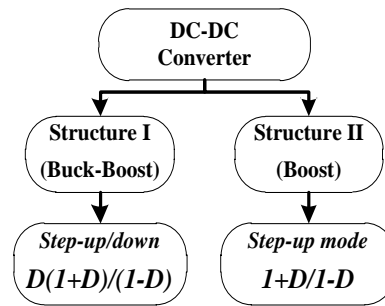


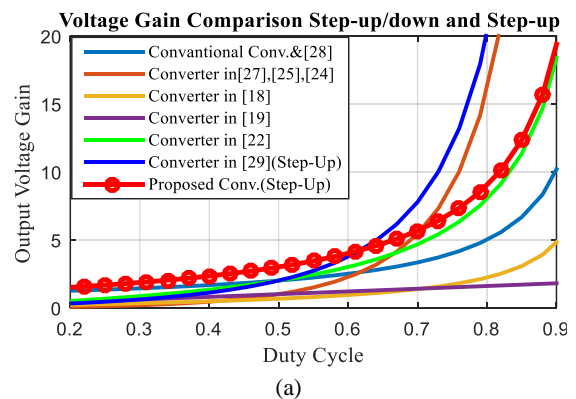
Fig. 7. Proposed converter block diagram.

Table 1. Comparison of structures (I, II).

Parameter	PROPOSED CONVERTER		CONVERTER IN [29]	
	Structure I	Structure II	Structure I	Structure II
Diode	3	2	4	3
Switch	2	1	2	1
MCCM	$\frac{D(1+D)}{1-D}$	$\frac{1+D}{1-D}$	$\left(\frac{D}{1-D}\right)^2$	$\frac{D}{(1-D)^2}$
Continuous Input	NO	YES	NO	YES
Common Ground	YES		NO	

3.1. High-voltage Gain Ratio in Step-up and Step-up/down Mode

A higher voltage gain ratio is represented by the intended converter for $D < 0.62$ compared to the similar converters in [18], [19], [22], [24], [25], [27] and [29]. Figs.8 (a) and (b) compare the ratios of voltage gain in accordance with the information presented in Tables 2 and 3, providing data on the proposed converter and other competitor converters. The horizontal axis in this Figure represents the duty cycle, which has been adjusted between 0.2 to 0.9. Also, the vertical axis shows the output voltage ranging from 0 to 20 volts. It can be seen that lower duty cycle allows high values of the output voltage with lower power loss.



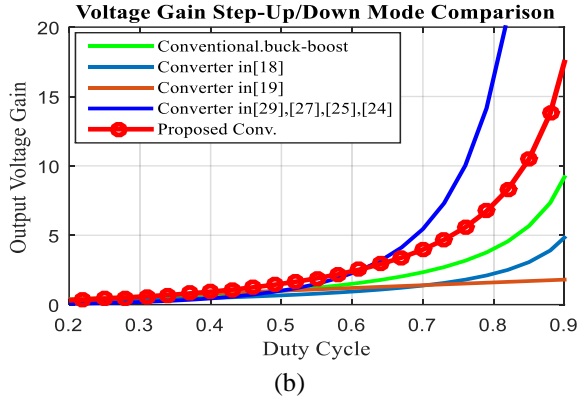


Fig. 8. Comparison of the voltage gain ratios and duty cycles of the proposed converter with other converters. (a) Step-up/down and step-up mode. (b) Step-up/down mode.

3.2. Values of Voltage Stress Among Power Switches

Figs. 9 (a) and (b) compare the voltage stress of power switches of the proposed converter with other competitor converters in step-up/down mode and step-up mode as presented in Table 2 and 3. According to the step-up/down mode and step-up mode (Figs.9 (a) and (b)), the lower power switches' voltage stress is found in the presented converter than the competitor converters.

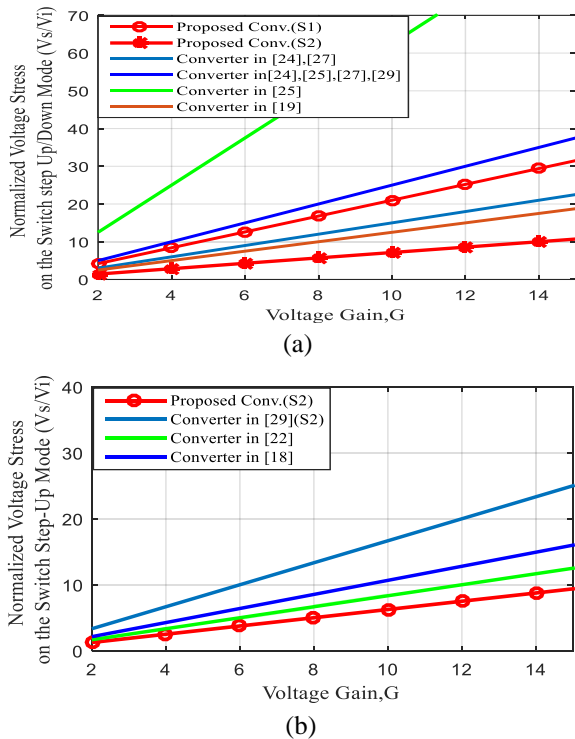


Fig. 9. Voltage stress imposed on the power switches versus output voltage gain. (a) Step-down mode with two switches (S_1 , S_2). (b) Step-up mode with one switch (S_1).

3.3. Total SDP

According to [30, 31], total SDP is a good index for the assessment of different properties of switching devices, such as potential costs, losses and cooling system requirements. The point to be made here is that current stress and voltage of a converter's switches and diodes must be taken into account in the assessment of its power loss and final cost of implementation. Therefore, these stresses must be evaluated. As an illustrative parameter, one can use the switching device power, i.e. SDP , as a measure for the power loss and the cost of the converter as already mentioned in [31]. The total average switching device power (SDP_{avg}) is calculated as,

$$SDP_{avg} = \sum_{i=1}^n V_{S_i} I_{S_{avg_i}} \quad (38)$$

Where, V_{S_i} and $I_{S_{avg_i}}$ are the peak voltage and average current of a switching period of i^{th} semiconductor employed in a power converter. The total average $SDPs$ of various converters are plotted in Fig.10. As can be seen in this Figure, the proposed converter offers lower SDP than other competitors, which directly translate to the lower power loss and the cost of semiconductors. For proposed converter can be calculated the total average SDP as,

$$SDP_{avg}(step-up) = \left(\frac{2}{1-D^2}\right)P_o \quad (39)$$

$$SDP_{avg}(step-up/down) = \left(\frac{-D^2 + 2D + 1}{D - D^3}\right)P_o$$

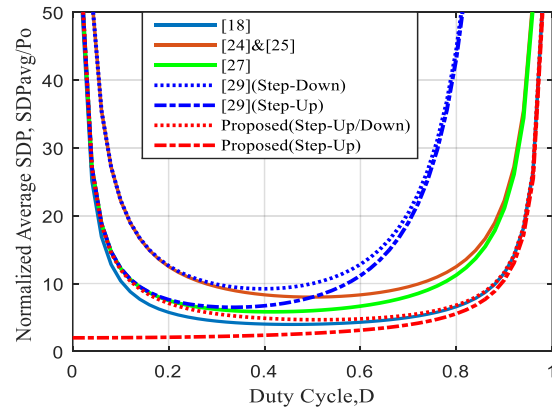


Fig. 10. Comparison of normalized total average switching device power (SDP_{avg}).

Table 2. A comparison of the proposed converter with similar converter in step-up/down mode.

Topology	Proposed Converter	IN[29]	IN[27]	IN[25]	IN [24]	IN [22]	IN[19]	IN[18]	Conventional buck-boost
Switches	2	2	2	2	2	1	2	1	1
Diodes	3	4	2	2	2	2	1	3	1
Capacitors	3	2	2	4	2	4	3	2	1
Inductors	2	2	2	3	2	3	2	2	1
Number of Elements	10	10	8	10	8	10	8	8	4
Voltage Gain	$\frac{D(1+D)}{1-D}$	$\left(\frac{D}{1-D}\right)^2$	$\left(\frac{D}{1-D}\right)^2$	$\left(\frac{D}{1-D}\right)^2$	$\left(\frac{D}{1-D}\right)^2$	$\frac{2D}{1-D}$	2D	$\frac{D}{1-D^2}$	$\frac{D}{1-D}$
Norm. SDP _{avg} /Po	$\frac{-D^2+2D+1}{D-D^3}$	$\frac{2(D^3-D+1)}{D(1-D)^2}$	$\left(\frac{1+D}{D(1-D)}\right)$	$\left(\frac{2}{D(1-D)}\right)$	$\left(\frac{2}{D(1-D)}\right)$	$\left(\frac{1}{D(1-D)}\right)$	-----	$\left(\frac{1+3D^2-2D^3}{D-D^3}\right)$	-----
Switch Voltage Stress (V _s /Vin)	$\frac{1}{1-D}$	$\frac{2D^2-2D+1}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{1}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	1	$\frac{1}{1-D}$	$\frac{1}{1-D}$
Diode Voltage Stress (V _D /Vin)	$\frac{1}{1-D}$	$\frac{1}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	1	$\frac{1}{1-D^2}$	$\frac{1}{1-D}$
Voltage Stress on Capacitors (V _C /Vin)	$\frac{D^2}{1-D}$	$\frac{D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{D}{1-D}$	$\frac{2D}{1-D}$	$\frac{D}{2D}$	$\frac{D^2}{1-D^2}$	$\frac{1}{1-D}$
Output Polarity	Positive	Positive	Positive	Positive	Negative	Positive	Positive	Negative	Negative

Table 3. A comparison of the proposed converter with similar converter in step-up mode.

Topology	Proposed Converter	IN [29]	IN [28]	Conventional boost
Switches	2	2	1	1
Diodes	3	4	2	1
Capacitors	3	2	2	1
Inductors	2	2	1	1
Number of Elements	10	10	8	4
Voltage Gain	$\frac{1+D}{1-D}$	$\frac{D}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
Norm. SDP _{avg} /Po	$\frac{2}{1-D^2}$	$\frac{2D^3-D^2+1}{D(1-D)^2}$	-----	-----
Switch Voltage Stress (V _s /Vin)	$\frac{1}{1-D}$	$\frac{1}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
Diode Voltage Stress (V _D /Vin)	$1 \frac{D}{1-D} \frac{D}{1-D}$	$1 \frac{D}{(1-D)^2} \left(\frac{D}{1-D}\right)^2 \frac{D}{1-D}$	$\frac{1}{1-D} \frac{1}{1-D}$	$\frac{1}{1-D}$
Voltage Stress on Capacitors (V _C /Vin)	$\frac{D^2}{1-D} \frac{D}{1-D}$	$\frac{D}{1-D}$	$1 \frac{1}{1-D}$	$\frac{1}{1-D}$
Output Polarity	Positive	Positive	Negative	Positive
Continuous Input	YES	YES	NO	YES

3.4. Inductive component and boundary condition

The discrete inductors must be designed such that the Continuous Conduction Mode (CCM) of operation is guaranteed for the proposed converter. Considering this requirement, the CCM condition is calculated based on the alternative circuit that is presented in Fig. 4(a) for inductors L_1 and L_2 as below.

$$\begin{cases} L_1 \geq \frac{(1-D)^2}{(1+D)^2} \times \frac{R_o}{f_s} \\ L_2 \geq \frac{D(1-D)}{(1+D)} \times \frac{R_o}{f_s} \end{cases} \quad (40)$$

Here, f_s represents switching frequency and R_o is load resistance. Therefore, the boundary conditions for L_1 and L_2 are as follows:

$$\begin{cases} \tau_{L1B} = \frac{(1-D)^2}{2(1+D)^2} \\ \tau_{L2B} = \frac{D(1-D)}{2(1+D)} \end{cases} \quad (41)$$

According to (41), Fig. 11 illustrates the relationship between $\tau_{L_{1,2}}$ and duty cycle D . For $\tau_{L_1} > \tau_{L1B}$ and $\tau_{L_2} > \tau_{L2B}$, the circuit will operate in $L_{1,2}$ -CCM; otherwise, it works in $L_{1,2}$ -DCM. In order to measure the total inductive component required to validate proper CCM functioning in the proposed converter, the normalized total time constant of the inductive components can be written using (41),

$$\tau_{tot} \geq \frac{-D^3 + D^2 - D + 1}{(1+D)^2} \quad (42)$$

Where,

$$\tau_{tot} = \tau_1 + \tau_2 = \frac{L_1 f_s}{R_o} + \frac{L_2 f_s}{R_o} \quad (43)$$

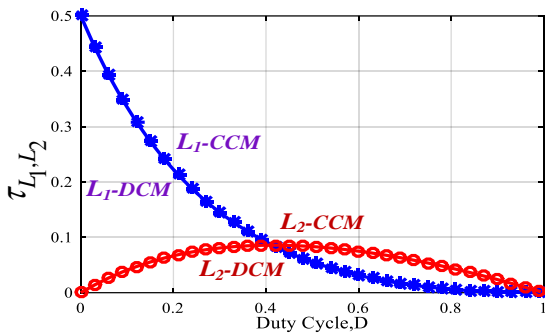


Fig. 11. Boundary conditions for the proposed converter.

The normalized total time constant of the inductive components is also calculated for the proposed converter and compared with [18],[19], [22] and [29] in

Fig.12. In other words, if the inductances are designed such that guarantee the normalized total time constant to be higher than the corresponding curve, can be said that the converter operates in CCM. As seen from Fig. 12.

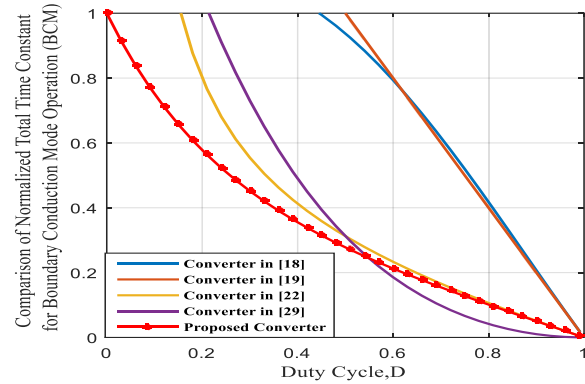


Fig. 12. Comparison of the normalized total time constant for boundary conduction mode operation.

4. SIMULATION RESULTS AND BUILDING A PROTOTYPE

The proposed converter has the ability to operate in both modes. Moreover, the developed buck-boost converter was simulated and examined in laboratory to approve the validity of the theoretical and experimental results. Table 4 shows the list of components used for experiments and simulation of proposed converter. The values of these parameters have been chosen based upon equations (31-37) and (14-18). Inductors' currents variations set 30%; voltage variations across capacitors C_1 , C_2 and C_o are regulated less than 5%, 5% and 0.2%, respectively. The capacitance of C_1 , C_2 and C_o was calculated based on the ripples of capacitor voltage based on equation (36-37) and the inductance of L_1 and L_2 was chosen based on the ripples of inductor currents. The level of input voltage of the intended converter changes from 15V dc to output voltage 60V dc with positive polarity in the step-up mode. The waveforms of L_1 and L_2 inductor currents in the CCM mode and also the input continuous current flow in the converter's input can be clearly observed. Moreover, given 15V input voltage and 0.6 duty cycle, the mean current of inductors L_1 and L_2 equal 6A, 1.5A, respectively, according to equations (14). According to equations (13) and (19), the voltage of capacitors C_1 , C_2 and C_o is about 22.5V, 37.5V and 60V, respectively. Diodes D_1 , D_2 and D_3 and the power switches S_1 , S_2 were chosen based on the components' current stress and voltage. The voltages stress of these five components was calculated to be 15V, 37.50V and 37.50V, 0V, 37.50V, respectively, according to equations (15) and (16). In addition, the peak and overshoot

values were also considered in computing the type of diode and switch.

Table 4. The results of simulations and experiments.

Structure Parameter	Structure I		Structure II
	Step-down Mode	Step-up Mode	Step-up Mode
Input voltage	15V	15V	15V
Output voltage	9V	36V	60V
Duty Cycle	0.3135	0.6	0.6
Load (R)	10Ω	36Ω	40Ω
Switching Frequency	40KHZ		
Inductors L_1, L_2 R_{L1}, R_{L2} ,	165μH, 483μH, 0.021Ω, 0.12Ω		
Capacitors C_1, C_2, C_o R_{C1}, R_{C2}, R_{C_o}	33μF-63V, 22 μF-160V, 220 μF- 250V 0.051Ω, 0.022Ω, 0.011Ω		
Mosfets	IRFP4668PBF ($R_{DS} = 9.7m\Omega$)		
Diodes	MBR10100 ($V_F = 0.85V$)		
DC Power Supply	GW Instek GPS-4303		
Digital Oscilloscope	MSO-2202E		

In step-down mode, the average current of inductors L_1 and L_2 is equal to 1.7A and 0.89A, respectively, when the input is set to be 15V and the duty cycle is 0.3135. Moreover, the amount of voltage stress imposed on capacitors C_1 , C_2 and C_o is equal to 2.2V, 6.8V and 9V, respectively. Furthermore, according to the analytic equations, the voltage stresses imposed on diodes and switches are 15V, 6.85V, 6.85V, 15V and 6.85, respectively. Fig.13 shows the simulation waveforms of the intended converter in both step-

down/step-up modes in CCM mode operation using the PLECS simulation. It shows inductor currents, capacitors and diodes voltage, output voltage and current, switches voltage and gate-source voltage of the MOSFET.

5. EXPERIMENTAL RESULT

The operation of the proposed converter and accuracy of the mathematical analysis through the laboratory prototype are presented in Figs.14 and 15 that show the waveforms of the intended converter in dual modes, determined in the laboratory. The results of the step-down mode converter experiments are shown in Fig.14. The output and input voltages are shown in Fig.14 (a) which are 9V and 15V. Fig. 14(b) shows the current across L_1 and L_2 . The voltages of the switches and diodes are shown in the Figs. 14(c) and (d) where $V_{D1} = 15V$, $V_{D2} = 7.4V$, $V_{D3} = 7.5V$, $V_{S1} = 15V$ and $V_{S2} = 7.2V$.

Some of the basic waveforms of the proposed converter are shown in Fig. 15 in step-up mode. Fig. 15(a) confirms that the output and input voltages are approximately 60V and 15V, respectively. Fig. 15(b) shows the current of the inductive elements. The stress voltages on S_2 , D_2 and D_3 are shown in the Fig. 15(c) that are approximately 38.6 V, 15 V and 38.8 V, which satisfies the equation in (15) and (16).

A picture of the prototype made is presented in the laboratory Fig.16. According to the tests results, it can be concluded that the proposed converter has a completely validated operation while confirming the principles of operation and the features claimed in former sections. The efficiency curves of the intended boost converter can be observed in terms of the output power and output current, respectively (Figs.17 (a) and (b)). These curves are the results of theoretical and experimental evaluations of the proposed converter, which have been investigated in step-up mode. According to theoretical calculations and experimental results in this mode for output current 2.2A, the efficiency of proposed converter is obtained approximately 95.7%. The experimental results of proposed converter with IRFP4668PBF MOSFET and MBR10100 diodes in step-up/down mode are investigated.

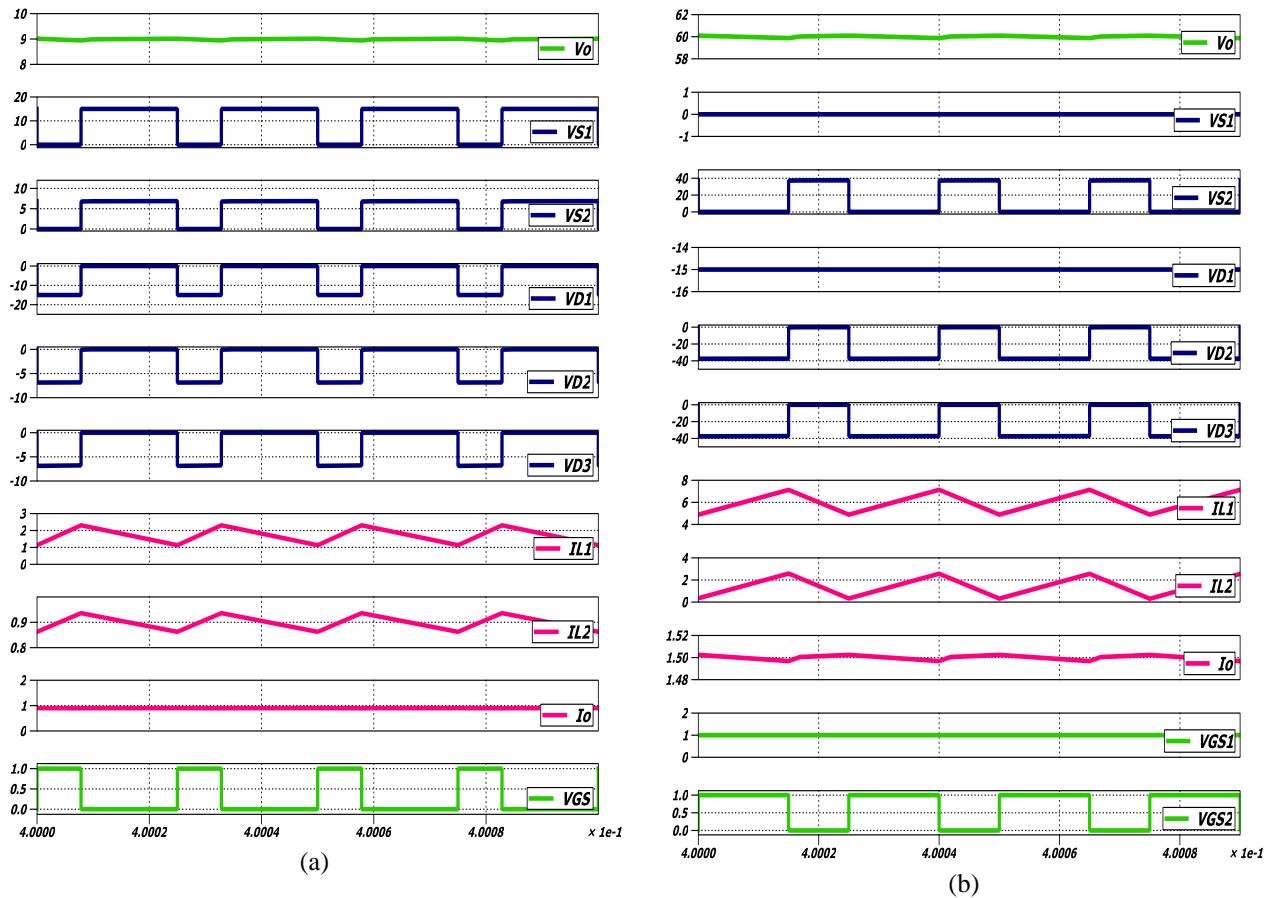


Fig. 13. Simulation waveforms in PLECS for the step-up/down mode of proposed converter. (a) Waveforms of step-down mode (structure I). (b) Waveforms of step-up mode (structure II).

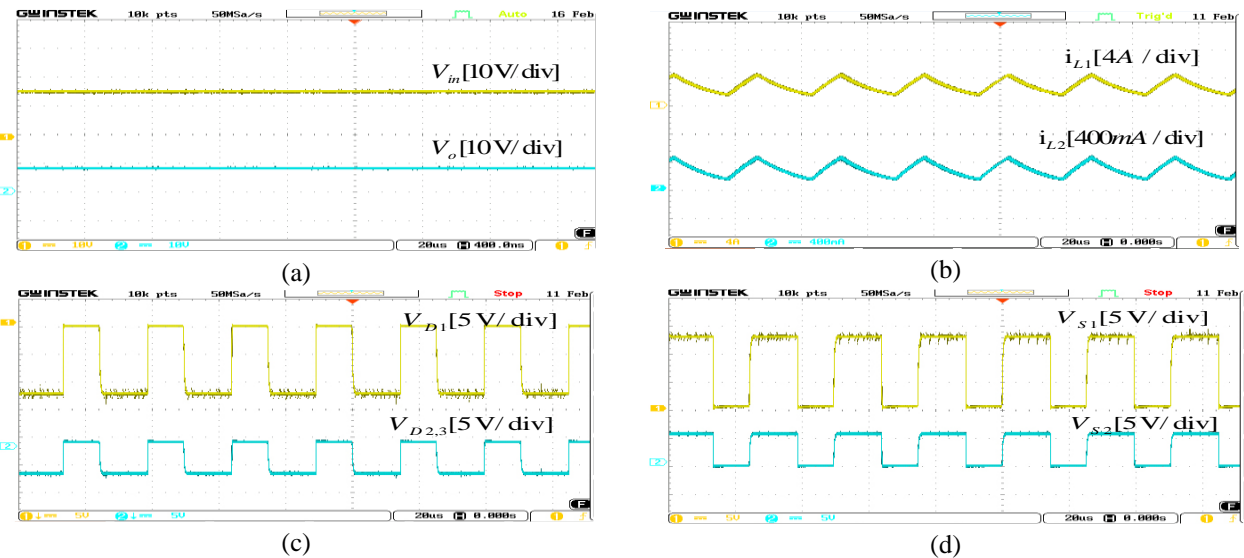


Fig. 14. Experimental results in the step-down mode. (a) Input and output-voltage waveforms: V_{in} , V_o . (b) Inductor current waveforms: i_{L1} , i_{L2} . (c) Diode voltage waveforms: V_{D1} , $V_{D2,3}$. (d) Switch voltage waveforms: V_{S1} , V_{S2} .

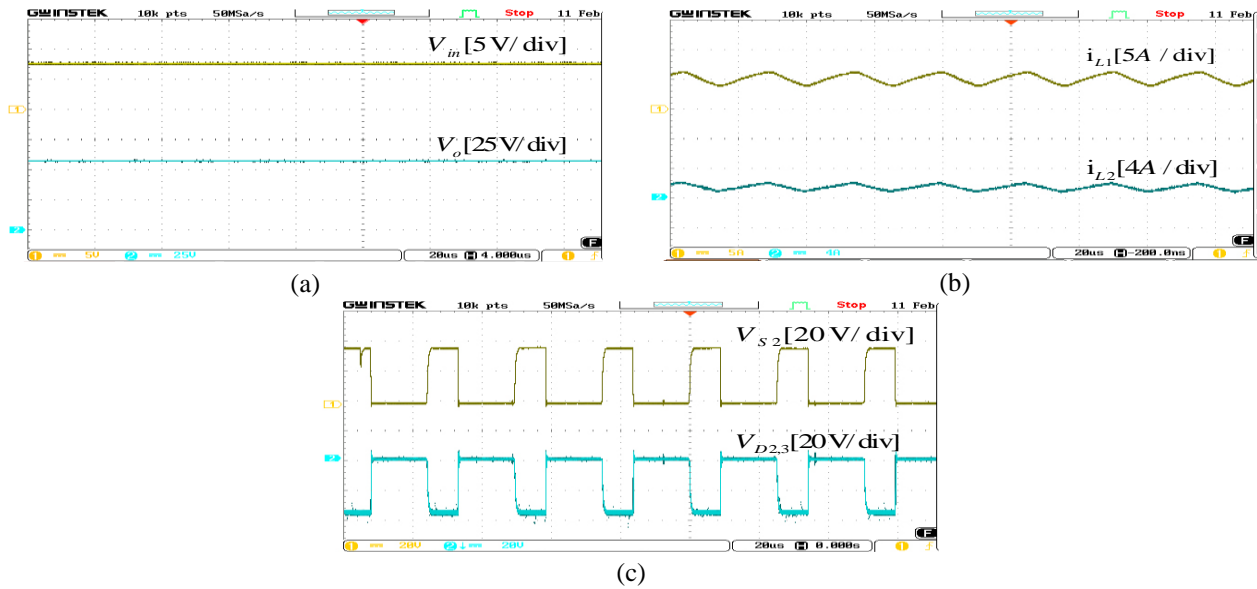


Fig. 15. Experimental results in the step-up mode. (a) Input and output-voltage waveforms: V_{in} , V_o . (b) Inductor current waveforms: i_{L1} , i_{L2} . (c) Switch and Diode voltage waveforms: V_{S2} , $V_{D2,3}$.

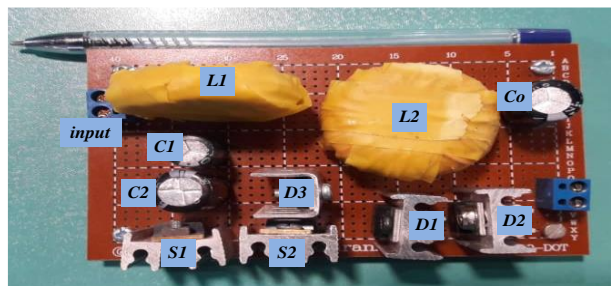


Fig. 16. Laboratory made prototype.

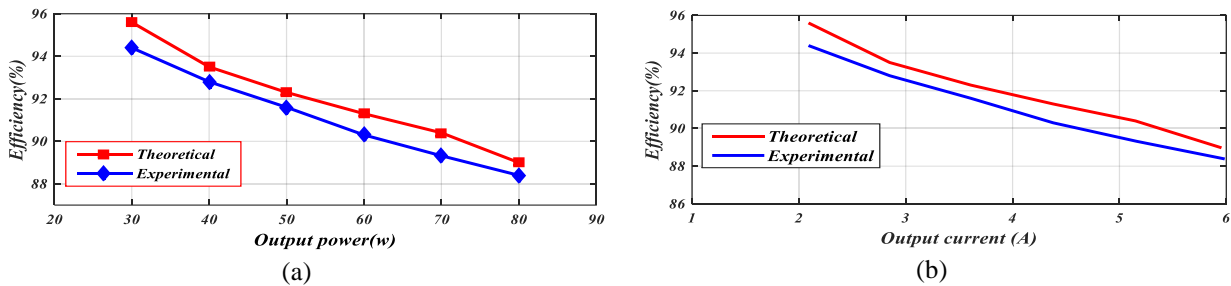


Fig. 17. Results of the theoretical and experimental evaluation of the proposed converter’s efficiency. (a) Efficiency versus output power. (b) Efficiency versus output current.

6. CONCLUSION

A flexible, positive output DC/DC converter with dual working modes was proposed, which is capable of running in the step-up or step-up/down mode and depends on the special application. In both modes, total SDP is lower compared with other DC/DC converters. In this converter, the DC voltage transfer ratio is improved without using any isolated transformers or coupled inductors. An intrinsically continuous input and high voltage gain ratio in the step-up mode make

use it in a wide range of industrial applications to fulfil public needs, especially in PV systems, solar power optimizers, and inverters. This freedom degree for the step-up mode with two voltage gain ratios is an advantage of the proposed converter, and the necessity for the topology choice is not only a high gain but also working versatile. The performance of the proposed converter was compared with similar ones in terms of the number of components, voltage gain, stress on elements, and total switching device power, implying

that the proposed converter is superior to other competitors' converters.

APPENDIX

Here, using the proposed converter with dual working mode for photovoltaic inverter is considered. The PV inverter's structure with grid-side inductor filter L_g , diodes, switches, output capacitor and Lifting capacitor are presented in Fig.18. The output voltage of PV changed by the proposed DC/DC converter with two different voltage gain ratios in step-up mode and one in step-down mode. Switches S_1 and S_2 are controlled synchronously by PWM in buck-boost mode. While, switch S_1 is always on and switch S_2 is controlled by PWM in boost mode.

Switches: $S_1, S_2, SP1, SP2, SN1$ and $SN2$, **Diodes:** D_1-D_3

Inductors: L_1, L_2 , **Grid-side inductor filter:** L_g

Lifting capacitor: $C_{DC-Link}$, **Output capacitor:** C_o

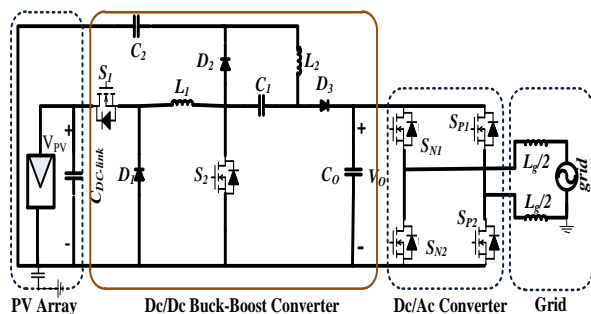


Fig. 18. The proposed PV Inverter.

REFERENCES

- [1] F. Blaabjerg, R. Teodorescu, Z. Chen, and M. Liserre, "Power Converters and Control of Renewable Energy Systems," 2004.
- [2] F. Blaabjerg, C. Zhe, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Transactions on Power Electronics*, Vol. 19, pp. 1184-1194, 2004.
- [3] T. V. Jensen and P. Pinson, "RE-Europe, a large-scale dataset for modeling a highly renewable European electricity system," *Scientific Data*, Vol. 4, p. 170175, 2017.
- [4] R. Reshma Gopi and S. Sreejith, "Converter topologies in photovoltaic applications – A review," *Renewable and Sustainable Energy Reviews*, Vol. 94, pp. 1-14, 2018.
- [5] M. H. Taghvaei, M. A. M. Radzi, S. M. Moosavain, H. Hizam, and M. Hamiruce Marhaban, "A current and future study on non-isolated DC-DC converters for photovoltaic applications," *Renewable and Sustainable Energy Reviews*, Vol. 17, pp. 216-227, 2013.
- [6] A. Tahri, H. El Fadil, F. Z. Belhaj, K. Gaouzi, A. Rachid, F. Giri, et al., "Management of fuel cell power and supercapacitor state-of-charge for electric vehicles," *Electric Power Systems Research*, Vol. 160, pp. 89-98, 2018.
- [7] H. Liu, H. Hu, H. Wu, Y. Xing, and I. Batarseh, "Overview of High-Step-Up Coupled-Inductor Boost Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Vol. 4, pp. 689-704, 2016.
- [8] S. Saravanan and N. R. Babu, "Design and Development of Single Switch High Step-Up DC-DC Converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Vol. 6, pp. 855-863, 2018.
- [9] M. Adly and K. Strunz, "Irradiance-Adaptive PV Module Integrated Converter for High Efficiency and Power Quality in Standalone and DC Microgrid Applications," *IEEE Transactions on Industrial Electronics*, Vol. 65, pp. 436-446, 2018.
- [10] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*, 2nd ed. ed.: Boston (Mass.) : Kluwer academic, 2001.
- [11] F. Mumtaz, N. Zaihar Yahaya, S. Tanzim Meraj, B. Singh, R. Kannan, and O. Ibrahim, "Review on non-isolated DC-DC converters and their control techniques for renewable energy applications," *Ain Shams Engineering Journal*, 2021.
- [12] J. C. Rosas-Caro, J. C. Mayo-Maldonado, A. Valderrabano-Gonzalez, F. Beltran-Carbajal, J. M. Ramirez-Arredondo, and J. R. Rodriguez-Rodriguez, "DC-DC multiplier boost converter with resonant switching," *Electric Power Systems Research*, Vol. 119, pp. 83-90, 2015.
- [13] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano, "A DC-DC multilevel boost converter". *IET Power Electronics* Vol. 3(1), pp. 129-137, 2010.
- [14] S. Iqbal, "A Hybrid Symmetrical Voltage Multiplier," *IEEE Transactions on Power Electronics*, Vol. 29, pp. 6-12, 2014.
- [15] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage Multiplier Cells Applied to Non-Isolated DC-DC Converters," *IEEE Transactions on Power Electronics*, Vol. 23, pp. 871-887, 2008.
- [16] H. Ardi and A. Ajami, "Study on a High Voltage Gain SEPIC-Based DC-DC Converter With Continuous Input Current for Sustainable Energy Applications," *IEEE Transactions on Power Electronics*, Vol. 33, pp. 10403-10409, 2018.
- [17] S. A. Gorji, A. Mostaan, H. T. My, and M. Ektesabi, "Non-isolated buck-boost dc-dc converter with quadratic voltage gain ratio," *IET Power Electronics*, Vol. 12, pp. 1425-1433, 2019.
- [18] J. Li and J. Liu, "A Novel Buck-Boost Converter With Low Electric Stress on Components," *IEEE Transactions on Industrial Electronics*, Vol. 66, pp. 2703-2713, 2019.
- [19] K. I. Hwu and T. J. Peng, "A Novel Buck-Boost Converter Combining KY and Buck Converters," *IEEE Transactions on Power Electronics*, Vol. 27, pp. 2236-2241, 2012.

- [20] M. R. Banaei and S. G. Sani, "Analysis and Implementation of a New SEPIC-Based Single-Switch Buck-Boost DC-DC Converter With Continuous Input Current," *IEEE Transactions on Power Electronics*, Vol. 33, pp. 10317-10325, 2018.
- [21] M. R. Banaei and H. A. F. Bonab, "A Novel Structure for Single-Switch Nonisolated Transformerless Buck-Boost DC-DC Converter," *IEEE Transactions on Industrial Electronics*, Vol. 64, pp. 198-205, 2017.
- [22] M. R. Banaei and H. A. F. Bonab, "A High Efficiency Non-Isolated Buck-Boost Converter Based on ZETA Converter," *IEEE Transactions on Industrial Electronics*, pp. 1-1, 2019.
- [23] N. Zhang, G. Zhang, K. W. See, and B. Zhang, "A Single-Switch Quadratic Buck-Boost Converter With Continuous Input Port Current and Continuous Output Port Current," *IEEE Transactions on Power Electronics*, Vol. 33, pp. 4157-4166, 2018.
- [24] S. Miao, F. Wang, and X. Ma, "A New Transformerless Buck-Boost Converter With Positive Output Voltage," *IEEE Transactions on Industrial Electronics*, Vol. 63, pp. 2965-2975, 2016.
- [25] A. Sarikhani, B. Allahverdienejad, M. Hamzeh, and E. Afjei, "A continuous input and output current quadratic buck-boost converter with positive output voltage for photovoltaic applications," *Solar Energy*, Vol. 188, pp. 19-27, 2019.
- [26] J. C. Rosas-Caro, V. M. Sanchez, J. E. Valdez-Resendiz, J. C. Mayo-Maldonado, F. Beltran-Carbajal, and A. Valderrabano-Gonzalez, "Quadratic buck-boost converter with positive output voltage and continuous input current for PEMFC systems," *International Journal of Hydrogen Energy*, Vol. 42, pp. 30400-30406, 2017.
- [27] J. C. Rosas-Caro, J. E. Valdez-Resendiz, J. C. Mayo-Maldonado, A. Alejo-Reyes, and A. Valderrabano-Gonzalez, "Quadratic buck-boost converter with positive output voltage and minimum ripple point design," *IET Power Electronics*, Vol. 11, pp. 1306-1313, 2018.
- [28] F. L. Luo., "Negative output Luo converters: voltage lift technique". *IEE Proceedings - Electric Power Applications* pp. 146(2), pp. 208-224, 1999.
- [29] M. A. Abbaszadeh, M. Monfared, and H. Heydari-doostabad, "High Buck in Buck and High Boost in Boost Dual-Mode Inverter (Hb²DML)," *IEEE Transactions on Industrial Electronics*, Vol. 68, pp. 4838-4847, 2021.
- [30] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," in *Power Electronics in Transportation (IEEE Cat. No.04TH8756)*, , pp. 125-132, 2004.
- [31] Y. Zhang, J. Liu, X. Ma, and J. Feng, "Comparison of Conventional DC-DC Converter and a Family of Diode-Assisted DC-DC Converter in Renewable Energy Applications," *Journal of Power Electronics*, Vol. 14, 2014.