A CMOS Low-Power Noise Shaping-Enhanced SMASH ΣΔ Modulator

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ABSTRACT:
A discrete-time (DT) high-resolution and low-power sturdy multi-stage noise-shaping (SMASH) sigma-delta (ΣΔ) modulator is introduced. It proposes major solution for high-resolution applications relying on M-bit digital input-feedforward (DFF) technique which eliminates a power-hungry analog adder before the stage's quantizer, decreases number of comparators for quantizer implementation and reduces the swing of the integrator's output and a 2nd-order noise-coupling (NC) technique realized by few extra analog paths and enhances the noise shaping of the modulator without adding active blocks. The effectiveness of the introduced modulator is supported by the behavioral simulation and extensive mathematical analyses. The proposed modulator along with conventional one is simulated in a 0.18μm CMOS technology. The results indicate an outstanding improvement in dynamic range (DR) and resolution with less complexity.

KEYWORDS: SMASH Sigma-Delta Modulators, Noise Shaping, Digital Feed Forward, Noise Transfer Function(Ntf), Resolution.

1. INTRODUCTION

The interest in low-power, high-resolution electronic systems with powerful innovations in various applications has attracted the attention of researchers and turned it to developing new architectures for analog to digital convertors (ADCs). Sigma-Delta (ΣΔ) converters offer higher resolution than other ADC converters with using two methods of oversampling and quantization noise-shaping to improve the signal-to-noise ratio and distortion (SNDR) [1]. The structure of MASH modulators eliminates the instability problems associated with higher-order single-loop structures, so that it is suitable for wideband applications. This structure can reach a high-order and noise shaping-enhanced with cascading stable 1st- and 2nd-order modulators. In MASH modulators, except the quantization noise of final stage which is shaped appropriately, the others are canceled by a digital cancelation logic. In general, the number of integrators in a modulator determines the order of NTF. The NC technique for ΣΔ ADC structure increases the total NTF while the number of integrators remains unchanged [2-4].

From [5, 24], "By using the analog feed-forward (AFF) path in the ΣΔ modulators, in addition to reducing the output swing of integrators, the modulator effectiveness is also improved". The main drawback of the AFF path is dependence on analog adder for the quantizer input. An analog adder needs a powerful op-amp and increases the power consumption [5-7]. The main feature of DFF path is that it eliminates a power-hungry analog adder before the stage's quantizer, decreases number of comparators for quantizer implementation and reduces the swing of the integrator's output [8-9]. The DFF path increases the input signal swing instead of the loop filter; thereby, reducing the size of sampling capacitor, which results in a higher tolerance in KT/C thermal noise and reduces power consumption [10].

MASH modulators require accurate gain coefficients and high-gain op-amps to delete the first-stage quantization noise [11-12]. The most advanced CMOS technologies enable high-performance op-amps; however, there is the problem of the high-gain requirement. Therefore, a SMASH architecture has been proposed [13]. It's sensitivity to op-amp gain and coefficients errors is lower and also it does not need digital cancelation logic filters that lead to the problem of non-compliance of digital filters with analog filters. The SMASH structure obviates the matching requirement, and therefore low-gain low-power op-amps can be used. Given that STF and NTF are obtained

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by fully analogue components, the problems of finite op-amp gain and coefficients mismatch affects the zeros of the overall NTF and the error appears at the output. This is in contrast to conventional MASH structures where digital filters perform the process of the overall NTF. In SMASH structure, the overall output includes quantizer-noise of all stages, while the output of the MASH structure only has noise of the final stage formed by modulator's NTF [13-14].

Here, a Low-Power Noise shaping-enhanced 2-2 SMASH-ΣΔ modulator is presented using a 2nd-order NC technique to enhance modulator's NTF order and DFF technique to decrease the integrators output's swing. The delay applied to the input DFF path also helps to hold low distortion feature in the system and reduce the speed required for DAC processing and DEM logic operations in the feedback. The effectiveness of the introduced modulator is supported by the behavioral simulation and extensive mathematical analyses. In the following, Section 2 gives the proposed 2-2 SMASH sigma-delta modulator structure. The system simulation results are stated in Section 3. Section 4 elaborates on the circuits implementation results of the introduced architecture. Section 5 is the conclusion.

2. THE PROPOSED ΣΔ MODULATOR

2.1. Sturdy MASH Structure

One of the best structures of modulators is the DT-SMASH modulators [13], which works similar to the MASH structure but it does not require digital cancellation filters. Therefore, SMASH modulator does not have the problem of mismatch in digital filters with analog filters which increases quantize-noise leakage in the modulator output. Fig. 1 illustrates a conventional two-stage SMASH ΣΔ modulator.

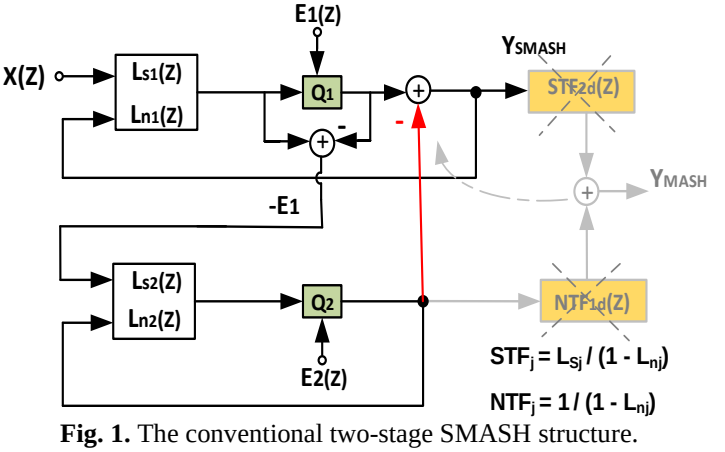


Fig. 1. The conventional two-stage SMASH structure.

Here, L_{sj} and L_{nj} represents the signal and the noise loop filters of j^{th}- stage [15]. STF_{jd} and NTF_{jd}, in MASH-ΣΔ modulators are the digital estimations of STF_j and NTF_j functions for j^{th}- stage, respectively [5]. By foreseeing a complete matching, the analog functions with digital estimations functions, the total output of the MASH structure, Y_{MASH}, is:

$$Y_{MASH} = STF_1 STF_2 X + NTF_1 NTF_2 E_2 \quad (1)$$

The first stage quantization noise, E_1, in MASH structure as the input of the second stage is removed at the output of the entire modulator in the digital domain. In SMASH structure, digital filters are removed and the second and first stages digital outputs are directly processed. The total output of the SMASH structure, Y_{SMASH}, is:

$$Y_{SMASH} = STF_1 X + NTF_1 (1 - STF_2) E_1 - NTF_1 NTF_2 E_2 \quad (2)$$

The proper choice for STF_2 leads to an additional noise shaping for E_1 [14-16]. Sensitivity of SMASH structure to finite op-amp gain and coefficient errors is lower than the conventional MASH structure.

2.2. AFF SMASH Structure

Fig. 2 indicates an AFF implementation of a 2-2 SMASH structure. The feedforward path connects the input signal directly to the quantizer input and reduces the output swing of integrators because they analysis the quantization noise instead of input signal. Assuming ideal components and choosing $STF_2(z) = STF_1(z) = 1$, the output of conventional 2-2 SMASH modulator will be as following:

$$Y = X - \frac{\left(1-z^{-1}\right)^4}{\left(1-z^{-1}+z^{-2}\right)\left(1-2z^{-1}+2z^{-2}\right)} E_2 \quad (3)$$

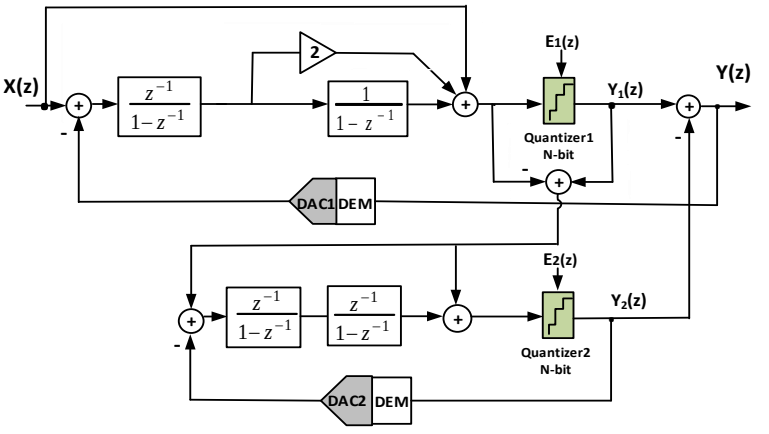


Fig. 2. The Conventional AFF 2-2 SMASH structure.

Here with $STF_2 = 1$, E_1 noise is eliminated from the overall output. In Fig. 2, the performance can be improved with adding a gain of d to the input of the second stage and also connecting the output of the second stage, Y_2, to the input of the integrators in the first stage. This improved structure is shown in Fig. 3 which has higher SNDR than before.

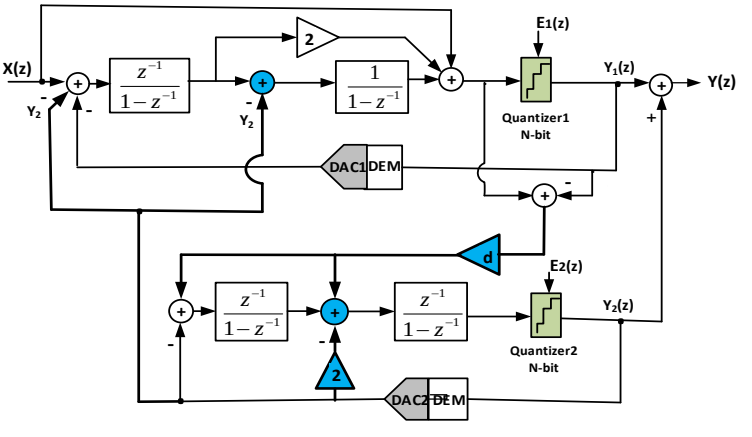


Fig. 3. The improved AFF 2-2 structure.

With $STF_1 = 1$, the total output of this structure is:

$$Y = X + NTF_1\left(1 + d \times STF_2\right)E_1 - NTF_1 NTF_2 E_2 \quad (4)$$

Now, E_1 is shaped with $NTF_1\left(1 + d \times STF_2\right)$. By applying $STF_2 = \frac{1}{d}\left(-2z^{-1} + z^{-2}\right)$, $d = 5$ and $NTF_1 = \frac{\left(1-z^{-1}\right)^2}{1+z^{-1}-z^{-2}}$, $NTF_2 = \left(1-z^{-1}\right)^2$ and the total output is:

$$Y = X + \left(\frac{\left(1-z^{-1}\right)^4}{1+z^{-1}-z^{-2}}\right)\left(E_1 - E_2\right) \quad (5)$$

So, E_1 and E_2 are shaped with order of four at the output.

2.3. Noise Coupling (NC) Technique in SMASH Structure

Because of instability problems of higher order single-loop structures, noise-coupling are recommended for low order structures to improve noise-shaping ability [2]. In addition, the SMASH structure contains cascaded low-order single-loop modulator of which the stability is guaranteed. It is possible to use the higher order single-loop structures in the SMASH modulator for extra shaping order [18-19]. Fig. 4 shows the structure of an NC-SMASH modulator. To make a 2nd-order NC path, it is necessary to connect the feedback path between the first and second stages as a function of the E_2 to the first-stage adder for extra shaping. In addition, this structure transfers a loop delay (z^{-1}) in the first stage from the second integrator output into the new feedback path leading to achieve loop stabilization in the deletion of the active adder before the *quantizer1*. It significantly reduces power consumption through removing the adder required in AFF path.

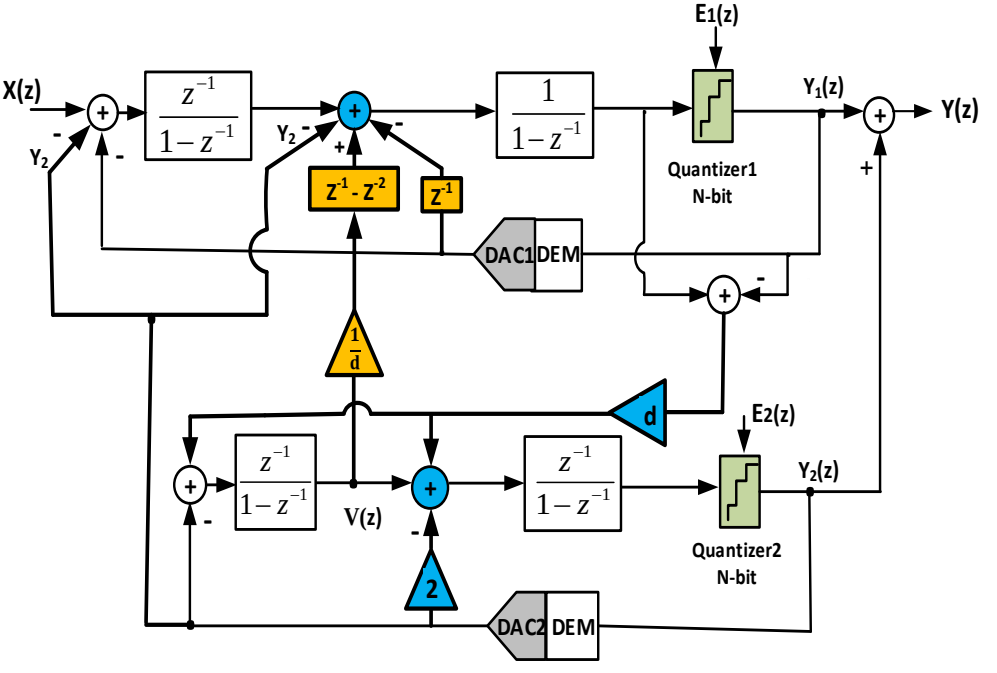


Fig. 4. The NC 2-2 SMASH structure.

The NC 2-2 SMASH modulator output will be:

$$Y = STF_1 X + NTF_1\left((1+d\times STF_2)+z^{-2}(STF_2-1)\right)E_1 \quad (6)$$
$$-\left((1-z^{-1})d\times STF_2\right)E_1 - NTF_1 NTF_2\left(1+\frac{1}{d}\times z^{-2}\right)E_2 +$$
$$NTF_2(1-z^{-1})E_2$$

By applying:

$$STF_1(z)=z^{-1}, STF_2=\frac{1}{d}\left(-2z^{-1}+z^{-2}\right),\quad d=5$$

and $NTF_1 = NTF_2 = \left(1-z^{-1}\right)^2$ the total output will be as following:

$$Y = z^{-1}X + \left(1-z^{-1}\right)^4\left(-0.2z^{-2}\right)E_1 + (1-2z^{-1}-0.2z^{-2})E_1 + \quad (7)$$
$$\left(1-z^{-1}\right)^3 z^{-1}\left(1-0.2z^{-1}+0.2z^{-2}\right)E_2$$

Which shows a six-order noise shaping for E_1 and E_2, plus an additional 2-order noise shaping term for E_1. This additional term is always smaller than the other in-band terms and has negligible effect on performance [28]. Therefore, the output is approximately as follows:

$$Y \simeq z^{-1}X - \underbrace{0.2z^{-2}\left(1-z^{-1}\right)^4}_{NTF_1}E_1 + \quad (8)$$
$$\underbrace{\left(1-z^{-1}\right)^3 z^{-1}\left(1-0.2z^{-1}+0.2z^{-2}\right)}_{NTF_2}E_2$$

Here, NTF_1 has four zeros at $z = 1$ and two zeros at $z = 0$. NTF_2 has three zeros at $z = 1$, one zero at $z = 0$ and a pair of complex-conjugate zeros at $z = 0.1\pm0.43i$ that all of them are withing the desired bandwidth.

2.4. The proposed DFF-NC 2-2 SMASH Structure

To solve the AFF shortcomings, we can use a digital feedforward path [8]. Fig. 5 displays the structure of our modulator. The DFF path contains a M-bit *quantizer3* (ADC_3) which have distinct reference voltage, $V_{reff,ADC3}$,

in comparison with *quantizer1* [22]. Moreover, DAC_3 is needed to feed the input signal to the loop and the *quantizer3* noise, E_3, is fully removed from the output of the modulator. The proposed architecture has several advantages because it uses extended DFF path and the second-order NC technique. It provides sixth-order NTF for both E_1 and E_2 without adding active blocks. Using the DFF path, it increases the input signal and achieves higher SNDR and resolution in the output modulator. The delay in DFF path lowers the time of signal processing for the dynamic element matching (DEM) in the DAC path [24]. The output $Y(z)$ will be as following:

$$Y = X + NTF_1\left(1 + d \times STF_2 + z^{-2}(STF_2 - 1)\right)E_1 - NTF_2 NTF_1\left(1 + \frac{1}{d}z^{-2}\right)E_2 + NTF_1\left(d \times STF_2 - 2z^{-1}K + z^{-2}(STF_2 - 1)\right)E_3 \quad (9)$$

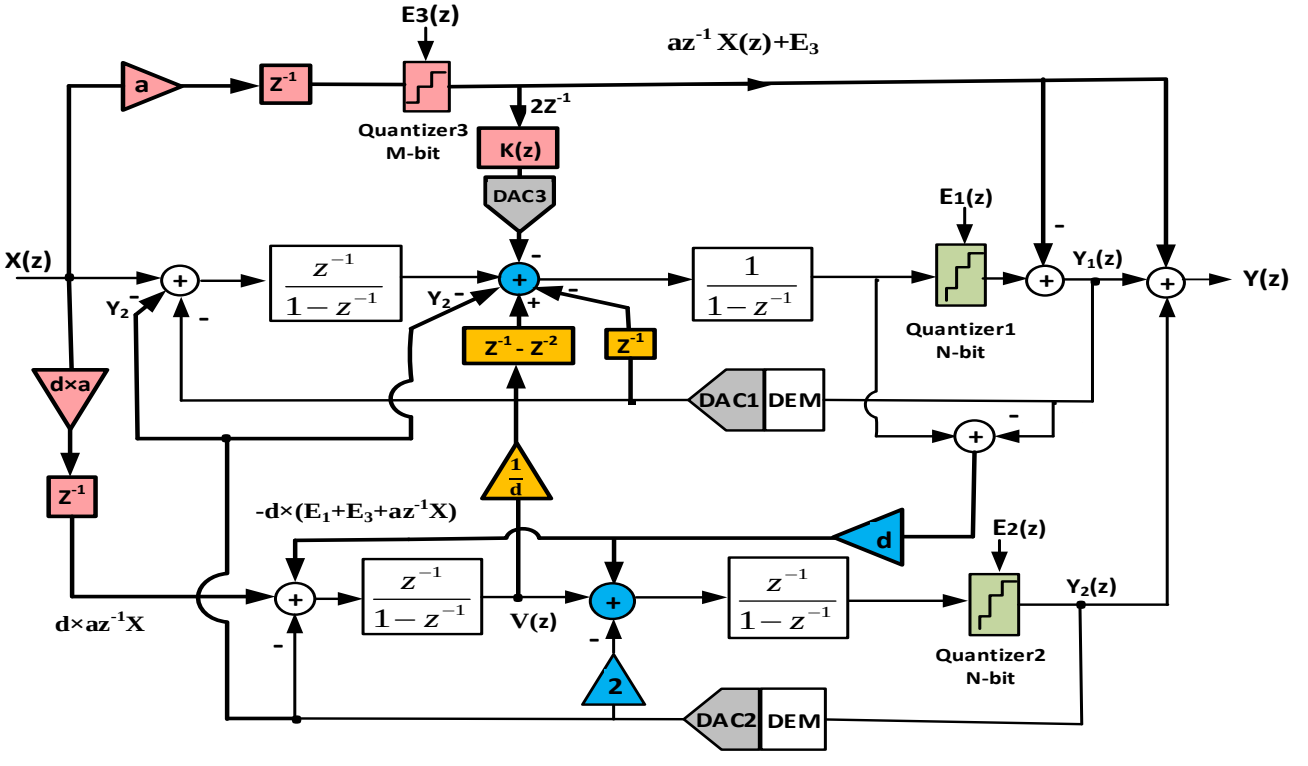


Fig. 5. The Proposed DFF-NC 2-2 SMASH modulator.

As an input signal, the DFF is digitized by an *M*-bit *quantizer3* containing *K(z)* and *M*-bit DAC_3 path in order to nullify of E_3 noise. The *K(z)* must be chosen to eliminate the effect of noise E_3 on the modulator output. Here, by selecting $K = -1 - 0.2z^{-2} + 0.1z^{-3}$, the effect of the E_3 is cancelled to avoid leakage in the output as following:

$$Y = X + NTF_1\left(1 + d \times STF_2 + z^{-2}(STF_2 - 1)\right)E_1 - NTF_2 NTF_1\left(1 + \frac{1}{d}z^{-2}\right)E_2 \quad (10)$$

By applying $STF_2(z) = \frac{1}{d}\left(-2z^{-1} + z^{-2}\right)$, $d = 5$, the NTF_1 and NTF_2 zeros can be optimized. With ignoring additional term for E_1 as before, the $Y_{proposed}$ of the proposed modulator is:

$$Y_{proposed} = X + \underbrace{0.2\left(1 - z^{-1}\right)^5\left(1 + z^{-1}\right)}_{NTF_1}E_1 - \underbrace{\left(1 - z^{-1}\right)^4\left(1 + \frac{1}{5}z^{-2}\right)}_{NTF_2}E_2 \quad (11)$$

Ideally, the output has the input signal, E_1 and E_2 with sixth-order shaping and E_3 is eliminated. Now, NTF_1 has five zeros at z = 1, a zero at z = -1 and NTF_2 has four zeros at z = 1, a pair of complex zeros at z = ±0.447i where all of them are within the signal band.

So, there are increasement in the noise shaping of the overall modulator and with an optimal value for d, the complex zeros of the NTF_2 are optimized.

As mentioned in [19], "one of the best ways to increase the SNDR of high-order wideband modulators is to optimally place a pair of complex conjugate zeros of the NTF from DC to a frequency f_0". So, we achieve lower quantized noises in-band and the decrease of overall noise leads to a higher SNDR [5]. To achieve an optimum value for d, a L[th]-order ΣΔ modulator with one pair of optimized complex zeros is examined. For $L \geq 2$, the NTF_2 (second stage NTF) is [19]:

$$NTF_2 = \left(1 - z^{-1}\right)^L \left(1 + \frac{1}{d} z^{-2}\right) \tag{12}$$

The value of d coefficient to achieve $SNDR_{max}$ and stability of the modulator can be checked using behavioral simulations. Fig. 6 illustrates the position of the NTF_1 and NTF_2 zeros for the introduced architecture.

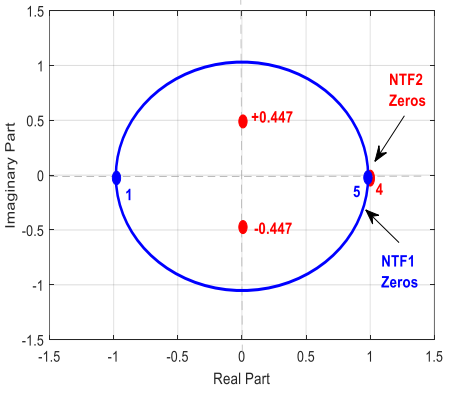


Fig. 6. Location of the zeros for the optimized NTF_1 and NTF_2.

The main advantage of DFF-SMASH ΣΔ modulators is that it does not have digital cancellation logic to suffer from non-compliance of analog and digital circuits. On the other hand, the DFF path with decreasing voltage range, makes the small gain errors caused by the mismatch less obvious. To investigate the mismatch of the DFF path technique in the SMASH-ΣΔ Modulator that is not preventable due to the manufacturing and process variations, with $K(z) = K + \varepsilon$ here ε is an error factor, the modulator output is:

$$Y = X + NTF_1\left(1 + d \times STF_2 + z^{-2}(STF_2 - 1)\right)E_1 - \tag{13}$$
$$NTF_2 NTF_1\left(1 + \frac{1}{d} z^{-2}\right) E_2 - 2z^{-1} NTF_1 \varepsilon E_3$$

Thus, the DFF path noise, E_3, may not eliminated thoroughly and shaped at the modulator's output with second-order noise-shaping to high frequencies, thus its destructive effect on the overall output is reduced.

3. SYSTEM-LEVEL RESULTS

To examine the performance of the introduced DFF-NC 2-2 SMASH ΣΔ, behavioral simulations were done for the modulator shown in Fig. 5 using MATLAB and SIMULINK. To make a comparison, a conventional 2-2 SMASH modulator, a AFF 2-2 SMASH modulator, and a NC 2-2 SMASH modulator were simulated. The OSR, signal bandwidth (BW), and sampling frequency f_s, were selected as 64, 2, and 256MHz, respectively. Two 4-bit quantizers were utilized in first and second stages, and 3-bit quantizer used in the DFF path of the SMASH structure (N= 4, M = 3). The gain between second and first stage, d, was equal to 5. Fig. 7 indicates PSD curve of the introduced modulator and it reaches SNDR=125.4 dB and ENOB=20.55 bits for Fin=0.2657MHz. Fig. 8 compares the PSD of this architecture with the mentioned structures. The best value of coefficient d positions two complex NTF zeros within the signal bandwidth, which leads to in-band noise reduction and SNDR enhancement. SNDR vs input signal amplitude in Fig. 9 shows that the introduced modulator resolution is increased 72 dB compared to the conventional 2-2 SMASH modulator.

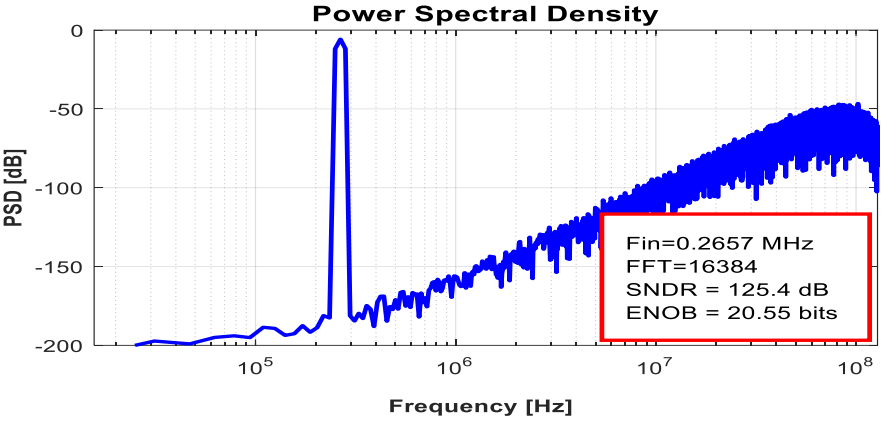


Fig. 7. Output PSD of the proposed modulator.

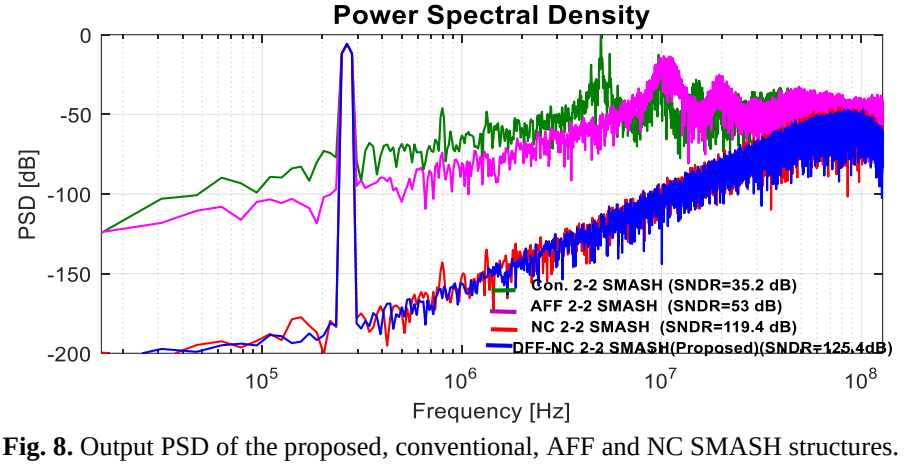


Fig. 8. Output PSD of the proposed, conventional, AFF and NC SMASH structures.

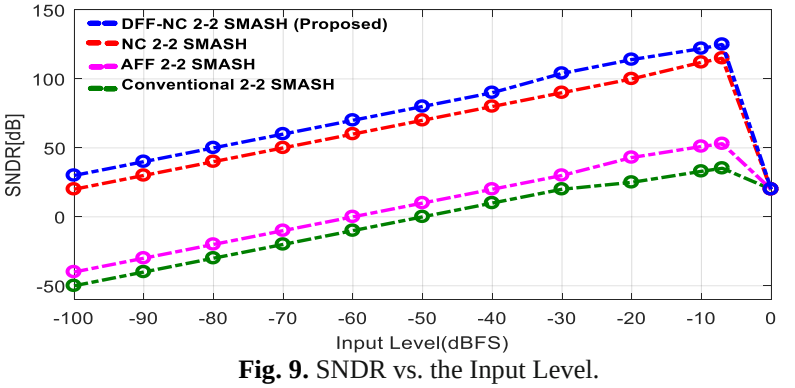


Fig. 9. SNDR vs. the Input Level.

Fig. 10 illustrates the swing of the integrators' output in the introduced modulator. Thus, there is a great decrease in the input swing of the *quantizer1* because of the DFF technique. For the proposed SMASH modulator, full range of $\pm V_{ref}$ and choosing operation range of $\pm 0.31 V_{ref}$, four comparators is required in first-stage quantizer realization. Therefore, the number of comparators applied in the proposed structure considering *quantizer2* (N=4) and *quantizer3* (M=3) is 4 + 15 + 7. Consequently, the DFF structure needs a smaller number of comparators than the AFF structure while the shaping capability is the same in the both structures [5].

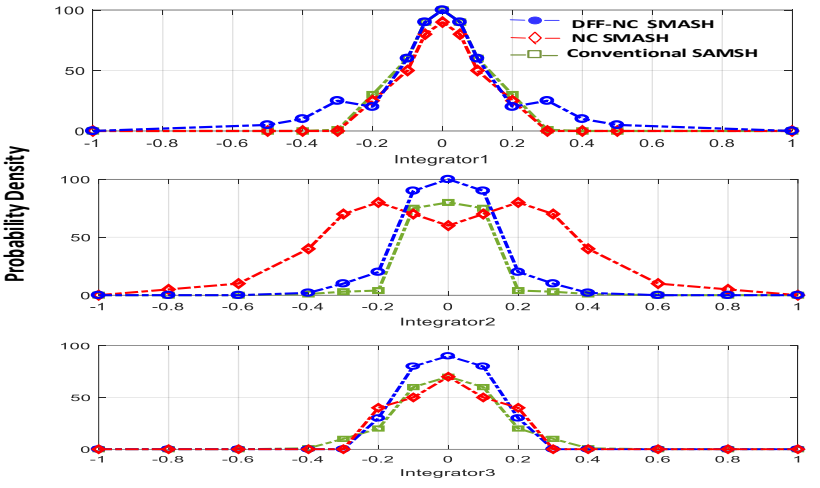
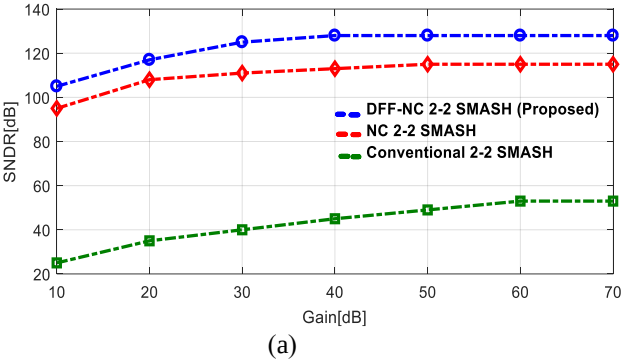


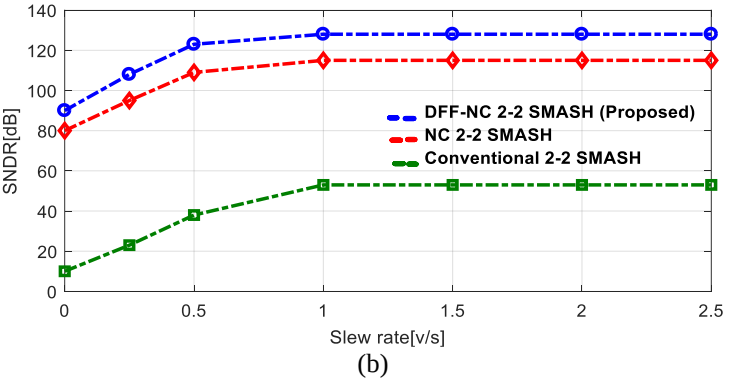
Fig. 10. Signal swing at the integrator1, integrator2 and integrator3 outputs in the SMASH modulator.

3.1. The Result of the Non-ideality Analysis

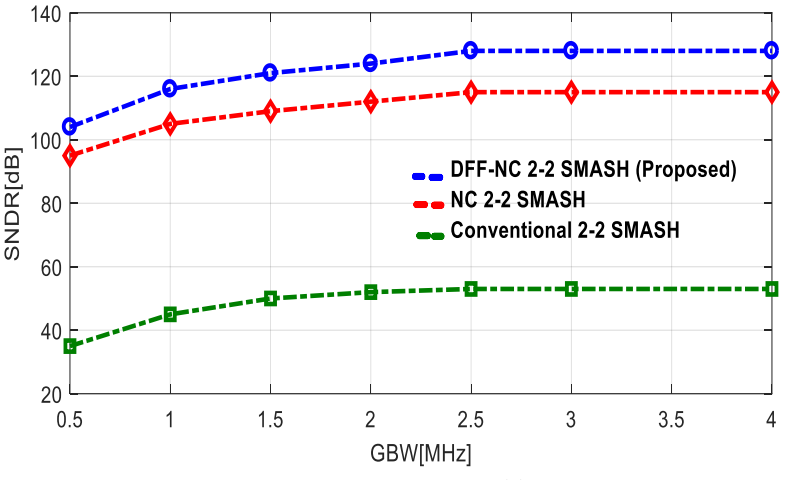
The outcomes of introduced structure with integrators' non-idealities parameters, including finite op-amp gain, slew rate and gain bandwidth were determined in Fig. 11. To make a fair comparison with various modulators, simulation of all structures was with the same OSR, BW, and f_s. SNDR variations illustrate in Fig. 11(a), the lowest op-amp gain in the DFF-NC 2-2 SMASH modulator is 40 dB that is notably less than that of other SMASH structures. Slew rate and GBW requirement shown in Fig. 11(b) and (c), are almost equal for all the structures.



(a)



(b)



(c)

Fig. 11. SNDR variation of the introduced structure as a function of a) op-amp gain; b) slew rate; c) GBW .

3.2. Nonlinear DACs

Using multi-bit quantizers in ΣΔ modulators requires linear multi-bit DACs. Different methods are available to have linear multi-bit DAC that the foremost available technique is data weighted average (DWA) which should be used to reduce the non-linear error of the DAC [20]. Here, only the effect of the first-stage DAC_1 nonlinearity is needed because this effect becomes visible in the modulator input. But the second-stage DAC_2 errors is lowered by second-order shaping if it is referred to the modulator input. Moreover, DAC_3 mismatch is formed by NTF and it has a lower effect on system performance. Consequently, any linearization technique is not used for DAC_3. Thus, the DWA linearization technique is used for the DAC_1. Fig. 12 illustrates the simulated PSD of the modulator DAC using DWA technique and its real . As can be seen, the DWA linearization technique reduces the error due to the DAC nonlinearities and improves the modulator SNDR. In this structure, 96 dB SNDR with the DWA linearization is increased to 121.5 dB, which is just around 2 dB less than the ideal DAC used in the proposed structure.

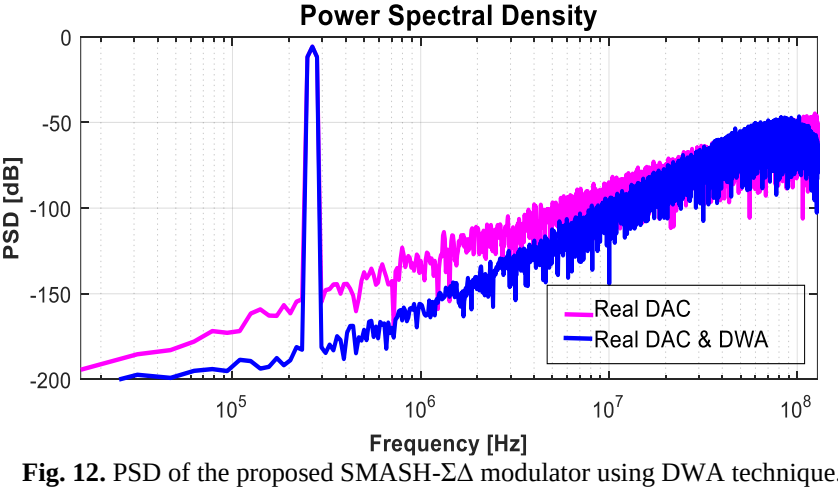


Fig. 12. PSD of the proposed SMASH-ΣΔ modulator using DWA technique.

Table 1 lists the system simulation results of the DFF-NC 2-2 SMASH modulator with Conventional, AFF and NC 2-2 SMASH modulators. The outcomes demonstrate the success of the induced SMASH modulator structure in comparison with other modulators.

Table 1. System simulation results of the DFF-NC 2-2 SMASH modulator with other SMASH structures.

Parameter	Conventional (Fig. 2)	AFF (Fig. 3)	NC (Fig. 4)	**DFF-NC (Fig. 5)**
SNDR [dB]	35.2	53	119.4	**125.4**
ENOB [bits]	6	8.5	19.54	**20.55**
Opamp Gain(A_{0MAX}) [dB]	60	50	50	**40**
Slew Rate [V/S]	1×10^{11}	1×10^{11}	1×10^{11}	**1×10^{11}**
GBW [MHZ]	2.5×10^{3}	2.5×10^{3}	2.5×10^{3}	**2.5×10^{3}**
2^{nd}-integrator Output Swing	0.21	0.85	0.85	**0.31**
NO. of Comparators in 1-main Quantizer(N=4)	15	15	15	**4**
NO. of Comparators in 2-main Quantizer(N=4)	15	15	15	**15**
NO.of Comparators in Extra Quantizer(M=3)	0	0	0	**7**
Total NO. of Comparators	30	30	30	**26**
Order of NTFs	4 , 4	4 , 4	6 , 6	**6, 6**
NO. of Integrators	4	4	4	**4**
NO. of feed-forward adder	1	2	2	**1**

4. CIRCUIT-LEVEL RESULTS

The circuit-level implementation is examined in this section. The simulations are based on a 0.18µm CMOS process with V_{DD}=1.8 V for signal BW= 2-MHz and OSR of 64. The introduced structure was implemented with switched-capacitor (SC) circuits (Fig. 13). To implement the first and second stages 4-bit DACs, 15 unit-capacitors are shared using the input sampling capacitors [19]. Thus, the first integrator feedback gain has no reduce, which leads in less op-amp power. The second integrator has four inputs, the first and third integrator outputs are DAC_3 for the DFF path and Y_2 for second stage output. Two similar imprints of C_{No} and C_{Ne} capacitors are needed to create the noise-coupling path between two stages with delays of z^{-2}. DAC_3 is implemented using seven DAC elements to achieve 8-level DAC [5].

As shown in Fig. 13, different types of switches are used. All floating switches are implemented as bootstrapped switches [27]. NMOS switches are used to connect low constant voltages while CMOS switches connect middle constant voltages.

All of the quantizers are featured with flash structure and its main parts are illustrated in Fig. 14. They contain a regenerative latch, a preamplifier circuit, and a SR latch [22]. In the proposed design, the differential SC latched comparator with input offset storage is used [5]. As shown in Fig. 14, the V_{ref} voltages and input-referred offset are sampled on the C capacitors during φ_1 and φ_{1d} phases, and the input signal crosses over the preamplifier during the φ_{2d} phase. During the sampling phase (φ_1), the preamplifier ensures a reduction in latch reference offset and prevents from entering the latch kickback noise to the comparator driving circuit.

The amplified difference of the comparator is followed by the regenerative latch and large and fast output yielded [26]. The digital output is held by SR latch for one clock cycle until the regenerative latch output is reset [23]. Moreover, CMOS switches sample reference voltage and PMOS switches reset the

preamplifier. The floating switch crossing the input signal has bootstrap structure [5].

Fig. 15 illustrates the output power spectrum (PSD) for 0.328 MHz input sinusoidal signal. The proposed modulator achieves a SNDR of value is 108 dB, and an ENOB of 18.45 . Fig. 16 illustrates the simulated SNDR compared to the full-scale input signal. Clearly, the dynamic range is 112 dB, which is mostly limited by the thermal noises.

Table 2 compares the proposed modulator with other related modulators. The *FOM* (figure of merit) of the analog to digital converters is obtained as follows:

$$FOM = SNDR + 10\log\left(\frac{f_{BW}}{P_{Total}}\right) \tag{14}$$

Where P_{Total} and f_{BW} stand for circuit power consumption and input bandwidth. The system and circuit results show well performance and higher resolution with lower power consumption for the proposed SMASH- ΣΔ modulator in comparison with the others.

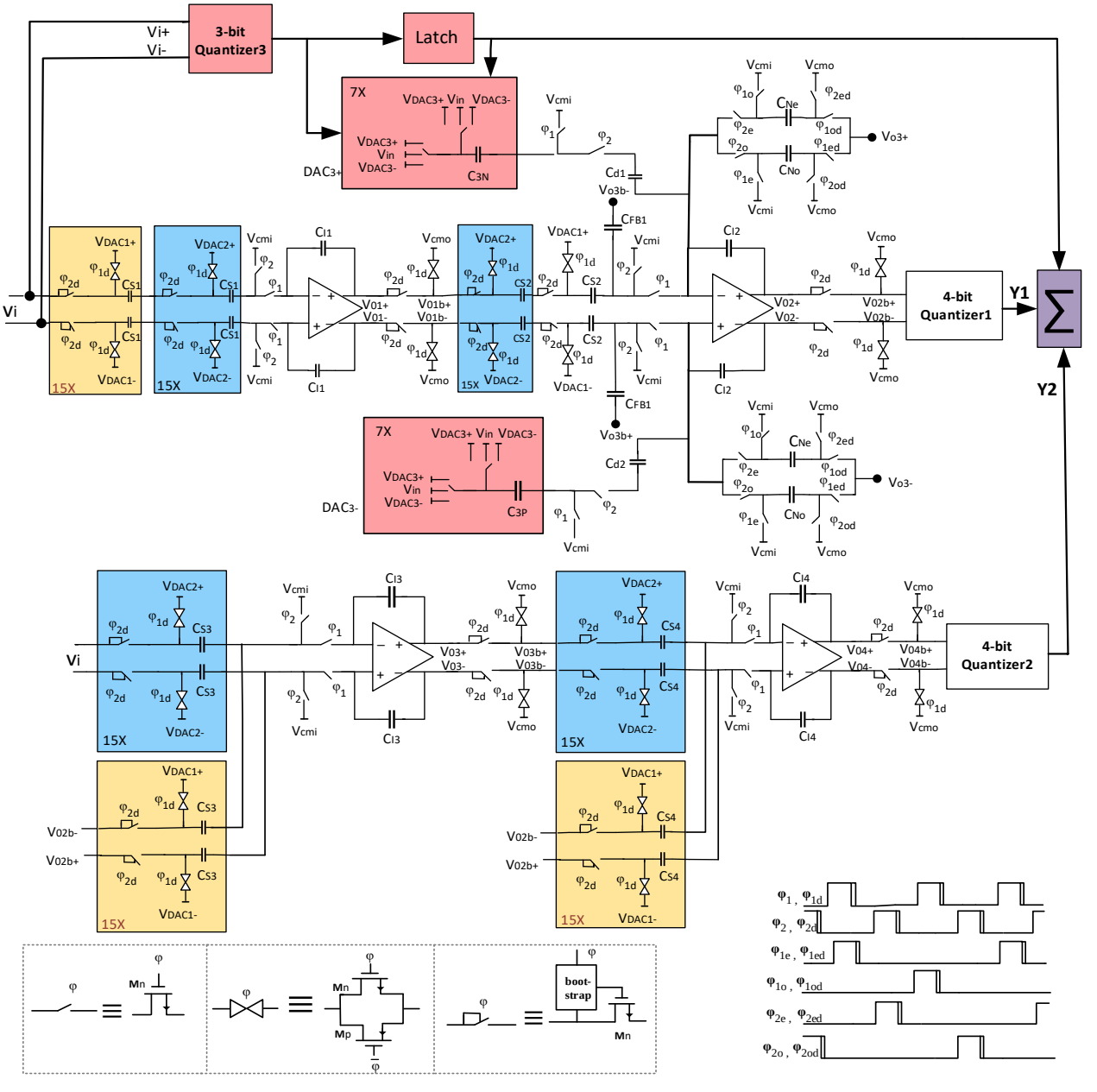


Fig. 13. The SC circuit implementation of the proposed SMASH modulator.

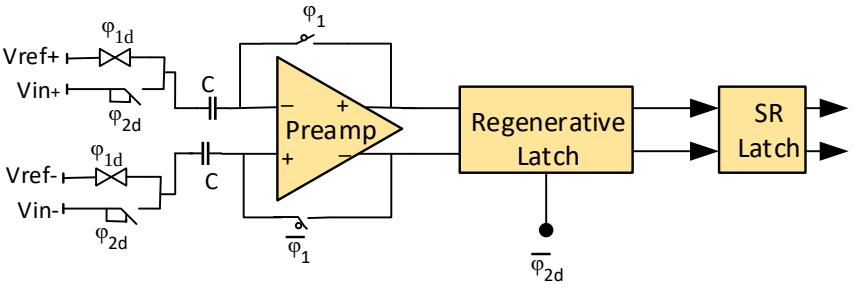


Fig. 14. Main part of the quantizers circuits.

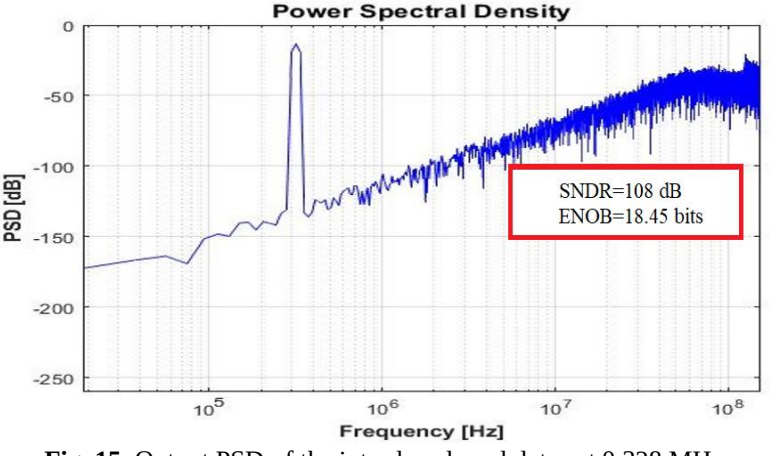


Fig. 15. Output PSD of the introduced modulator at 0.328 MHz.

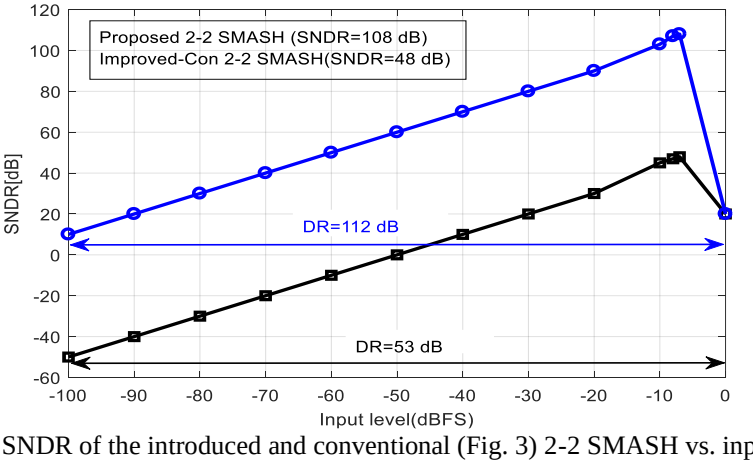


Fig. 16. Simulated SNDR of the introduced and conventional (Fig. 3) 2-2 SMASH vs. input signal amplitude.

Table 2. Performance comparison with circuit simulation results.

Parameter	AFF-NC 2-1 MASH [19]	AFF- 2-2 SMASH [28]*	DFF- 4th Single loop [22]	AFF- 2-2 SMASH [29]*	DFF-NC - 2-1 MASH [5]*	AFF 2-2 SMASH (Fig.3)*	**This Work***
SNDR [dB]	85.2	72.9	58.5	74.5	98.4	49.5	**108**
ENOB [Bits]	13.9	12	11	12	16	8.5	**18.45**
DR [dB]	87	75.8	66	-	101	53	**112**
Power Dissipation (mW)	31.6	20.4	26	3.3	26.3	15.8	**31**
Sampling Rate (MHz)	160	500	128	20	160	256	**256**
Oversampling Ratio	8	12.5	8	16	8	64	**64**
Signal Bandwidth (MHz)	10	20	8	0.625	10	2	**2**
FOM_S [dB]	170	165.7	172	157	184	130	**186**
Technology (nm) CMOS	90	65	65	90	180	180	**180**
Order of NTFs	4	0,4	4	4,4	4	4,4	**6,6**
NO. Of Integrators	3	4	4	4	3	4	**4**
NO. Of feed-forward adder	2	1	1	2	1	2	**1**

*Simulation results.

5. CONCLUSION

An effective architecture was presented for ΣΔ modulators. It is a 2-2 SMASH modulator with 6- order noise-shaping ability. The DFF technique eliminates the need for power hungry analog adder before the quantizer and decreases significantly the number of comparators for quantizer implementation. A second-order NC technique was utilized for achieving a 6-order noise shaping and increasing dynamic range. system-level and circuit-level simulations results supported effectiveness of the induced structure. Therefore, the proposed ΣΔ modulator is appropriate for low-power noise shaping-enhanced wideband usages.

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