Low Power Broadband sub-GHz CMOS LNA with 1 GHz Bandwidth for IoT Applications

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ABSTRACT:
This paper presents a broadband low-power CMOS low noise amplifier (LNA) in 130 nm technology for sub-GHz Internet of Things (IoT) applications. The proposed circuit consists of a current reuse common source amplifier (CSA) in the forward path, and a positive simple transconductance amplifier (PSTA) in the feedback path. Theoretical calculation of the input admittance shows a positive part that presents a parallel inductance. This equivalent parallel inductance in the input can cancel out the input capacitance of CSA and electrostatic discharge (ESD) pad, enhancing the frequency bandwidth in the sub-GHz frequency band. Post-layout was simulated including ESD pads and package model in 130 nm CMOS technology, LNA achieves a voltage gain of 16.5 dB in a frequency bandwidth of 50 MHz to 1.1 GHz, noise figure (NF) of less than 2.4 dB, input return loss (S11) of -11 dB, input third order intercept point (IIP3) of -11 dBm and 1 mW power consumption from a 1 V power supply, showing a good figure of merit compared to other works. The occupied core area is less than 0.002 mm^2.

KEYWORDS: Sub-GHz CMOS LNA, Broadband LNA, Low Power, IoT.

1. INTRODUCTION

The number of low power wide area network (LPWAN) connections will increase with an annual growth rate of more than 100% till 2023 [1]. Also, sub-GHz LPWAN technologies are the main section of many internet of things (IoT) applications [2], [3]. Fig. 1 demonstrates the position of the proposed LNA on a typical IoT device. As shown in figure, LNA plays an important role in improving the overall system performance. In terms of power consumption, the special issues should be considered to receivers designed for LPWAN technologies as they need to sustain long battery life. On the other hand, low power LNAs as the most power-hungry section of IoT receivers are considered by researchers to be worthy of study, in recent years [4]-[8]. Designing of an LNA mainly consists of a trade-off between power gain, bandwidth, power consumption, noise figure (NF), linearity and impedance matching while considering the required stability.

Various techniques have been proposed for broadband LNA design: a) Distributed amplifier (DA), which absorbs the input/output parasitic capacitance of the input/output transistor as part of the transmission line, thereby leading to a broadband operating performance [9] b) Feedback configuration which achieves the wideband performance due to the inherent property of feedback [10], [11] c) Common gate (CG) configuration in which the input impedance equals approximately to 1/gm for a wideband frequency [12], and d) Common source (CS) configuration with broadband impedance matching network [13].

Authors in [14] have achieved a good impedance matching in 6 GHz bandwidth using the resistive feedback technique, but the circuit suffers from high power consumption and a large area due to the on-chip inductors. By combining current reuse, resistor feedback, inductor feedback, mirror bias, inductor peaking and source inductive degeneration techniques in [15], Lin et al. proposed a broadband low-voltage LNA in 100 MHz to 2.5 GHz frequency range but large power consumption and occupied area. In [16], -11 dB S11 is achieved in a frequency bandwidth of 1.3 GHz by using the CG structure and gm-boosting, but the power consumption is as large as 5.7 mW.

In this paper, a sub-GHz LNA in 50 MHz to 1.1 GHz frequency range and power gain of 16.5 dB is proposed. The LNA provides simulated NF of less than 2.4 dB, 1

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dB compression point (P1dB) of -20.5 dBm, S11 of less than -11 dB, input third order Intercept Point (AIP3) of -11.5 dBm, and consumes only 1 mW power from a 1 V power supply. The circuit is composed of a current reuse common source amplifier in forward path and a positive simple transconductance amplifier in voltage-shunt feedback path, using 130 nm CMOS technology. To the author's knowledge, this is the lowest power consumption in this frequency bandwidth in 130 nm CMOS LNA design reported to date. Combining of current-reuse circuit and feedback techniques makes an active inductor at the input that can cancel out the input capacitance due to RF electrostatic discharge (ESD) pad capacitance and input capacitance of CSA. To reduce the noise generated by feedback circuit, the transistors used in feedback are biased at a very low current.

The rest of the paper is organized as follows: Section 2 analyses the proposed circuit, whereas Section 3 presents the results of the post-layout simulation with a comparison with several recent similar works. Finally, the conclusion is presented.

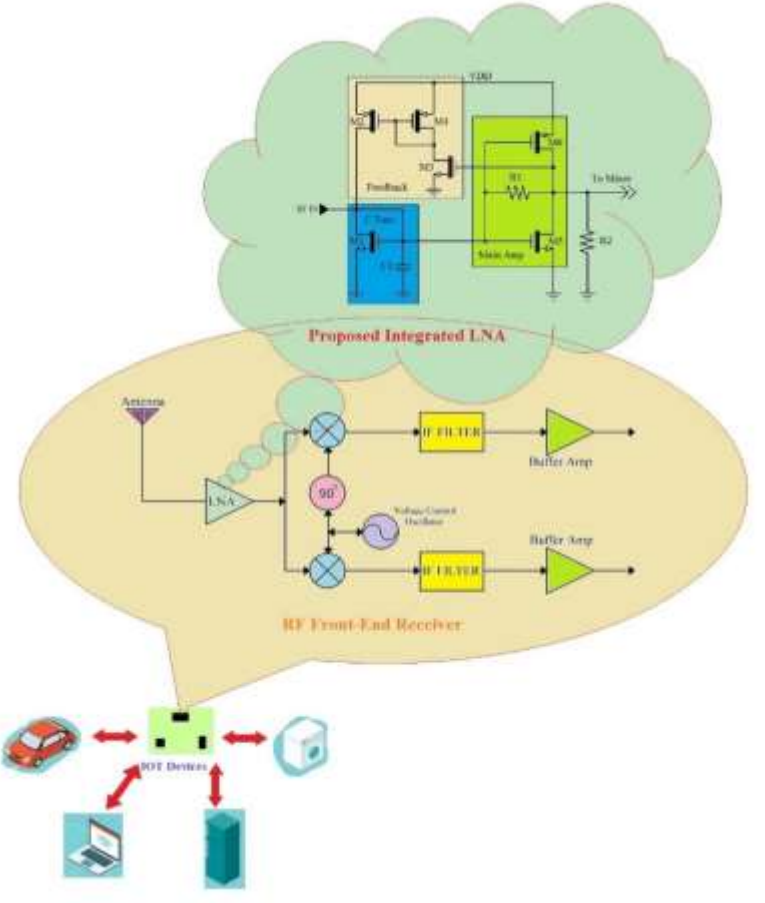

Fig. 1. Position of the proposed LNA on a typical IoT device.

2. ANALYSIS OF PROPOSED CIRCUIT

Fig. 2 shows the proposed circuit. As shown in figure, the circuit is composed of two main sections: a main amplifier, and feedback section. M_5 and M_6 form the current-reuse common source amplifier. M_2 to M_4 is a positive simple transconductance amplifier [17] and build voltage-shunt feedback. M1 plays as a current source to provide DC bias of feedback network. Also, M_1 to M_4 are biased in a very low currents to reduce the noise injected into the input. Using the feedback network, the input impedance of the proposed circuit behaves inductively that can be used to impedance matching in sub-GHz by absorbing the input capacitor including ESD pad, while the power dissipation is still low. ESD pads are often not used in high frequency pads due to its high parasitic capacitor, but here they can be used in the input pad due to cancellation with equivalent inductor seen from the input. ESD has always been an important issue in the semiconductor manufactures as the source of unexpected destruction of integrated circuits and the proposed circuit has been protected in this regard.

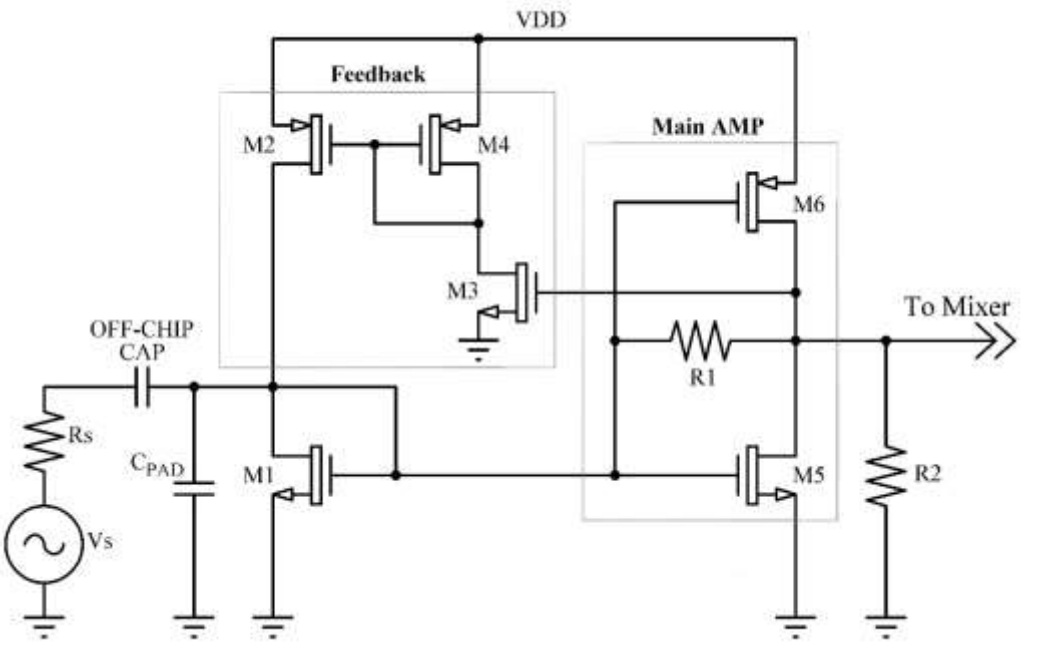

Fig. 2. The proposed circuit.

Fig. 3 illustrates the proposed AC equivalent circuit. The C_L includes load and all parasitic capacitors at the output and C_{in} represents the all input parasitic capacitances including ESD pad. The transconductances of R_1 and M_1 are small; therefore, they are ignored in the figure. Equations (1) to (4) show the input impedance, voltage gain, noise figure, and input AIP3 of the circuit, respectively. Based on (1), the input impedance consists of a series resistor and inductor in parallel with C_{in}. It is evident that C_{in} can be tuned to cancel out the imaginary part of the first term in (1) over a wide frequency range by adjusting the size of input ESD pad, especially in sub-GHz. Also, according to (2) which shows the circuit's gain, increasing the feedback coefficients (i.e., gm_2 and gm_3) decreases gain. Equation (3) indicates the circuit noise figure. According to the equation, the transconductance of M_5 and M_6 plays an important role in the noise figure.

$$Zin = \left(\frac{gm_4}{gm_2 gm_3 (gm_5 + gm_6)(ro_5 \| ro_6 \| R_2)} + \frac{gm_4 j\omega C_L}{gm_2 gm_3 (gm_5 + gm_6)} \right) \left\| \left(\frac{1}{j\omega C_{in}} \right) \right. \tag{1}$$

$$Av = \frac{Vo}{Vs} = \frac{-(gm_5 + gm_6) gm_4 \left(ro_5 \left\| ro_6 \right\| R_2 \left\| \frac{1}{j\omega C_L} \right. \right)}{(gm_5 + gm_6) gm_2 gm_3 \left(ro_5 \left\| ro_6 \right\| R_2 \left\| \frac{1}{j\omega C_L} \right. \right) R_S + gm_4} \tag{2}$$

$$NF = 1 + \frac{(\gamma_5 + \gamma_6)}{R_S (gm_5 + gm_6)} + \frac{\gamma_3 gm_3 gm_2^2 R_S}{gm_4^2} + \frac{\gamma_4 gm_2^2 R_S}{gm_4} + (\gamma_1 + \gamma_2) gm_2 R_S \tag{3}$$

The relationship between the output and input voltages can be obtained by linear assumption of feedback network. The third derivation of this relation, the value of input AIP3 will be calculated as following [18]:

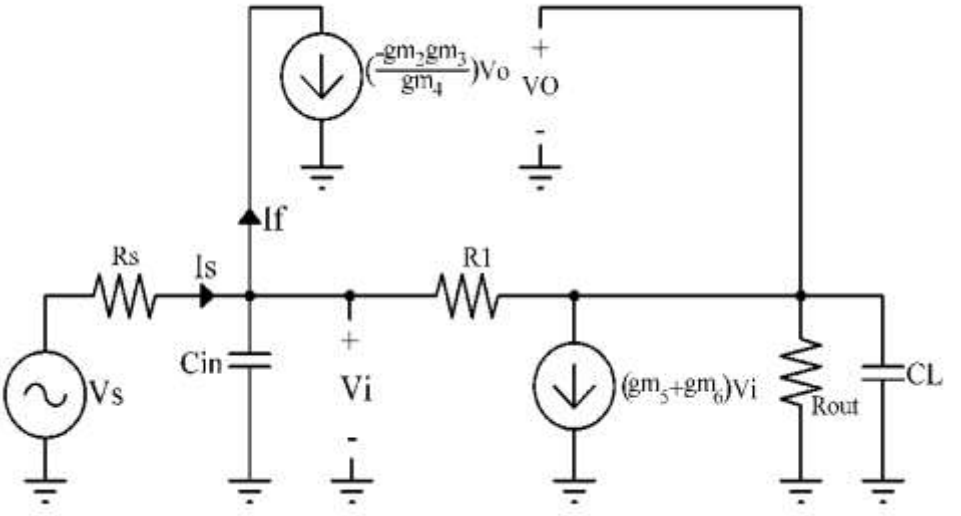

Fig. 3. AC equvalent circuit.

$$AIP_3 = \frac{\left(1+(gm_5+gm_6)\,gm_2\frac{gm_3}{gm_4}R_S\left(ro_5\left\|ro_6\right\|R_2\left\|\frac{1}{j\omega C_L}\right.\right)\right)^2}{(K_5+K_6)\left(ro_5\left\|ro_6\right\|R_2\left\|\frac{1}{j\omega C_L}\right.\right)} \times\sqrt{\frac{2}{3}\times\frac{(gm_5+gm_6)\left(ro_5\left\|ro_6\right\|R_2\left\|\frac{1}{j\omega C_L}\right.\right)}{gm_2\frac{gm_3}{gm_4}R_S}} \quad (4)$$

Where K is $\frac{1}{2}\mu C_{OX}\frac{W}{L}$

Fig. 4 shows the equivalent circuit of input impedance. Analytical and simulated S11 for the proposed circuit has been depicted in Fig. 5 that shows the equivalent circuit agrees well with the simulation results.

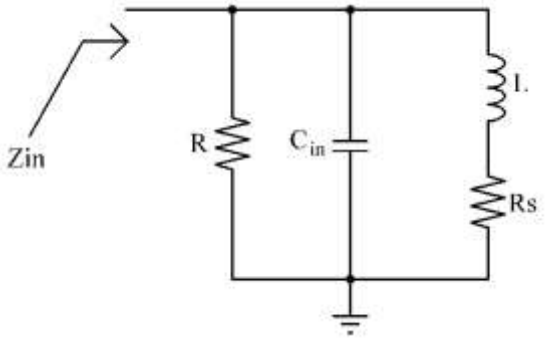

Fig. 4. The equivalent circuit of input impedance.

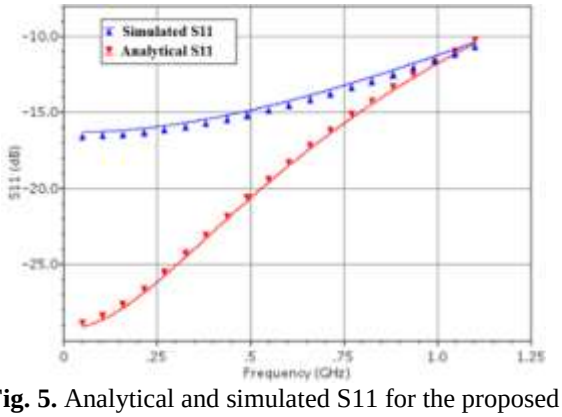

Fig. 5. Analytical and simulated S11 for the proposed circuit.

3. SIMULATION RESULTS

The proposed LNA has been simulated by of Cadence SpectreRF IC design software. All ESD parasitic capacitor and wire bonding effects has been also considered in the simulation as depicted in Fig .6. As shown in Fig. 7, simulated S11 is less than -11 dB up to 1.1 GHz. Also, Fig. 8 illustrates the noise figure and power gain, which are less than 2.4 dB and more than 16.5 dB in the desired band, respectively. Based on Fig. 9, P1dB and input AIP3 in the proposed LNA are -20.5 dBm and -11 dBm, respectively. Fig. 10 demonstrates the performance variation, relative to the typical corner (TT) at 500 MHz. The S11 is the most sensitive parameter, as it varies 3 dB from SS to FF corners, but in the worst case it is still better than -16 dB. In general, the corner variations have acceptable effects on the LNA parameters.

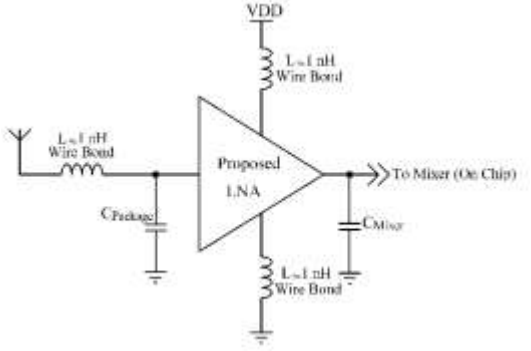

Fig. 6. The bond-wire and load capacitance in LNA.

In the SS corner, the NF increases and the gain declines due to a lower DC current, while in FF the gain goes up and NF decreases because of the increase in DC current. Also, Fig. 11 shows layout of the proposed circuit, which only occupies an area of 0.002 mm2. The corners simulation in different temperatures has also been carried out, that are summarized in Table 1. According to the table, the sensitivity of the circuit parameters to the process is acceptable. MOS sizes and other element values are summarized in Table 2. Also, in Table 3 this work is compared with other recent similar works where the Figure of Merit (FOM) is calculated from (5) [19]. As shown in the table, FOM for the proposed circuit is significantly improved compared to other works due to the very low power consumption.

$$FOM = \frac{Gain[lin] \times BW\,[GHz]}{Power[mW] \times (NF[lin] - 1)} \quad (5)$$

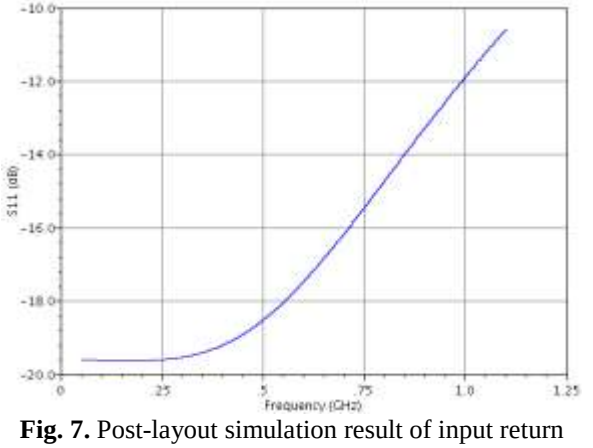

Fig. 7. Post-layout simulation result of input return losses.

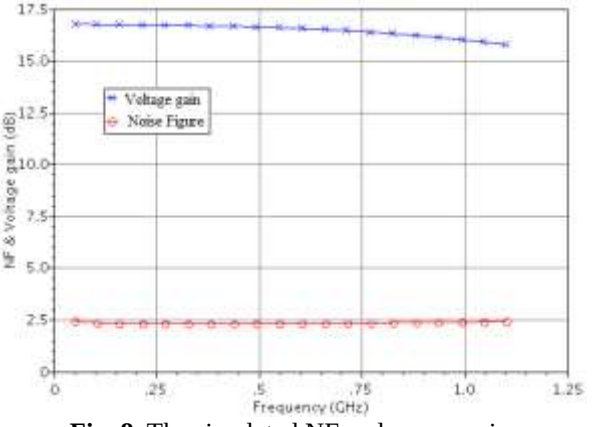

Fig. 8. The simulated NF and power gain.

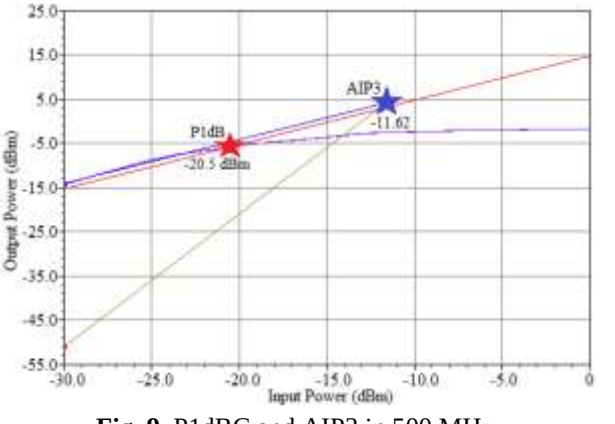

Fig. 9. P1dBC and AIP3 in 500 MHz.

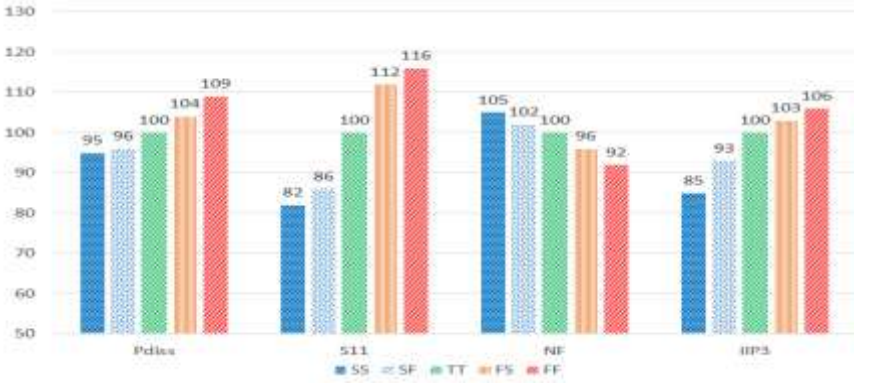

Fig. 10. Performance variation relative to typical corner (TT) at 500 MHz.

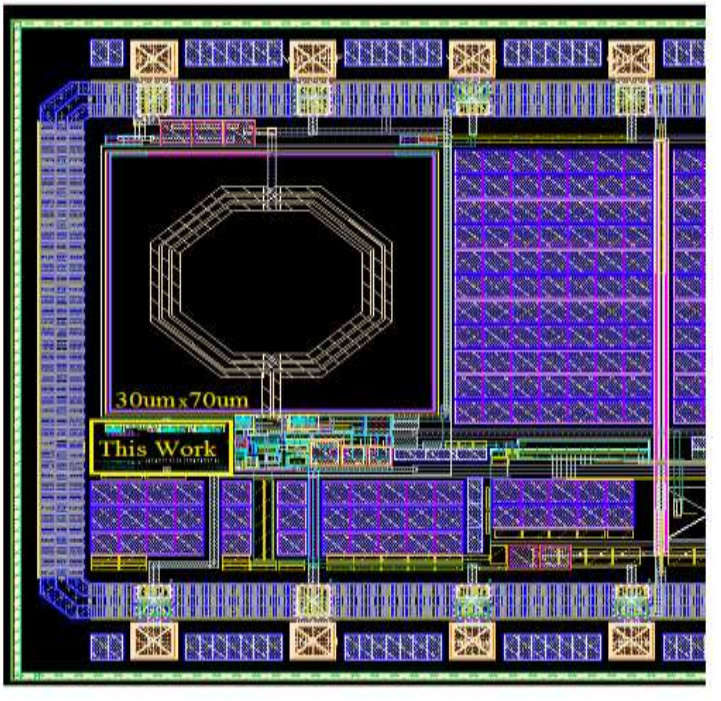

Fig. 11. Layout of proposed LNA Core.

Table 1. Simulated performance summary of the proposed LNA in different process corner cases.

Corner Process	BW (GHz)	Power (mW)	S11 (dB)	Gain (dB)	NF (dB)
TT@ 27˚C	0.05-1.1	1	<-11	16.5	<2.4
SS@ 80˚C	0.05-1.1	0.7	<-9	15	<2.6
FF@ -20˚C	0.05-1.1	1.2	<-11.5	17.5	<2.2

Table 2. MOS sizes and component values of the proposed circuit.

Transistors W(µm) / L(µm)	Resistance (KΩ)	Capacitors (PF)
M1 8 / 0.13	R1 10	Cin 1.6
M2 6 / 0.13	R2 3	
M3 3 / 0.13		
M4 4 / 0.13		
M5 45 / 0.13		
M6 75 / 0.13		

Table 3. Broadband-LNA performance summary in CMOS technology.

References	BW (GHz)	S11 (dB)	Gain (dB)	NF (dB)	IIP3 (dBm)	VDD (V)	Pdc (mW)	FOM (GHz/mW)	CMOS Tech(nm)
[13]	0.1–6.1	< -11	19	2.3	-16	1.2	7.35	9.92	180
[14]	0.1–2.5	< -11	10.2-12.4	<2.8	-2	1	5.5	1.48	180
[15]	0.05–1.3	< -11	24-27.5	2.3-3	-2.2	1	5.7	4.69	65
[20]	0.05-1	< -10	24-30	2.2-3.3	-4	1.2	19.8	1.02	130
[18]	0.9-2.3	< -15	22	2.3	-5.5	0.6	5.2	4.87	90
[19]	0.1–3.4	< -10	16	3.4	-1.46	1	3.3	5.33	130
This Work	**0.05–1.1**	**<-10.5**	**16.5**	**<2.4**	**-11.5**	**1**	**1**	**10.4**	**130**

4. CONCLUSION

In this paper, a broadband low noise amplifier by using 130 nm CMOS technology is presented for sub-GHz IoT applications. The large input capacitance of amplifiers decreases the frequency bandwidth. The proposed feedback network has enhanced the frequency bandwidth by absorbing the input capacitor, including the input capacitance of ESD pad and input capacitance of main amplifier. The post-layout simulation results showed a gain of 16.5 dB, S11 less than -10.5 dB, NF below 2.4 dB with 1 GHz bandwidth and just 1 mW power consumption that indicates a good agreement with analytical results. The circuit core occupies only 0.002 mm^2.

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