Three PWM based Control Technics for Switched Boost Inverter

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ABSTRACT:
Switched Boost Inverter (SBI) operates in buck-boost mode with an extensive spectrum of output voltage obtainable from a specific source voltage. Also, this structure provides superior protection against Electromagnetic Wave Interference (EMI) juxtaposed with the traditional impedance source inverter. The number of energy storage elements in this structure has been reduced, which increases the efficiency of the converter in low-power applications, reducing cost, size, and weight. In this paper, this inverter is analyzed and investigated in different operating modes and steady-state. Also, three different pulse width modulation (PWM) control techniques are presented for this inverter. Simulation results are presented in PSCAD-EMTDC software to validate the calculated relationships and confirm their performance in three different switching methods.

KEYWORDS: Switched Boost Inverter, Pulse Width Modulation (Pwm) Technique, Modified Pwm Method, High Frequency Switching Method.

1. INTRODUCTION

Power electronic converters are essential interface devices for grid integration of renewable energy [1-3]. They are also commonly utilized in various power systems like distributed generation sources, power factor correction devices, hybrid electric vehicles, and air-space industries [4]. Traditional voltage source inverters (VSI) can be used in many applications, but they have problems. Voltage source inverters are not boost inverters. Therefore, they need a high input voltage. Also, high-level voltage generation without interface devices increases the cost of renewable energy systems. In the last few years, researchers have focused primarily on reducing the size and increasing the efficiency of power electronic converters. Therefore, the conventional VSI and CSI (current source inverter) topologies have been improved significantly. These improved topologies are called impedance source inverters [5], [6]. The first impedance source inverter (ZSI) was pioneered by Peng in 2003 [7]. The ZSI includes a passive X-shape network that is coupled to the inverter bridge and the dc power source. Unlike the traditional voltage source inverters, these converters have the advantage of increasing and decreasing the source voltage by virtue of the shoot-through (ST) operation. Thus, the converter output voltage is either stepped-up or stepped-down juxtaposed to the source voltage. One of the essential advantages of this structure is the shoot-through state. This means that in one leg of the inverter, the switches can be turned on together, and a short circuit can occur without causing a current spike. This ability is entirely inapplicable in conventional converters. In addition, the ST state protects ZSI from electromagnetic interference (EMI). Unlike the conventional CSI, CSI based ZSI provides protection against open circuit. These characteristics therefore make ZSI an appropriate topology for varied applications like uninterruptible power supplies, variable speed drive, and renewable power systems [8-10]. However, the cost and size of these converters are notably increased due to the presence of two inductors and capacitors in the impedance network. Therefore, they may not be desirable in applications where weight, cost, and size are of importance e.g. in low-power applications. Further studies have been conducted in terms of improving ZSI. Some of them are focused on presenting new structures for ZSI, and some of them concentrate on the control techniques and the application of these converters. Then improved topologies after the conventional ZSI were achieved in terms of increasing the voltage gain, boost factor,

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efficiency, and output power as well as reducing the number of energy storage elements including inductor and capacitor, the current and voltage stress of the active components [11]. Nevertheless, it is not possible to achieve every goal in one converter. In [12], the quasi ZSI (qZSI) is developed in four different topologies. The q-ZSI also provides equal boost factor as ZSI and all its characteristics. One of the important advantages of this converter is the continuity of the source current and the voltage stress across the capacitors is lower than [8]. In [13-17], different structures were presented to maximize voltage gain by using active switched inductors and capacitor cells. Another type of ZSI propounded in [1] is known as SBI. The operation of this proposed converter is similar to the ZSI converter but with a reduced number of passive components which causes an improvement in efficiency, size, weight, and cost.

There are some of the methods presented to improve the modulation technique of switch boost inverter (SBI). These methods include Space Vector Modulation (SVM), Pulse Width Modulation (PWM), Select Harmonic Elimination (SHE), Model Predictive Control (MPC), artificial intelligence techniques such as neural networks and fuzzy logic, etc. PWM technique for switch boost inverter is a powerful and simple solution that addresses the drawbacks of voltage source inverter. One of the main issues with the voltage source inverter is its limited voltage boost capability, which restricts its application in high step-up systems. The PWM technique overcomes this limitation by providing a flexible and efficient way to control the output voltage of the switch boost inverter. This technique allows for precise control of switching frequency and duty cycle, which enables the system to operate at optimal efficiency while maintaining stable output voltage. Additionally, the PWM technique provides better harmonic performance and reduces electromagnetic interference, making it an ideal solution for high step-up applications. With its ability to overcome the limitations of voltage source inverters, PWM is becoming increasingly popular in various industries, including renewable energy, electric vehicles, and industrial automation.

The switch boost inverter utilizes the shoot-through state of the voltage source inverter to boost the input voltage, whereas the traditional PWM techniques of voltage source inverter do not permit the inverter bridge to be in the shoot-through state. This paper proposed three different PWM techniques suitable for switch boost inverter. Compared to the traditional PWM used in VSI, the three proposed PWM techniques can provide the shoot-through interval without losing the quality of the output voltage waveform and solve the lack of boost ability of VSI. Also, these techniques provided that the sum of the shoot-through duty ratio and modulation index is less than unity.

This work presents a steady-state investigation of the SBI. Also, three PWM control techniques for this inverter are fully described with their key relationships.

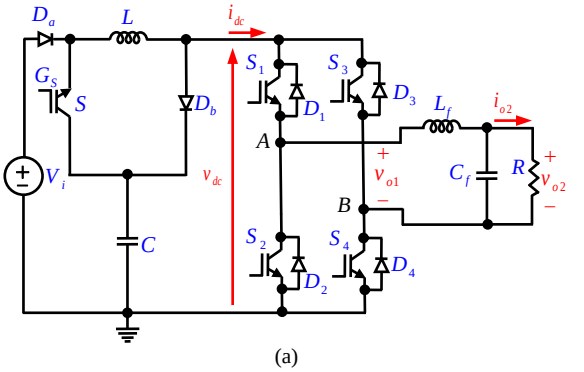
2. REVIEW ON SBI

The power circuit and equivalent circuits of the SBI in [1] are illustrated in Fig. 1. In this converter, an SB (switched boost) network comprising two diodes (D_a) and (D_b), a switch (S), a capacitor (C), and an inductor (L) are mounted in-between the source voltage (V_i) and the inverter bridge. The output section of the inverter has a low-pass LC filter to provide a smoothened load voltage (v_{o1}) waveform. The converter is analyzed in two operating modes for each switching cycle (T_S) shoot-through (ST) and non-shoot-through (nST) states.

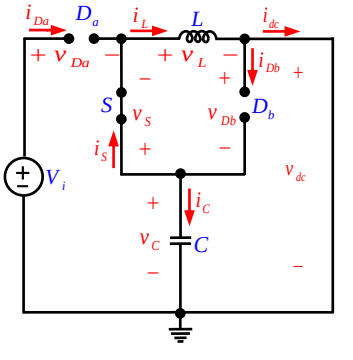
***ST state*:** In Fig. 1(b), the ST equivalent circuit of SBI is shown. In this mode, switches in one or two legs of the full bridge inverter are turned on simultaneously. The duration is determined by D_{ST} where D_{ST} represents the duty cycle of the converter switches. The duty cycle of the ST interval is described as follows:

$$D_{ST} = \frac{T_{ST}}{T_s} \tag{1}$$

T_S represents the switching period and T_{ST} equals the sum of the time intervals of one period in which the ST state occurs, and the number of these periods can be different and depends on the type of switching techniques. However, the ST states are equal to $D_{ST}T_S$ in each switching method.



(a)



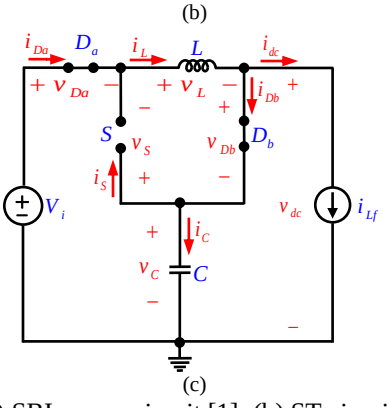


Fig. 1. (a) SBI power circuit [1]; (b) ST circuit; (c) nST circuit

According to Fig. 1(b), *S* is turned-on resulting in the reverse-biased mode of diodes D_a and D_b and therefore does not lead to current flow. *C* is discharged to the *L* through the *S* and inverter bridge. The energy stored in *L* increases. Applying KVL and KCL in this operation mode can be written as:

$$v_L = V_C \tag{2}$$

The inductor voltage for the current is expressed by:

$$v_L = L\frac{di_L}{dt} \tag{3}$$

By replacing (2) in (3), the inductor current is computed by:

$$i_L = \frac{V_C}{L}t + I_{LV} \tag{4}$$

The primary magnitude of current passing through the inductor is expressed as I_{LV} is ST interval. According to (4), the inductor current increases linearly in this operation mode.

The current and voltage relationships of the switch, capacitor, and diodes are computed by:

$$v_S = 0 \tag{5}$$

$$i_S = i_L = \frac{V_C}{L}t + I_{LV} \tag{6}$$

$$v_{D1} = V_i - V_C \tag{7}$$

$$v_{D2} = -V_C \tag{8}$$

$$i_{D1} = i_{D2} = 0 \tag{9}$$

$$v_{dc} = 0 \tag{10}$$

$$i_{dc} = i_L = \frac{V_C}{L}t + I_{LV} \tag{11}$$

$$i_C = -i_L = -\frac{V_C}{L}t - I_{LV} \tag{12}$$

According to (6), the current passing through *S* in ST mode is equivalent to the current passing through *L*. Also, according to relations (7), (8), and (10), it is clear that the voltage stress on D_a and D_b is equal to $V_i - V_C$ and $-V_C$, respectively. The voltage of the dc link is equivalent to zero due to the shoot-through states of the legs of the inverter. The current of the dc link is same as the current passing through *L* as shown in (11).

***nST state*:** The power can be transferred to the load considering the switching technique of the inverter. Since inverter legs are open-circuited at some moments the power transferred to the load is zero. Therefore, in this mode, there are two states for connecting the impedance network to the full bridge inverter. During the initial (1st) state, the inverter bridge is expressed by a current source, and the power is transferred to the load. During the subsequent (2nd) state, the full bridge inverter will be an open circuit. It is worth mentioning that the open circuit mode and its duration can be different according to the switching technique and the modulation index (*M*) of the full bridge inverter. In some switching methods such as the high-frequency switching method, the state of the open circuit does not occur. Nevertheless, the voltage across the component of SBI will be the same per the approximate circuit in Fig. 1(c). In Fig. 1(c), the approximate circuit of SBI in nST interval is depicted. D_a and D_b and *S* are all turned-on. The inverter is fed by the source voltage V_i and *L*. *C* is charged through D_a and D_b. The current passing through *L* in this mode is equivalent to the summation of the current of *C* and the source current of the inverter (DC link current). Applying KVL and KCL in this operation mode can be written as:

$$v_L = V_i - V_C \tag{13}$$

The current passing through *L* in nST interval is obtained from (13) in (3) as follows:

$$i_L = \frac{V_i - V_C}{L}t + I_{LP} \tag{14}$$

I_{LP} is the primary magnitude of the inductor *L* in nST. The current passing through *L* decreases by considering, $V_C > V_i$

The current and voltage relationships of the switch, capacitor, and diodes are computed by:

$$v_S = V_C - V_i \tag{15}$$

$$i_S = 0 \tag{16}$$

$$v_{D1} = v_{D2} = 0 \tag{17}$$

$$i_{D1} = i_L = \frac{V_i - V_C}{L} t + I_{LP} \quad (18)$$

$$v_{dc} = v_{dc,\max} = V_C \quad (19)$$

$$i_{dc} = \begin{cases} i_{Lf} & \text{for state 1} \\ 0 & \text{for state 2} \end{cases} \quad (20)$$

$$i_C = i_{D2} = i_L - i_{dc} = \begin{cases} \frac{V_i - V_C}{L} t + I_{LP} - i_{Lf} & \text{state 1} \\ \frac{V_i - V_C}{L} t + I_{LP} & \text{state 2} \end{cases} \quad (21)$$

The voltage stress across the S is equal to $V_C - V_i$. Also, the current passing through the dc link i_{dc} would have two values, according to (21). If the inverter is in state 1, its value would be equal to the value of the current passing through the load i_{Lf}, and if the inverter is in state 2 of the nST mode, the open circuit state would occur.

The steady-state voltage waveforms of the converter for two operating modes ST and nST are indicated in Fig. 2. When $G_S = 1$, the switch S will be switched on and the inverter will operate in ST interval, otherwise, it will be in nST interval. In the steady state, the average voltage across the inductors in a switching cycle is equal to zero. In other words:

$$\frac{1}{T_s} \int_0^{T_s} v_L dt = \left(\int_0^{T_{ST}} v_L dt + \int_0^{T_{nST}} v_L dt \right) = 0 \quad (22)$$

By replacing v_L from (2) and (13) in (22), the derived equation is given by:

$$\int_0^{T_{ST}} V_C dt + \int_0^{T_{nST}} (V_i - V_C) dt = 0 \quad (23)$$

The voltage across the capacitor by replacing (1) in (23) and considering $T_{ST} + T_{nST} = T_s$ can be obtained as:

$$V_C = \frac{1 - D_{ST}}{1 - 2D_{ST}} V_i \quad (24)$$

The average voltage of the dc link (V_{dc}) using (10), (19) and (1) is computed by:

$$V_{dc} = \frac{1}{T_s} \left(\int_0^{T_{ST}} 0 \, dt + \int_0^{T_{nST}} V_C \, dt \right) = (1 - D_{ST}) V_C \quad (25)$$

The boost factor of SBI can be written as:

$$B = \frac{v_{dc,\max}}{V_i} \quad (26)$$

According to the value of $v_{dc,max}$ from Fig. 2 and the (24), the SBI boost factor is calculated by:

$$B = \frac{V_C}{V_i} = \frac{1 - D_{ST}}{1 - 2D_{ST}} \quad (27)$$

The curve V_c/V_i versus DST is illustrated in Fig. 3. When $D_{ST}=1$, V_c/V_i is equivalent to 1, also if D_{ST} is close to 0.5, its value becomes much higher. It is important to emphasize that similar to the ZSI, the duty cycle of the ST mode of the SBI cannot exceed 0.5. The expression for the conversion ratios V_c/V_i of SBI is similar to ZSI, according to relationships (25) and (27) . SBI average dc link voltage is (1-D) times that of ZSI [1].

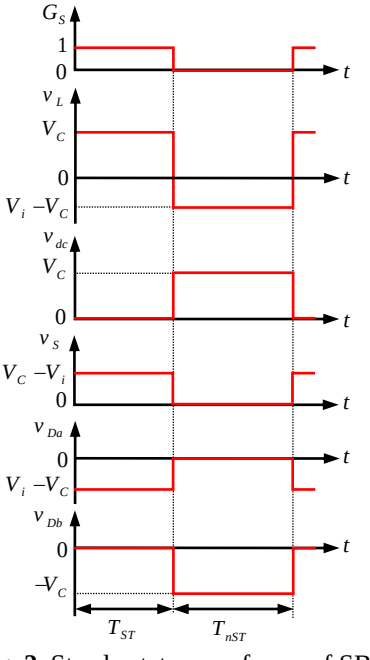


Fig. 2. Steady state waveforms of SBI.

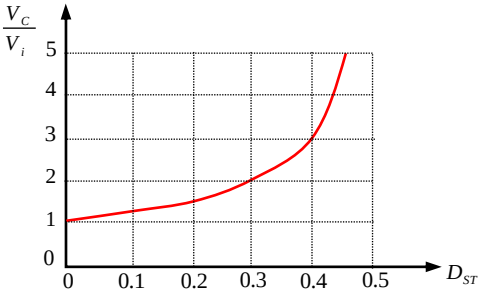


Fig. 3. Transfer characteristics of SBI.

3. PROPOSED PWM TECHNIQUES FOR SBI

SBI uses ST interval to increase the source voltage (V_i), while the conventional PWM technique of VSI prohibits the inverter bridge from being in ST interval. In the following, three different control methods based

on PWM technique are presented for this inverter. The voltage and current ripple of the inverter component are fully described in each switching technique due to their dependence on the type of switching method.

A. The First PWM technique

The gate control signals using the first PWM method for SBI are presented in Fig. 4. G_S, G_1, G_2, G_3 and G_4 are the gate control signals of the switches S, S_1, S_2, S_3 and S_4, respectively. In this method, gate control signals G_x (x=1 to 4) are produced by juxtaposing the reference signals Ref_{SX} (x = 1 to 4) to a triangular carrier signal $v_{tri}(t)$ of amplitude V_p. The gate control signal (G_S) for the switch S is achieved by summing up shoot-through periods ST_1 and ST_2. There are four ST states in this method for each period. Therefore, the switch will be switched on and off four times in each switching period, which leads to higher switching losses. The output frequency of the inverter (f_o) is also selected to be $f_s >> f_o$. The following relationships must be established:

$$Ref_1 = -Ref_4 \tag{28}$$

$$Ref_2 = -Ref_3 \tag{29}$$

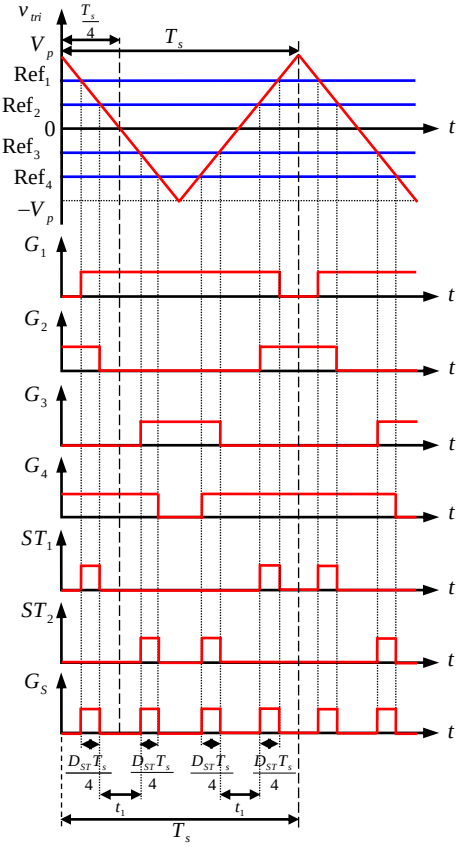


Fig. 4. Control signal generation for SBI using the first PWM technique.

According to Fig. 4, the signals (G_1-G_4) in the first PWM control technique when the output voltage of the inverter is positive, the ensuing relationships are derived:

If $Ref_1 > v_{tri}(t)$ then $G_1 = 1$;
If $Ref_2 < v_{tri}(t)$ then $G_2 = 1$;
If $Ref_3 > v_{tri}(t)$ then $G_3 = 1$;
If $Ref_4 < v_{tri}(t)$ then $G_4 = 1$.

To generate the negative output voltage of the inverter, the way the switches turn on must be changed as follows:

If $Ref_1 > v_{tri}(t)$ then $G_3 = 1$;
If $Ref_2 < v_{tri}(t)$ then $G_4 = 1$;
If $Ref_3 > v_{tri}(t)$ then $G_1 = 1$;
If $Ref_4 < v_{tri}(t)$ then $G_2 = 1$.

So:

$$\begin{cases} ST_1 = G_1 \wedge G_2 \\ ST_2 = G_3 \wedge G_4 \\ G_S = ST_1 \vee ST_2 \end{cases} \tag{30,31,32}$$

"$\wedge$" and "$\vee$" represent logical AND and OR, respectively.

Mathematical relationship between Ref_1 ***and*** Ref_2 ***with duty cycle*** D_{ST}

Slope of line (a) in the time span of $0 \le t < \frac{T_s}{4}$ can be written based on the similarity law of triangles as shown in Fig. 4:

$$\frac{Ref_1 - Ref_2}{\frac{D_{ST}T_s}{4}} = \frac{V_p}{\frac{T_s}{4}} \tag{33}$$

By simplifying (33) can be written as follows:

$$D_{ST} = \frac{Ref_1 - Ref_2}{V_P} \tag{34}$$

Effect of the ST state on the output voltage (v_{o1})

According to Fig. 4, during the t_1 interval, the power is transferred to the load and the positive and negative voltages are generated across the inverter by

switches (s_1-s_2) and (s_3-s_4), respectively. This time interval can be calculated by the law of similarity of triangles as follows:

$$\frac{Ref_2 - Ref_3}{t_1} = \frac{V_p}{\frac{T_s}{4}} \quad (35)$$

By replacing (29) in (35), the following equation can be written:

$$t_1 = \frac{Ref_2 T_s}{2V_P} \quad (36)$$

To make certain the ST time interval is not more than the inverter power transmission time and does not interfere with the power v_{o1} time intervals, it should be selected so that the absolute width of the ST time interval is not more than the absolute width attainable from the zero distance in each period, in another word:

$$D_{ST}T_s < T_s - \frac{(Ref_2)T_s}{V_p} \quad (37)$$

By simplifying (37), we have

$$D_{ST} < 1 - \frac{Ref_2}{V_p} \quad (38)$$

In above relationship $M = \frac{Ref_2}{V_p}$

By replacing (34) in (38), the ensuing expression is derived:

$$Ref_1 < V_p \quad (39)$$

The current and voltage waveforms of SBI components, when the output voltage of the inverter is positive are shown in Fig. 5.

The maximum current ripple of the inductor L is in t_1 interval. By considering (14), the ensuing equation can be computed:

$$i_L|_{t=t_1} = I_{LV1} = \frac{V_i - V_C}{L} t_1 + I_{LP1} \quad (40)$$

The value of the ripple current of the inductor is derived by:

$$I_{L,PP} = I_{LP1} - I_{LV1} = \frac{D_{ST}V_i}{2(1-2D_{ST})Lf_s} \frac{Ref_2}{V_P} \quad (41)$$

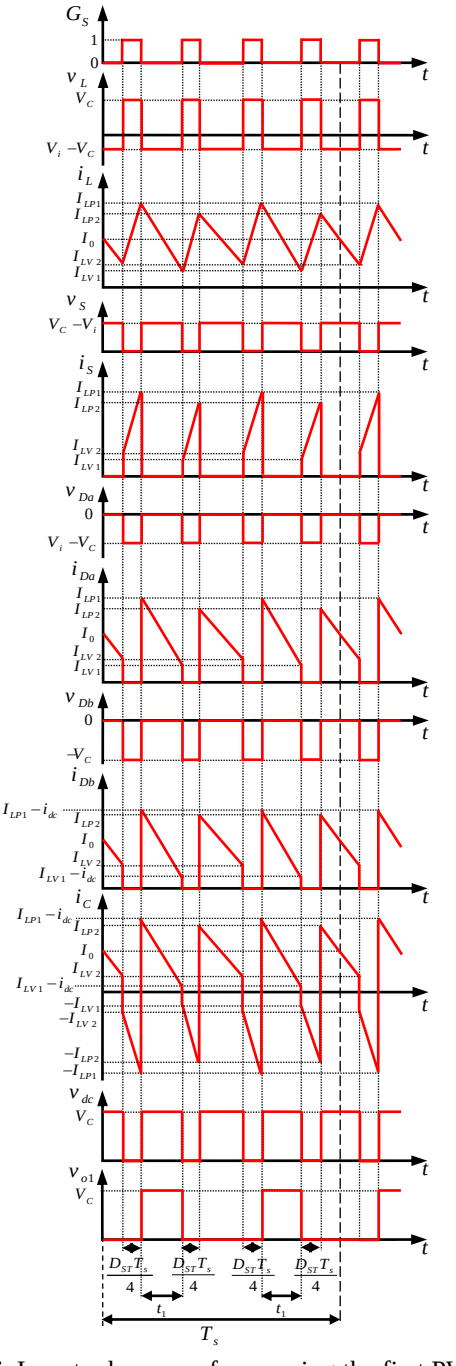


Fig. 5. Inverter key waveforms using the first PWM method

B. The Second PWM technique

This subsection presents a modified PWM switching technique for SBI founded on conventional sine-triangle PWM having unipolar voltage switching. Each switching period of switch (S) contains only two switching sequences in each T_s with a constant switching frequency. The general scheme of the control diagram to create the PWM control signals for the converter employing the modified PWM control is

presented in Fig. 6. The control signals created for the positive half cycle of v_m for T_S are illustrated in Fig. 7(d). According to Fig. 7(d), by juxtaposing the sinusoidal modulation signals $v_m(t)$ and $-v_m(t)$ with a high-frequency triangular carrier $v_{tri}(t)$ with amplitude V_p, the gate control signals for switches S_1 and S_2 are created. The frequency (f_S) of the carrier signal is selected such that $f_s >> f_o$. Hence, v_m is considered to be almost constant during T_S according to Fig. 7(d).

Signals ST_1 and ST_2 are produced by juxtaposing $v_{tri}(t)$ to two fixed voltages V_{ST} and $-V_{ST}$, accordingly. The two signals enter the desired shoot-through time in the D_{ST} interval in the gate control signals of the inverter. In this case, the gate control signals for S_4, S_5, and S are derived from the given logical expressions:

If $V_{ST} > v_{tri}(t)$ then $ST_1 = 1$;

If $-V_{ST} < v_{tri}(t)$ then $ST_2 = 1$;

If $v_m(t) > v_{tri}(t)$ then $G_1 = 1$;

If $-v_m(t) < v_{tri}(t)$ then $G_4 = 1$.

So

$$G_2 = \overline{G_1 \wedge ST_2} \quad (42)$$

$$G_3 = \overline{G_4 \wedge ST_1} \quad (43)$$

$$G_S = \overline{ST_1 \wedge ST_2} \quad (44)$$

In above relationship, "$\bar{}$" indicates logical NOT.

The voltage waveform at the input (V_{dc}) and output (v_{o1}) of the inverter bridge is presented in Fig. 7(d). There are nine time intervals for v_{o1} in each switching cycle. The conducting components for every of these time intervals are listed in Table 1.

Table 1. Conducting components in each time interval.

On Switches	Time interval number
S, S_1, S_3, S_4	1, 9
S_2, S_4	2, 8
S_1, S_2 (S_3, S_4 in negative half-cycle of $v_{in}(t)$)	3, 7
S_1, S_3	4, 6
S, S_1, S_3, S_4	5

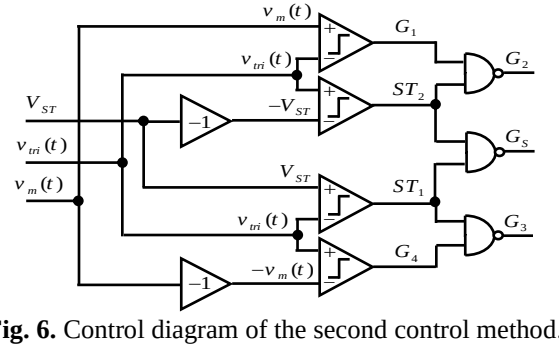


Fig. 6. Control diagram of the second control method.

Mathematical Relation between V_{ST} and D_{ST}

D_{ST} can be changed with different V_{ST}s, as indicated by Fig. 7(c). The slope of the triangular carrier line (a) in $0 \le t < \frac{T_s}{2}$ interval is computed by:

$$a = \frac{-V_p - V_p}{\frac{T_s}{2}} = \frac{-V_p}{\frac{T_s}{4}} \quad (45)$$

By placing (45) in the equation of the line and also using the coordinates $\left| \begin{matrix} t = 0 \\ v_{tri}(t) = V_P \end{matrix} \right.$, the ensuing equation can be written:

$$v_{tri}(t) - V_p = a(t-0) = \frac{-V_p}{\frac{T_s}{4}} t \quad (46)$$

Simplifying the above relationship, for the $0 \le t < \frac{T_s}{2}$ $v_{tri}(t)$, the subsequent equation is derived:

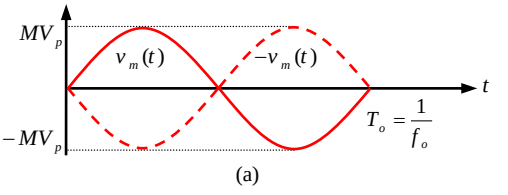
$$v_{tri}(t) = \left(\frac{-V_p}{\frac{T_s}{4}} \right) \left(t - \frac{T_s}{4} \right) \quad (47)$$

The slope line of the triangular carrier from Fig. 6(c) in $\frac{T_s}{2} \le t < T_s$ is computed by:

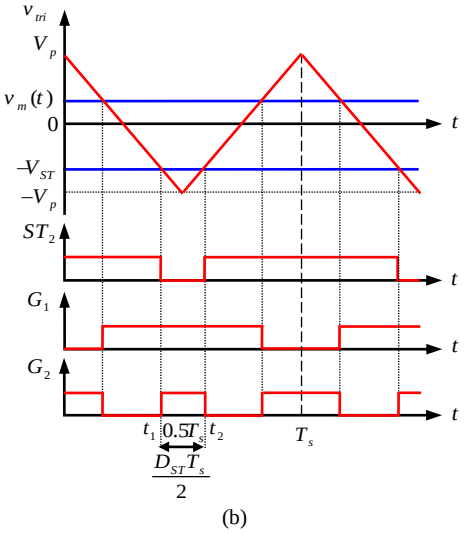
$$a = \frac{V_p - (-V_p)}{\frac{T_s}{2}} = \frac{V_p}{\frac{T_s}{4}} \quad (48)$$

By placing the above relationship in the equation of the line and also considering the coordinates $\left| \begin{matrix} t = T_s \\ v_{tri}(t) = V_P \end{matrix} \right.$, we can write:

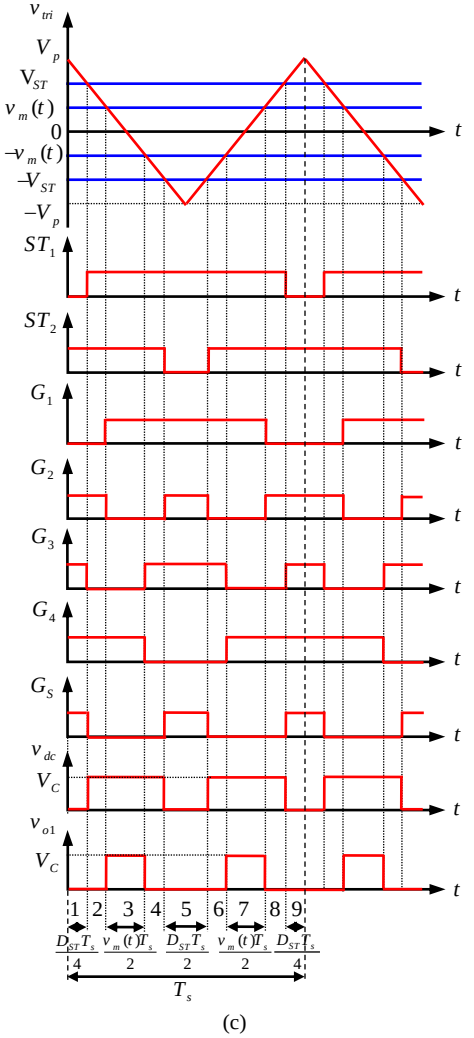
$$v_{tri}(t) - V_p = a(t - T_s) = \frac{V_p}{\frac{T_s}{4}} t - 4V_p \quad (49)$$



(a)



(b)



(c)

Fig. 7. Second control method; (a) sinusoidal modulation of $v_m(t)$ and - $v_m(t)$ signals; (b) ST state in S_1 and S_2; (c) control signals in positive half cycle of switching cycle $v_m(t)$.

By simplifying (49), $v_{tri}(t)$ in $\frac{T_s}{2} \le t < T_s$ time interval is obtained as follows:

$$v_{tri}(t) = \left(\frac{V_p}{\frac{T_s}{4}}\right)\left(t - \frac{3T_s}{4}\right) \tag{50}$$

From (47) and (50), the ensuing equations are provided:

$$v_{tri}(t) = \begin{cases} \left(\frac{-V_p}{\frac{T_s}{4}}\right)\left(t - \frac{T_s}{4}\right) & for \;\; 0 \le t < \frac{T_s}{2} \\ \left(\frac{V_p}{\frac{T_s}{4}}\right)\left(t - \frac{3T_s}{4}\right) & for \;\; \frac{T_s}{2} \le t < T_s \end{cases} \tag{51}$$

So

$$v_{tri}(t_1) = -V_{ST} \tag{52}$$

$$v_{tri}(t_2) = -V_{ST} \tag{53}$$

$$v_{tri}(t_1) = v_{tri}(t_2) \tag{54}$$

$$t_2 - t_1 = \frac{D_{ST}T_s}{2} \tag{55}$$

By replacing (52) in (51), the following relationship can be calculated:

$$-V_{ST} = \left(\frac{-V_p}{\frac{T_s}{4}}\right)\left(t_1 - \frac{T_s}{4}\right) \tag{56}$$

By simplifying (58), the expressions for t_1 can be obtained as:

$$t_1 = \frac{T_s}{4}\left(1 + \frac{V_{ST}}{V_p}\right) \tag{57}$$

In the same way, by substituting the relation (53) in the relation (51) in $\frac{T_s}{2} \le t < T_s$, the ensuing equation is given as:

$$-V_{ST} = \left(\frac{V_p}{\frac{T_s}{4}}\right)\left(t_2 - \frac{3T_s}{4}\right) \tag{58}$$

The expressions for t_2 by simplifying (59) can be obtained as:

$$t_2 = \frac{T_s}{4}\left(3 - \frac{V_{ST}}{V_p}\right) \tag{59}$$

By replacing t_1 and t_2 from (57) and (59) in (55), the following equation can be obtained:

$$\frac{D_{ST}\,T_s}{2} = \frac{T_s}{4}\left(3 - \frac{V_{ST}}{V_p}\right) - \frac{T_s}{4}\left(1 + \frac{V_{ST}}{V_p}\right) \tag{60}$$

So, D_{ST} is derived as:

$$D_{ST} = \frac{4T_s}{4T_s} - \frac{4T_s V_{ST}}{4T_s V_p} \tag{61}$$

Finally, by considering (61), D_{ST} can be calculated as:

$$D_{ST} = 1 - \frac{V_{ST}}{V_p} \tag{62}$$

Effect of ST State on Output Voltage (v_{o1})

The source voltage (v_{dc}) waveform and the output voltage (v_{o1}) across the inverter bridge are illustrated in Fig. 6(d). The voltage v_{o1} has three-time intervals of zero (when $v_{o1} = 0$) and two time intervals of power transfer (when $v_{o1} = V_C$) in individual switching cycle. To make certain that the ST time interval is not more than the inverter power transfer time period, and does not interfere with the power v_{o1} time intervals, it ought to be chosen so that the absolute width of the ST time interval will not surpass the absolute attainable width from the zero distance in each switching cycle.
So,

$$D_{ST}T_s < T_s - \max\left(\frac{v_m(t)T_s}{V_p}\right) \tag{63}$$

By simplifying (63), the subsequent equation is derived:

$$D_{ST} < 1 - M_{\max} \tag{64}$$

where $M_{\max} = \max\left(\frac{v_m(t)}{V_p}\right)$ indicates the maximum modulation index.
By replacing D_{ST} from (62) in (64), we have:

$$1 - \frac{V_{ST}}{V_p} < 1 - M_{\max} \tag{65}$$

By simplifying (65), the ensuing equation is provided:

$$V_{ST} > M_{\max} V_p \tag{66}$$

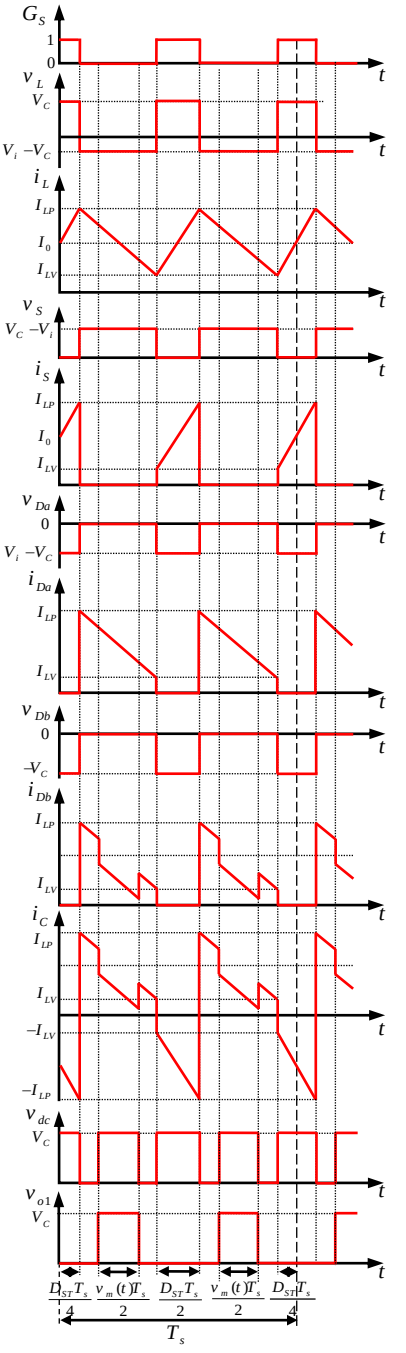


Fig. 8. Inverter key waveforms using second PWM method.

The harmonic spectrum of v_{o1} is equivalent to that of VSI with the conventional sine-triangle PWM, with unipolar voltage switching v_{o1} given by:

$$(V_{o1,\max})_{fundamental} = V_{o2,\max} = M_{\max} V_C = M_{\max}\left(\frac{1-D_{ST}}{1-2D_{ST}}\right)V_i \quad (67)$$

The current and voltage waveforms of SBI components using this switching method are shown in Fig. 8. In Fig. 8 and according to Fig. 7(d), the current and voltage waveforms are presented for the positive half of the period $v_m(t)$. According to the relationships (63) and (64), the modulation index is a function of time $\left(M = v_m(t)/V_p\right)$. So, the waveforms i_{Db}, i_C, and v_{o1} alternately change in each switching cycle $T_o = 1/f_o$. In Fig. 8, the waveforms are drawn for an arbitrary switching cycle. According to Fig. 8 and the value of relationship (14), the ensuing equation is written by:

$$i_L\Big|_{t=\frac{D_{ST}T_s}{2}} = I_{LP} = \frac{V_C}{L}\frac{D_{ST}T_s}{2} + I_{LV} \quad (68)$$

By replacing V_C in (24,) the inductor current ripple is computed by:

$$I_{L,PP} = I_{LP} - I_{LV} = \frac{D_{ST}(1-D_{ST})V_i}{2(1-2D_{ST})Lf_s} \quad (69)$$

C. The Third PWM technique

The switching method presented in this subsection is a high frequency switching method. The general design of the control circuit for generating PWM control signals is shown in Fig. 9, which can generate ST states by using two short-circuit signals V_{ST1} and V_{ST2} and a high-frequency triangular signal. Additionally, in Fig. 10, the waveforms of ST signal for switching cycle are presented. Relating to Fig. 10, two triangular $(v_{tri}(t))$ and sine $(v_m(t))$ signals that have frequencies f_s are juxtaposed to each other. The value of the amplitude of $v_m(t)$ is $|1|^{P.U.}$ and it has minimum and maximum values $0^{P.U.}$ and $1^{P.U.}$, respectively. V_{ST1} and V_{ST2} have $0Hz$ can be obtained by

$$V_{ST1} = D_{ST} \quad (70)$$

$$V_{ST2} = 1 - D_{ST} \quad (71)$$

If $V_{ST1} > v_{tri}(t)$ then $h_1 = 1$

If $V_{ST2} < v_{tri}(t)$ then $h_2 = 1$

In order to produce ST signals (ST_1 and ST_2), a step signal (u) with a frequency of (f_s) is required, which is obtained from the comparison of $v_m(t)$ with zero value. The signals ST_1 and ST_2 are obtained as:

$$ST_1 = h_1 \wedge u' \quad (72)$$

$$ST_2 = h_2 \wedge u \quad (73)$$

The symbol "$\wedge$" indicates logical AND.

According to Figs. 9 and 10 as well as the above relationships, the gate signals of the switches are obtained by:

$$G_{S1} = G_{S4} = u \vee ST_1 \quad (74)$$

$$G_{S2} = G_{S3} = u' \vee ST_2 \quad (75)$$

$$G_S = ST_1 \wedge ST_2 \quad (76)$$

The symbol "$\vee$"indicates logical OR.

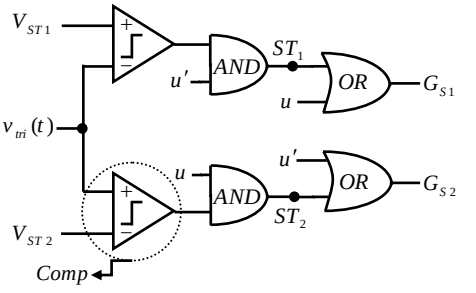


Fig. 9. PWM signal generation circuit in third control method.

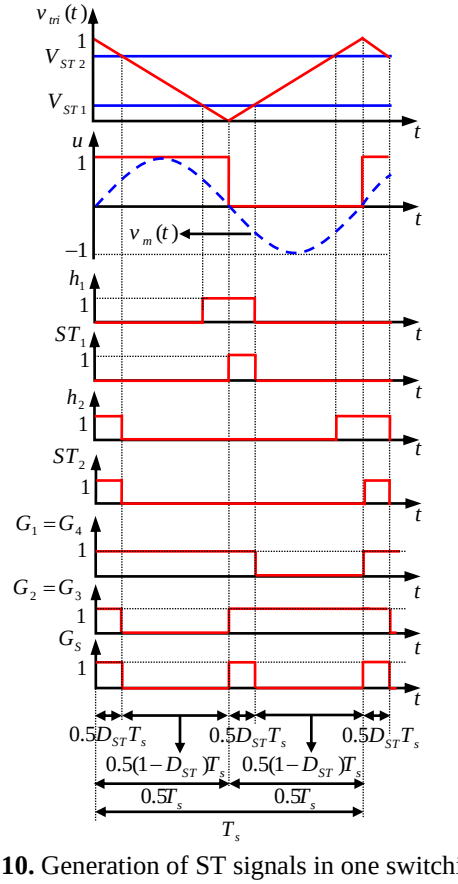


Fig. 10. Generation of ST signals in one switching cycle in the third method.

The steady state waveforms of components in one switching cycle using the third control method are presented in Fig. 11. Considering (4) in ST operation mode, the peak magnitude of inductor current is obtained as:

$$i_L\big|_{t=0.5D_{ST}T_s} = I_{LP} = \frac{V_C}{2L} D_{ST} T_s + I_{LV} \tag{77}$$

The dc-link voltage and capacitor current values are calculated as follows for the resistive load.

$$i_{dc} = I_{o,\max} \tag{78}$$

$$i_C = i_{D2} = i_L - i_{dc} = \frac{V_i - V_C}{L} t + \left(I_{LP} - I_{o,\max}\right) \tag{79}$$

$I_{o,\max}$ is the maximum current of the load which is equivalent to the dc-link current in the nST operation mode. The peak magnitude of the current load is expressed by:

$$I_{o,\max} = \frac{v_{o1,\max}}{R} = \frac{V_C}{R} \tag{80}$$

According to the capacitor current balance law, the mean current passing through the capacitors in a switching period is equal to zero and is expressed as:

$$\frac{1}{T_s}\int_0^{T_s} i_C\, dt = \frac{2}{T_s}\int_0^{0.5T_s} i_C\, dt = 0 \tag{81}$$

By replacing i_C from (12) and (79) in (81), the resulting equation is expressed by:

$$\int_0^{0.5D_{ST}T_s} \left(-\frac{V_C}{L} t - I_{LV}\right) dt + \int_0^{0.5(1-D_{ST})T_s} \left[\left(\frac{V_i - V_C}{L}\right) t + \left(I_{LP} - I_{o,\max}\right)\right] dt = 0 \tag{82}$$

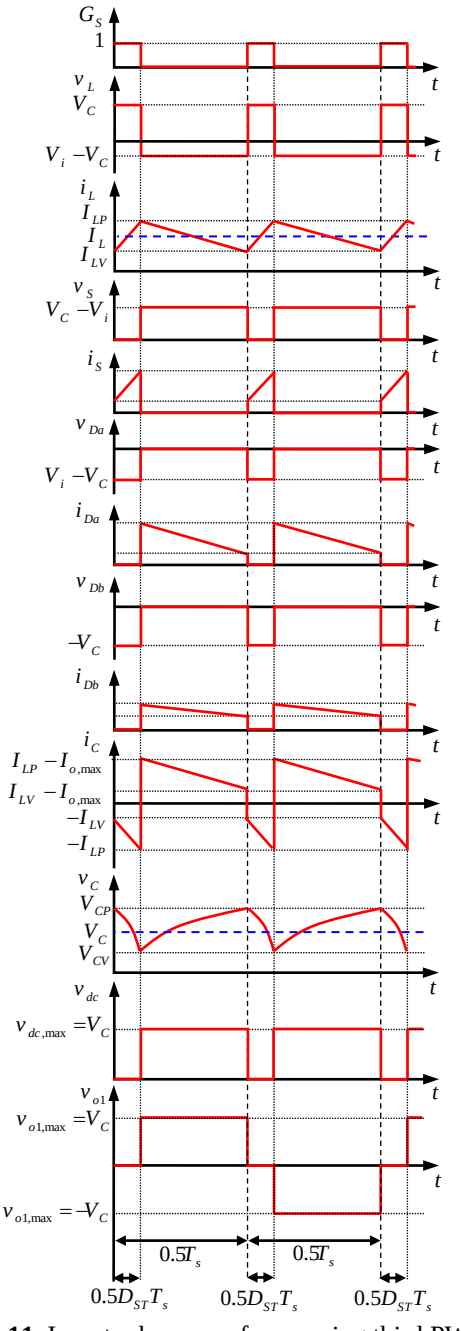


Fig. 11. Inverter key waveforms using third PWM method.

By simplifying (82) and considering (77) and (80), the result is:

$$\frac{V_C D_{ST}^{\ 2}}{4Lf_s} + \frac{(V_i - V_C)(1-D_{ST})^2}{4Lf_s} + I_{LP}(1-2D_{ST}) - \frac{V_C(1-D_{ST})}{R} = 0 \tag{83}$$

By replacing (24) in (83), the resulting equation is expressed by:

$$I_{LP} = \frac{V_i(1-D_{ST})}{1-2D_{ST}}\left(\frac{1-D_{ST}}{R(1-2D_{ST})}+\frac{D_{ST}}{4Lf_s}\right) \quad (84)$$

By replacing (84) in (77), I_{LV} is as follows:

$$I_{LV} = \frac{V_i(1-D_{ST})}{(1-2D_{ST})}\left(\frac{1-D_{ST}}{R(1-2D_{ST})}-\frac{D_{ST}}{4Lf_s}\right) \quad (85)$$

Calculation of the value of the inductor in the boundary condition

The performance of SBI depends on the change in the inductor value. Therefore, calculating the minimum value of the inductor is necessary to operate in the desired state. The diodes D_a and D_b have Synchronous Operation (SOD) and turn on and off together if the SBI components and other parameters such as switching frequency and duty cycle have appropriate values. Otherwise, there may be a situation where the diodes turn on and off as an Asynchronous Operation (AOD). According to Fig. 11, $I_{LV} = I_{o,\max}$ in the boundary state. So by considering (80) and (85), the value of the inductor L_c in the boundary state between AOD and SOD performance is calculated as follows:

$$L_C = \frac{R(1-2D_{ST})}{4f_s} \quad (86)$$

According to the above relationship, it is clear that by maximizing the magnitude of R and minimizing the magnitudes of D_{ST} and f_s, the value of boundary inductor is increased. Also, for certain values of R, D_{ST} and f_s, if $L > L_C$ is selected, the inverter operates in SOD operation and if $L < L_C$ then the inverter will operate in AOD operation.

Calculation of inductor current ripple and capacitor voltage ripple in SOD operation

The value of current and voltage ripples of the inductor and capacitor accordingly are among the dominant criteria in power electronic converter design. Also, an increase in current and voltage ripple values can lead to an increase in stress on the converter components and disrupt its proper operation. According to Fig. 11, the current ripple passing through the inductor is obtained from the difference between the upper and lower limits of the inductor current. Therefore, according to (84) and (85), we can write:

$$I_{LPP}^{SOD} = I_{LP} - I_{LV} = \frac{V_i D_{ST}(1-D_{ST})}{2Lf_s(1-2D_{ST})} \quad (87)$$

It is evident that the inductor current ripple has an inverse relationship with the inductor value., when the value of the inductor increases, the ripple decreases, and vice versa. Under these conditions, the peak magnitude of the inductor current ripple will occur in $L = L_C$. By substituting L_C from (86) into (87), the peak magnitude inductor current ripple value in SOD operation is obtained as:

$$I_{LPP,\max}^{SOD} = \frac{2V_i D_{ST}(1-D_{ST})}{R(1-2D_{ST})^2} \quad (88)$$

The voltage ripple across the capacitor in this operation can be obtained by integrating the current passing through capacitor in $0 \le t \le 0.5D_{ST}T_s$ time interval as follows:

$$V_{C,PP}^{SOD} = V_{CP} - V_{CV} = -\frac{1}{C}\int_0^{0.5D_{ST}T_s} i_C(t)dt \quad (89)$$

By replacing (12) into (89) and considering (24) and (85), the voltage ripple across the capacitor in SOD operation is computed by:

$$V_{C,PP}^{SOD} = \frac{V_i D_{ST}(1-D_{ST})^2}{2f_s RC(1-2D_{ST})^2} \quad (90)$$

It can be seen that the voltage ripple of the capacitor is not dependent on the changes in the magnitude of the inductor.

4. SIMULATION RESULTS

To prove the accuracy of the presented control methods, the SBI is simulated in PSCAD/EMTDC software. The used parameters in the simulation are presented in Table 2.

Table 2. Used parameters in the simulation.

parameters	values
(V_i)	$20V$
(f_o)	$50\,Hz$
(f_s)	$5\,kHz$
(D_{ST})	0.4
$(M_{\max})$	0.5
(L)	$5.6\,mH$
(C)	$470\,\mu F$
(L_f)	$4\,mH$
(C_f)	$10\,\mu F$
(R)	$25\,\Omega$

A. Simulation results for first control method

The generation of switching signals using the first control method for a switching cycle is shown in Fig. 11. There are four reference signals

($Ref_1, Ref_2, Ref_3, Ref_4$) that produce switching signals of S_1 and S_2 compared to the triangular carrier $v_{tri}(t)$. The switches in each leg of the inverter are logically added together to produce an ST state which is obtained through relations (30)-(32). There are four ST time intervals in one switching cycle with the same time intervals equal to each other, as shown in Fig 12. The amplitude of the triangular carrier is equal to $V_p = 1$. Therefore, according to the mentioned statements and from the relationship (34), the values of signals Ref_1 and Ref_2 should be selected so that $Ref_1 - Ref_2 = 0.4$. Also, according to Table 2, $Ref_2 / V_p = Ref_2 = M = 0.5$, this value guarantees the relation (38) ($D_{ST} < 1 - Ref_2$). So, the values of the reference signals are chosen $Ref_1 = 0.9$, and $Ref_2 = 0.5$, respectively. Fig. 13 shows the results of steady-state voltage and current waveforms. Fig. 13(a) depicts the voltage across and current flowing through inductor *L*. As it is clear in the ST state, the voltage across the inductor V_L is equal to 60V, which is equivalent to the voltage across the capacitor V_C as shown in Fig. 13(e). Also, V_L in the nST state is almost equal to -40*V*, which confirms the correctness of the relationship (13). The current passing through inductor i_L increases and decreases linearly in the ST and nST states, respectively. According to (41), the peak magnitude of the current ripple is 0.35*A*, which is also the same value in Fig. 13(a). Fig. 13(b) illustrates the current and voltage waveforms of the switch. In ST state, the switch is on and V_S is zero, but in nST state, the *S* is turned off, and $V_S = V_C$. The current and voltage waveforms of D_a and D_b which are off in ST state and on in nST state are presented in Fig. 13(c) and 13(d). In the nST state, the i_{Da} is always equal to i_L, while i_{Db} is less than i_L during the time that power transfers, which (21) and Fig. 13(d) confirm its correctness. V_{Da} according to (7) and (8) are equal to -40V and -60V respectively, which also have the same value in Figs. 13(c) and 13(d), as well as the voltage and current of the dc-link are expressed in Fig. 13(e). The dc-link voltage is zero in ST state and is the same as V_{C1} in the nST state. In ST state, i_C and i_{DC} have the same value, but in the opposite directions. While i_{DC} is equal to zero, i_C will be equal to i_L in nST mode.

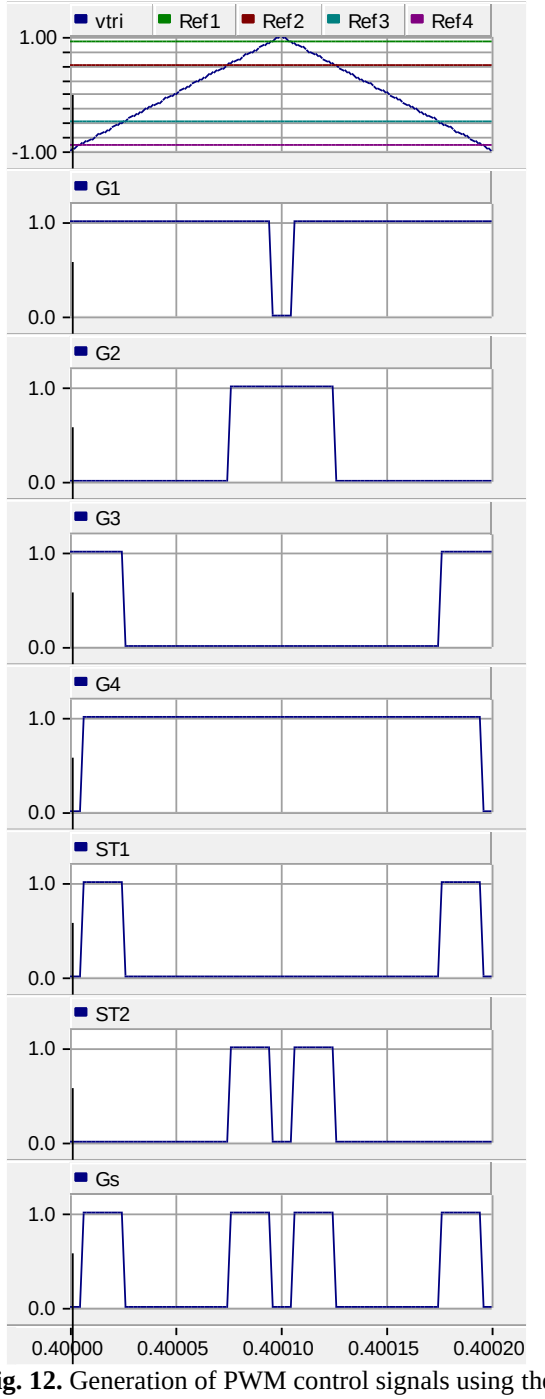


Fig. 12. Generation of PWM control signals using the first control method.

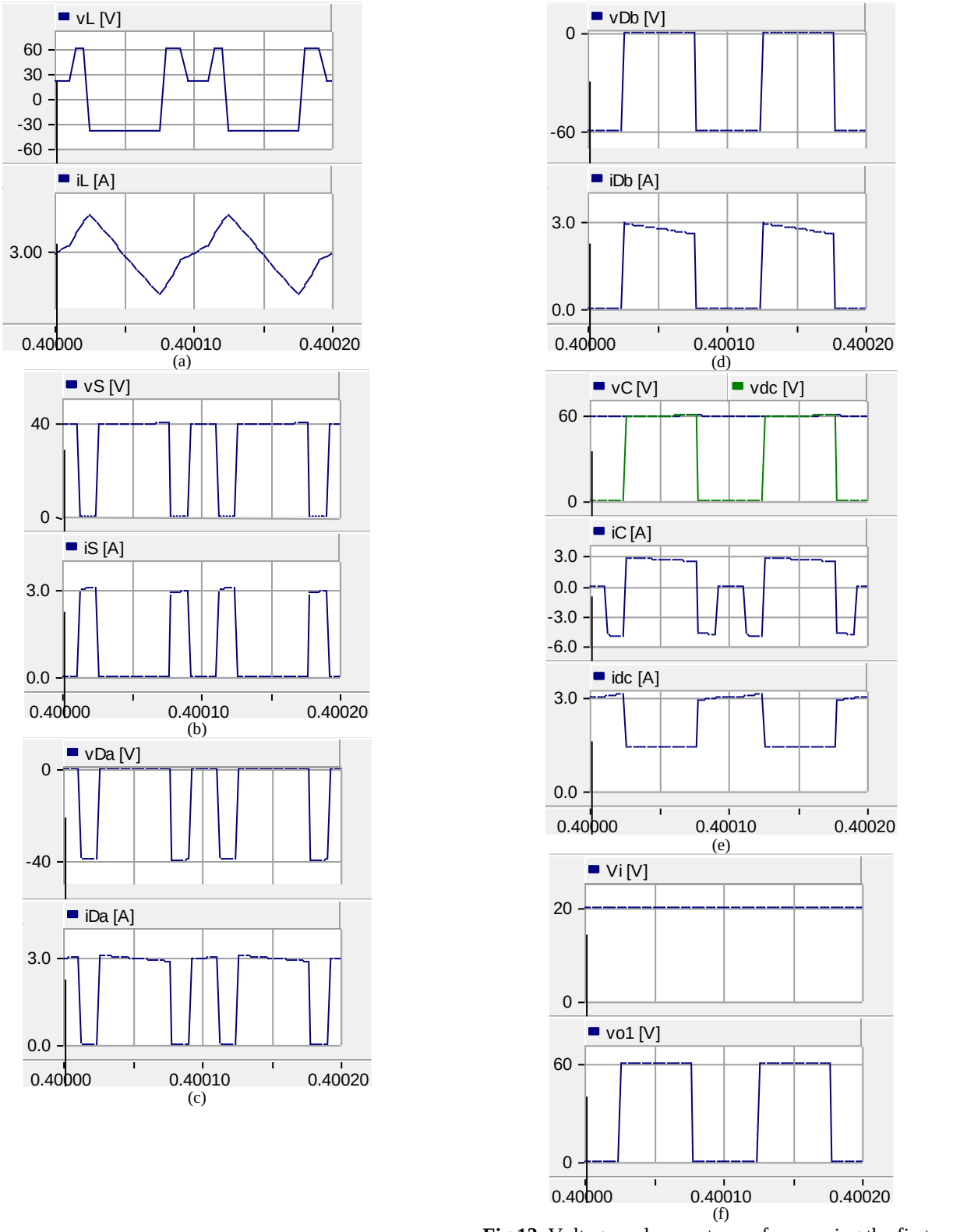


Fig 13. Voltage and current waveforms using the first control method; (a) voltage and current of L; (b) voltage and current of S; (c) voltage and current of D_a; (d) voltage and current of D_b; (e) voltage and current of C and dc-link; (f) input and output voltage of inverter.

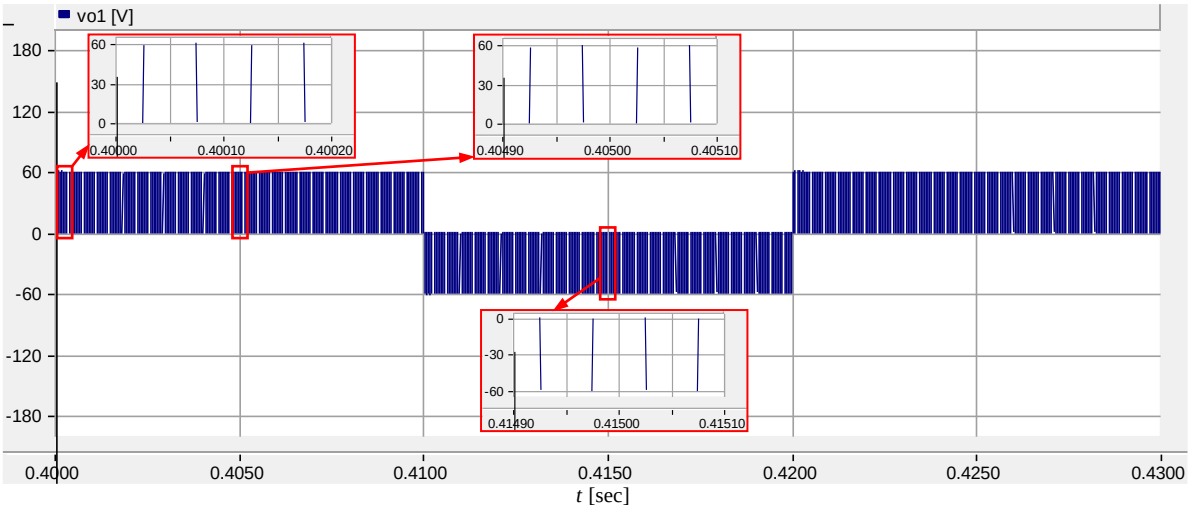


Fig. 14. Inverter output voltage waveform using first control method for one output period (T_o).

The voltage and current waveforms of the capacitor as the input voltage waveform and the output voltage waveform of the inverter are presented in 13(f). The maximum and minimum output voltage of the inverter is equivalent to the maximum magnitude of the dc-link voltage and it alternates with a much lower frequency than the switching frequency. Fig. 14 depicts the output voltage waveform of the inverter for a switching cycle of T_o. The modulation index is constant in this switching method, so the power transmission interval will always be constant in this state. The output voltage waveform of the inverter is presented for several arbitrary switching cycles of T_s, in all three cases, the power transmission interval is constant and the amplitude of the waveform is equal to $\pm 60V$.

B. Simulation results for the second control method

The gate signals in the second control method are illustrated in Fig. 15, which corresponds to the waveforms of Fig. 7. In this method, sinusoidal modulation is used, by juxtaposing $v_m(t)$ and $-v_m(t)$ with $v_{tri}(t)$, the signals related to the switches S_1 and S_4 are obtained. Also, in this method, unlike the previous method, the ST signals are not dependent on the switches signals, and ST states are achieved directly by using two V_{ST} and $-V_{ST}$ waves. The gate signals of the other two switches of the inverter are obtained by using the logical combination of the signal G_1, G_4, ST_1 and ST_2 which have already been mentioned in (42) and (43). According to Fig. 15, the value of the amplitude of the triangular carrier (V_p) in this switching method is considered to be $1pu$.

It should be $|V_{ST}| = 0.6$ according to (62). Also, for the peak magnitude of the modulation index to be 0.5, the value of the amplitude $v_m(t)$ should be equal to 0.5. The simulation results by employing the second control method are presented in Fig. 16. The modulation index in this method changes sinusoidally and does not have a constant value, therefore, in the nST state, the time interval of the power will be different. For this reason, the waveform of the dc-link current will also change with variation of the modulation index. Fig. 16(a) indicates the voltage and current waveforms of the inductor L. In reference to (2), in the ST state, it will be equivalent to the voltage across the capacitor C which is equivalent to $60V$ in Fig. 16(d). In the nST state, V_L is almost equal to $-40V$, which is in good agreement with (13). The current passing through L increases and decreases linearly in ST and nST modes, respectively. Also, according to (69), the inductor current ripple is equivalent to $0.43A$, and the current ripple extracted from Fig. 16(a) will be the same magnitude. The current and voltage of the switch S are presented in Fig. 16(b). As it is obvious, in ST mode, S is turned on and the voltage across of it, is zero and the current passing through it, is equal to i_L the nST mode, S is switched off and the current passing through it is zero. V_S in the nST state is also equal to 40V, which shows the correctness of (15). In this switching method, unlike the previous method, the on and off states of the switch are reduced. i_{Da} is shown in Fig. 16(c). It is off in the ST state and the i_{Da} is equal to zero, and it is on in the nST state and the i_{Da} is equal to i_L. V_{Db}, V_C, and V_{DC} are presented in Fig. 16(d). The voltage across the diode in the nST state is zero and equal to the voltage across the capacitor, which shows that the diode is on in the nST state. DC-link voltage is also zero in ST state due to the ST of the inverter leg, and in nST state it is equal to V_C, which shows the correctness of (19). According to (24) and the values of

Table 2, the average voltage across the capacitor is same as 60V, which is almost equivalent to the value obtained from Fig. 16(d). The current passing through the diode D_b and capacitor (C) is not shown in Fig. 15 because their values in nST state depend on the value of the dc-link current. The dc-link current in nST mode varies by changes in the magnitude of the modulation index, their waveforms cannot be assumed to be constant for a period of time, so the waveforms of the current passing through the diode and capacitor and the dc-link current are illustrated by Fig. 16, respectively. Fig. 16(a) shows the waveform of the current passing through the dc-link i_{dc} in several different intervals. According to Fig. 16(a) and (11), the value in ST state is equal to i_L and follows this value in all time intervals. In the nST state, according to Fig. 16(a), by the change of the modulation index, the value will be different in each switching cycle so that if the modulation index is at the peak magnitude, it will be zero in a shorter time period, but with the reduction of the modulation index value, the time interval will be zero. The power is reduced and i_{dc} will be zero for most of the time. Fig. 16(b) shows the waveform of the current passing through diode D_b the same as the dc-link current in multiple time intervals. In the ST mode, D_b is off, and the current passing through it is zero, but in the nST mode, the current passing through D_b is equal to under the condition that $i_{dc}=0$, otherwise it is obtained from the difference between i_L and i_{dc}, which is in a good agreement of (21). i_{Db} is equal to i_C in nST state as shown in Fig. 16(c). i_C is equal to $-i_L$ in ST state according to (12) and Fig. 16(c) confirming its correctness. Fig. 15(d) shows the waveform of the output voltage of the inverter before the filter. According to Fig. 16(d), it is clear that in the power transmission range, the maximum value of the inverter output voltage is equal to the maximum value of the dc-link voltage. Figs. 16(e) and 16(f) indicate the filter inductor voltage and current and the output load, respectively. In ST state, the voltage across inductor is same as $(-v_{o2})$. In the nST mode, if the power is transferred to the load, v_{Lf} will be equal to the $(v_{o1}-v_{o2})$ and if the dc-link current is zero, v_{Lf} will again be equal to $-v_{o2}$. The maximum value v_{o2} from (67) is equal to 30V, which is confirmed by Fig. 16(e). For better understanding, all the waveforms are shown in Fig. 17 for several different time intervals for one output period.

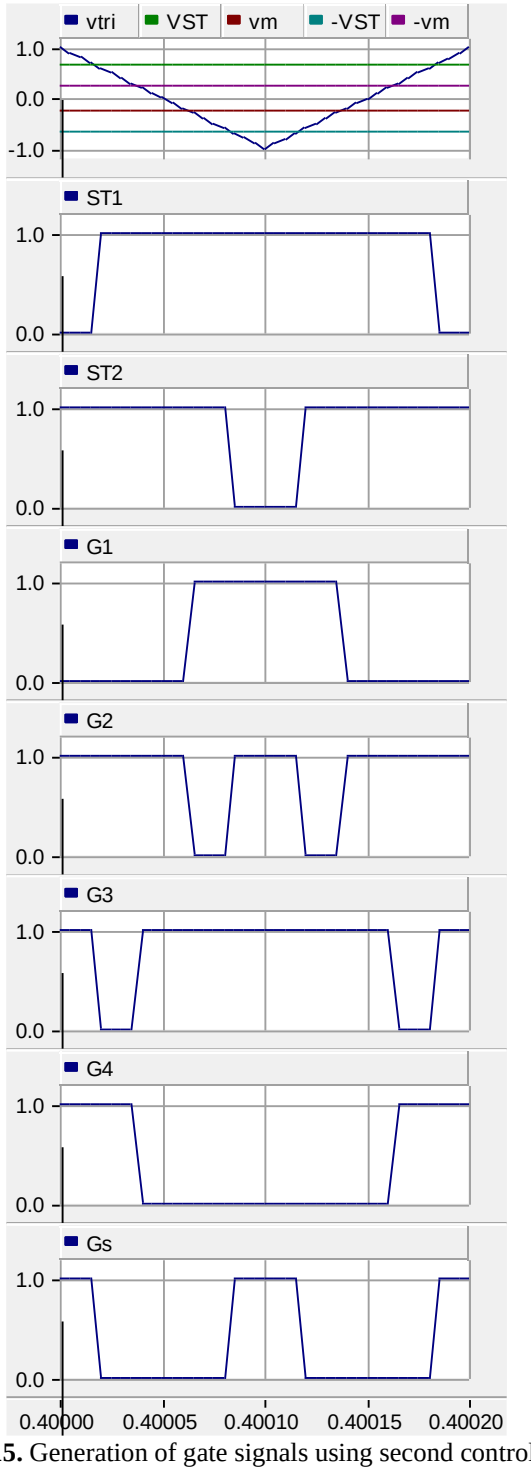
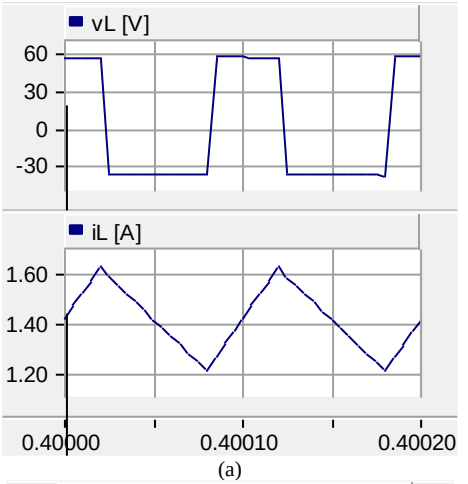
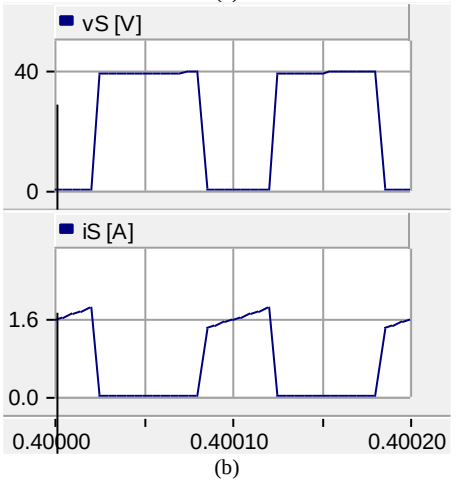


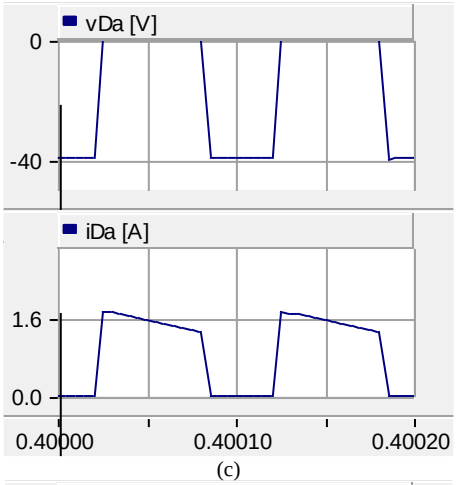
Fig. 15. Generation of gate signals using second control method.



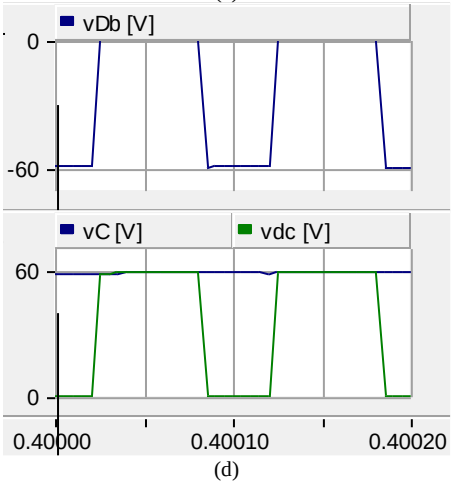
(a)



(b)

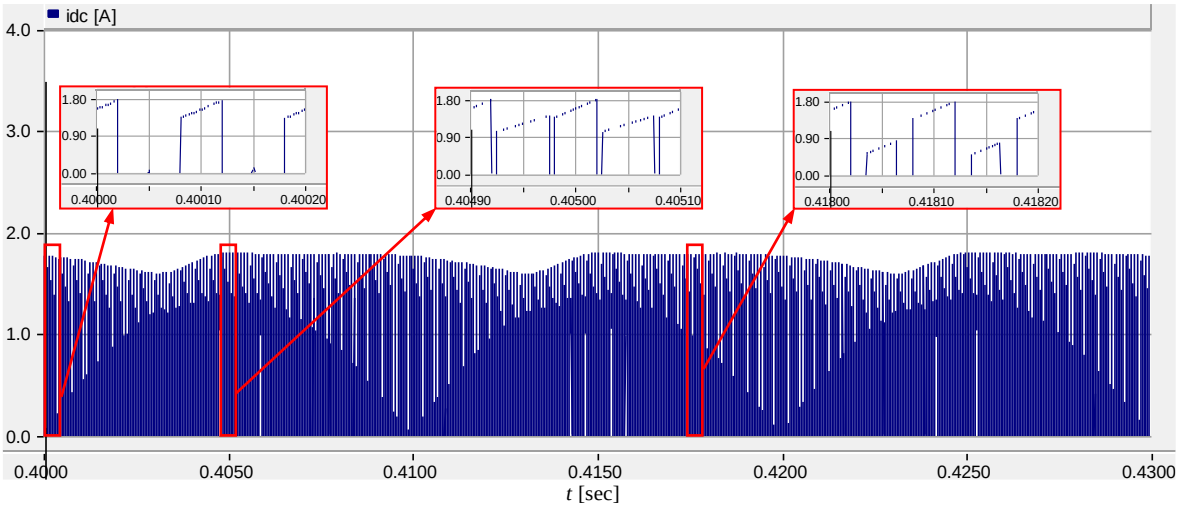


(c)

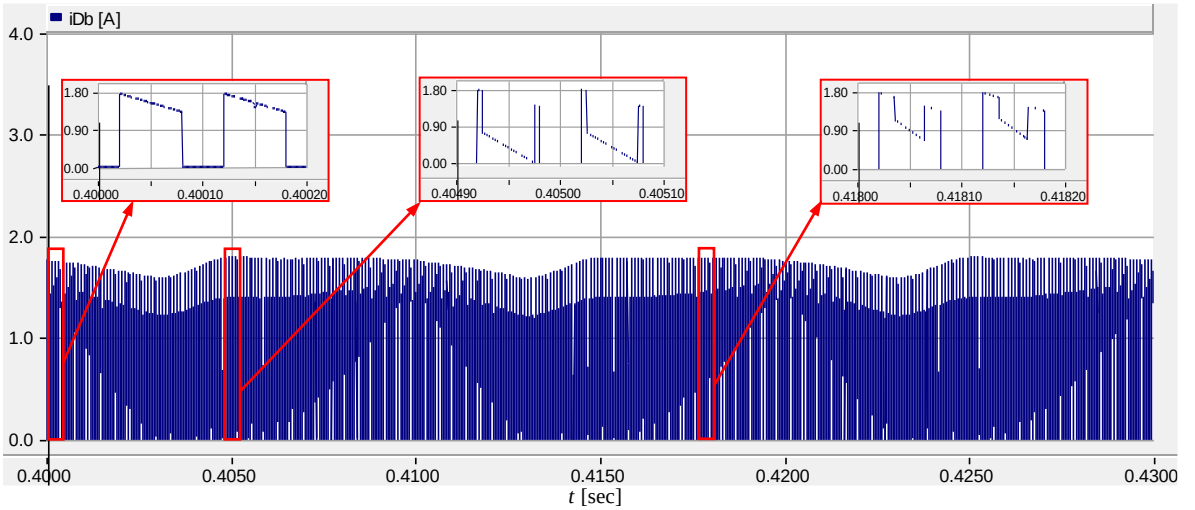


(d)

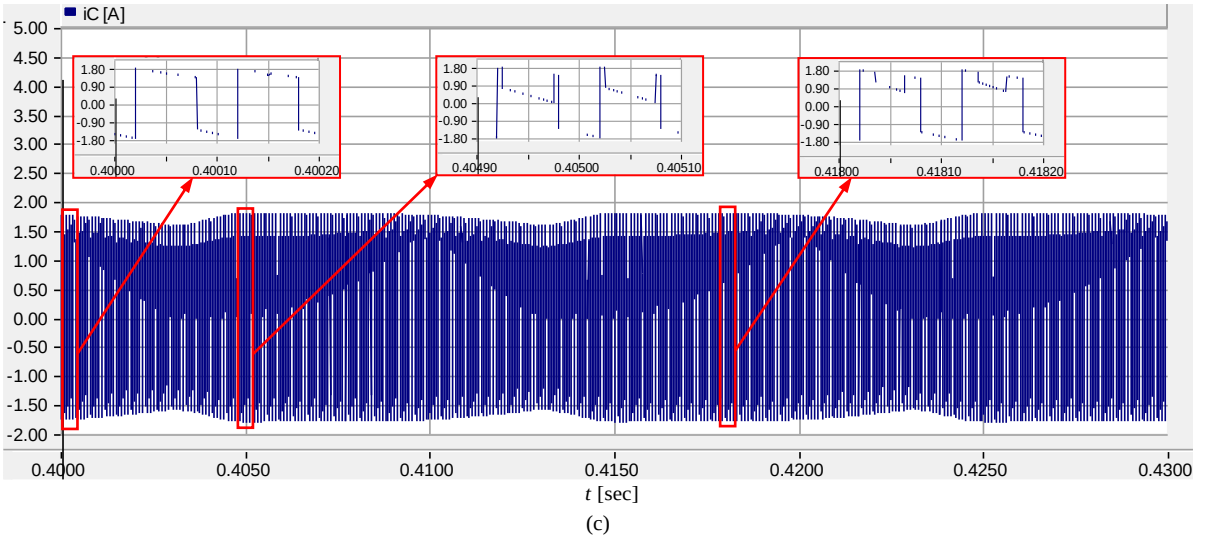
Fig. 16. Waveforms of voltage and current using second control method; (a) voltage and current of *L*; (b) voltage and current of *S*; (c) voltage and current of D_a; (d) voltage across D_b, *C* and dc-link



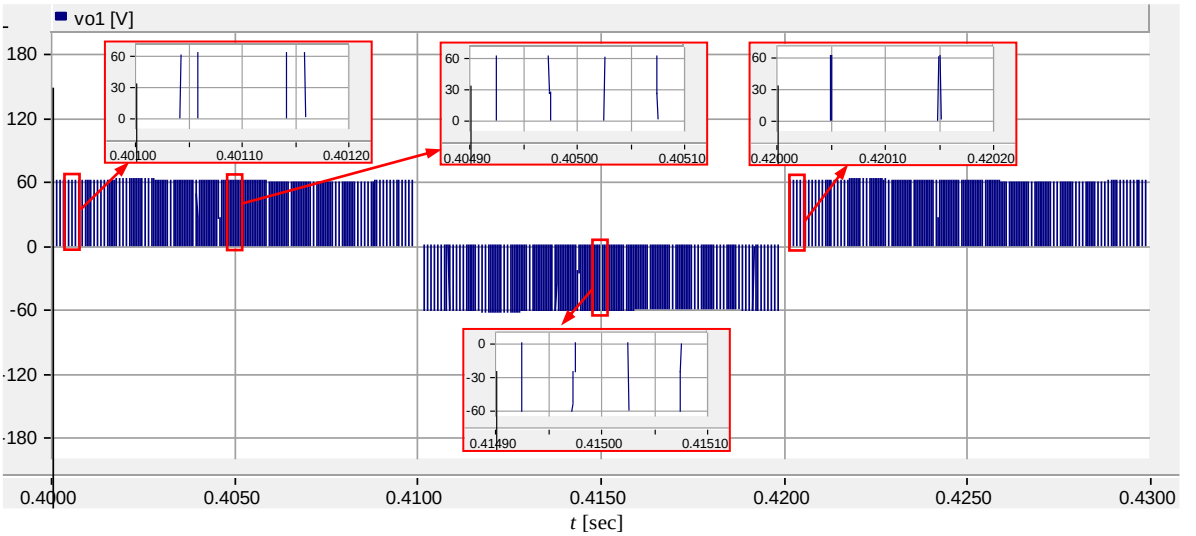
(a)


iDb [A]
4.0
3.0
2.0
1.0
0.0
1.80
0.90
0.00
0.40000
0.40010
0.40020
0.40490
0.40500
0.40510
0.41800
0.41810
0.41820
0.4000
0.4050
0.4100
0.4150
0.4200
0.4250
0.4300
t [sec]

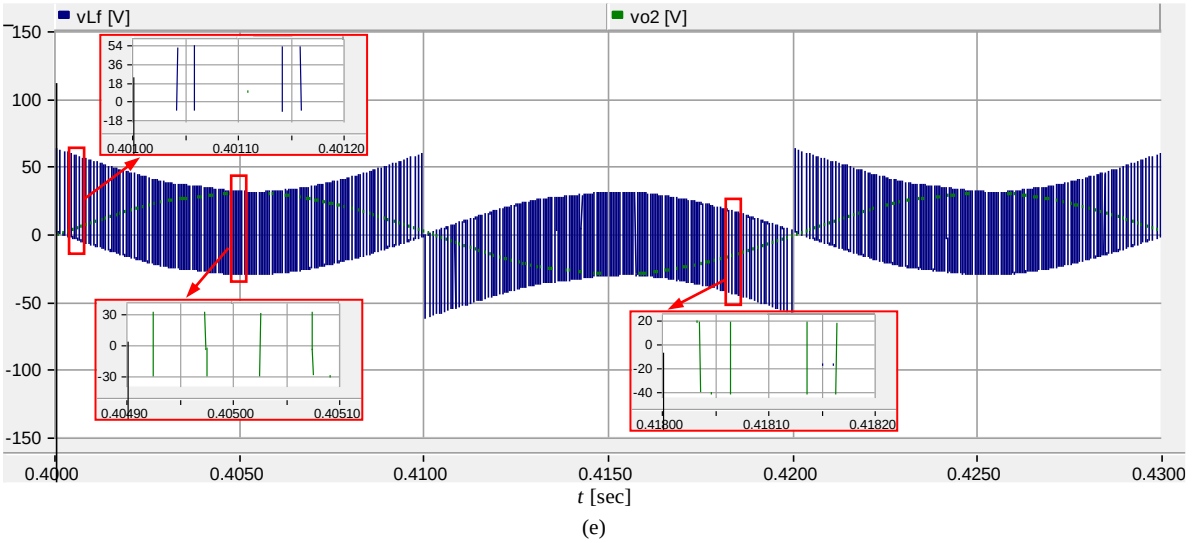
(b)


iC [A]
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
-0.50
-1.00
-1.50
-2.00
1.80
0.90
0.00
-0.90
-1.80
0.40000
0.40010
0.40020
0.40490
0.40500
0.40510
0.41800
0.41810
0.41820
0.4000
0.4050
0.4100
0.4150
0.4200
0.4250
0.4300
t [sec]

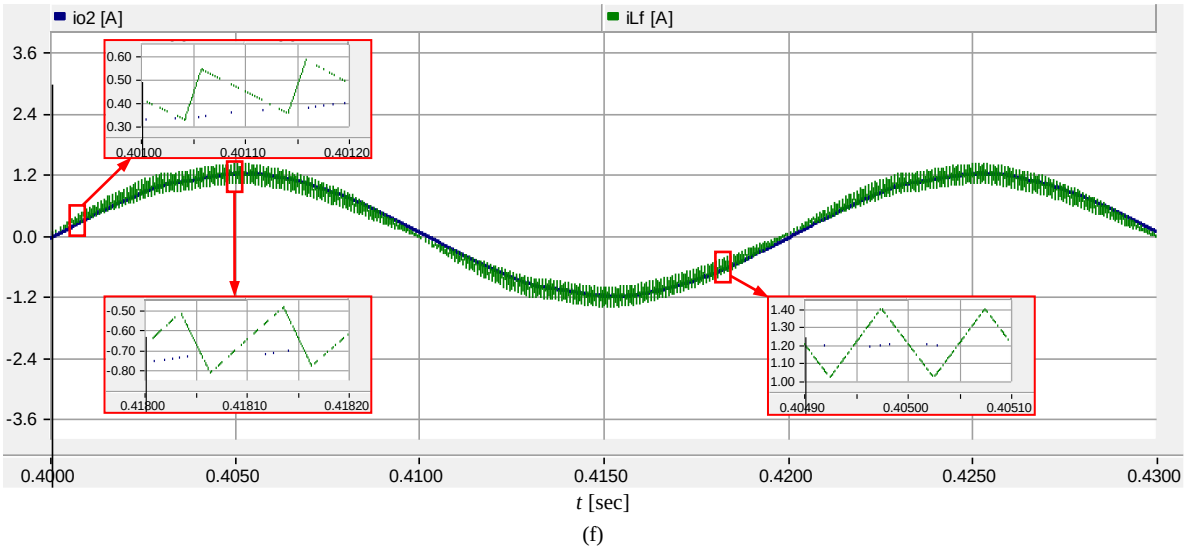
(c)


vo1 [V]
180
120
60
0
-60
-120
-180
60
30
0
-30
-60
0.40100
0.40110
0.40120
0.40490
0.40500
0.40510
0.42000
0.42010
0.42020
0.41490
0.41500
0.41510
0.4000
0.4050
0.4100
0.4150
0.4200
0.4250
0.4300
t [sec]

(d)



(e)



(f)

Fig. 17. Inverter waveforms using the second control method for one output period (T_o).

C. Simulation results for the third control method

The control signals using the third control method are shown in Fig. 18. The switches gate signal of the inverter bridge and S are turned on and off with frequency of $f_s = 5kHz$. When S is turned on, the inverter is in ST state, and when S is off, the inverter is in nST state. In this switching method, there are two identical time periods for creating the ST mode and the duration of each of these time periods is equal to $(D_{ST}T_s)/2$. The duty cycle is equal to 0.4, based on Table 2. So, S will be switched on for 40% of a T_s.

The steady state current and voltage waveforms of SBI components are illustrated in Fig. 18. V_L and i_L are shown Fig. 19(a). According to Fig. 19(a), V_L is equivalent to 60V in ST mode, which is in a good agreement with (2). Also, in the nST mode, its value is around -40V, which confirms (13). i_L increases linearly in ST mode and reaches its maximum value, and in nST mode, i_L decreases linearly until it reaches its minimum value. The maximum and minimum values i_L according to the (84) and (85) are equal to 7.41A and 6.98A, respectively, which is confirmed by Fig. 19(a). Also the ripple of i_L, according to (85) is equal to 0.43A which is in a good agreement with the values of the waveform of L. The voltage and current passing through the switch are illustrated by Fig. 19(b). S is turned on in the ST state and V_S is zero, and i_S is equal to i_L, according to (6). In nST mode, S is turned off and i_S reaches zero. According to (15), V_S is equal to 40V which is confirmed by Fig. 19(b). Figs. 18(c) and 18(d) present the waveforms of current and voltage of D_a and D_b which are off in ST mode and the current passing through them is zero and they are turned on in nST mode. V_C, i_C and i_{dc} are shown in Fig. 19(e). V_C is

around 60V, which confirms (24). i_C is same as $-i_L$ in the ST mode and in the nST mode, it is equivalent to iD_b. According to the dc-link voltage waveforms, its maximum value is equal V_C, which shows that in the nST mode, the dc-link voltage is equal V_C. i_{dc} is equivalent to i_L in ST mode and in nST mode, it is same as the current passing through the load. In Fig. 19(f), the input voltage and the output voltage of the inverter are presented. The input voltage is 20V, and the maximum output voltage of the inverter is same as the maximum voltage of the dc-link, 60V.

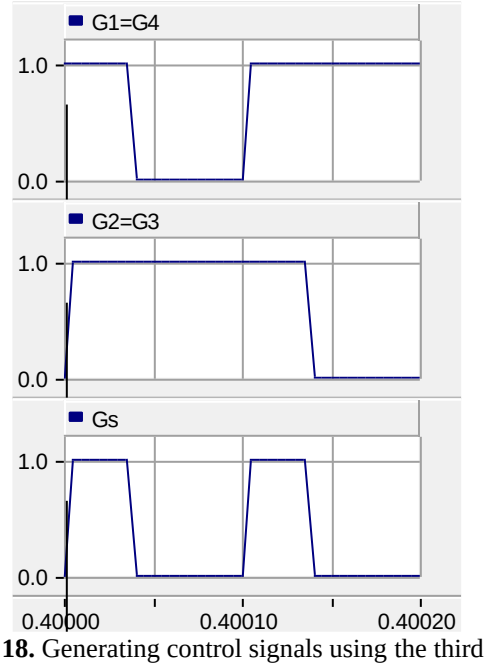
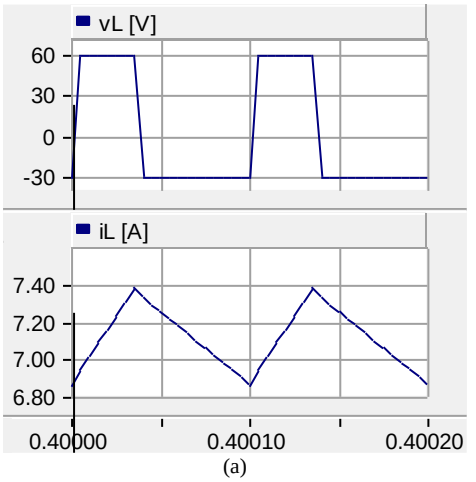
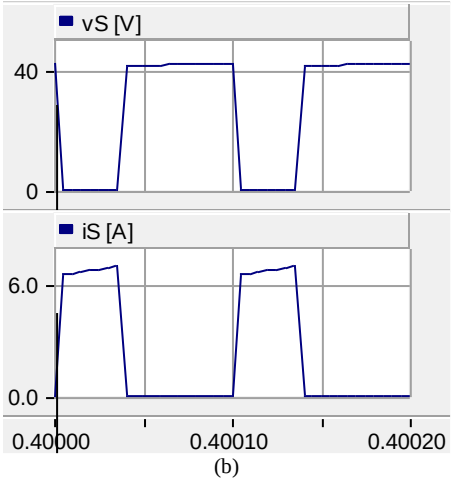


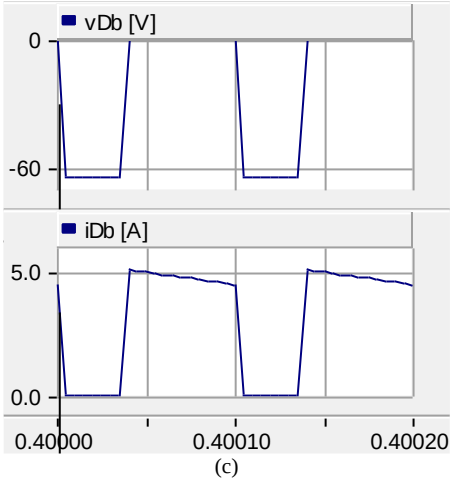
Fig. 18. Generating control signals using the third control method.



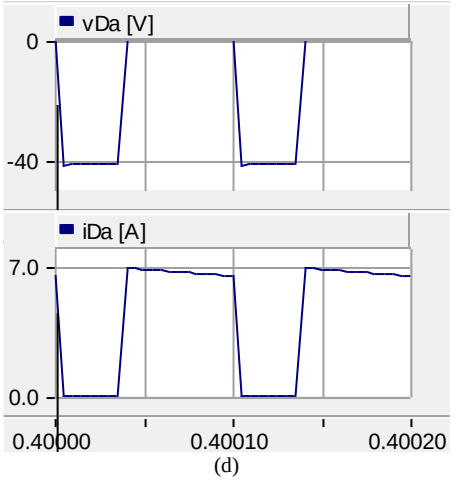
(a)



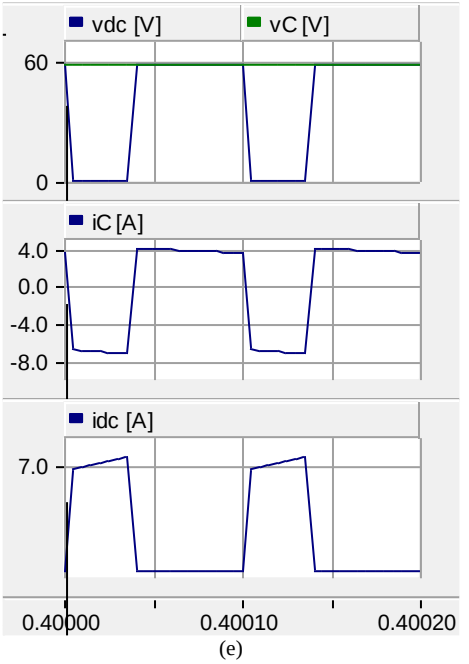
(b)



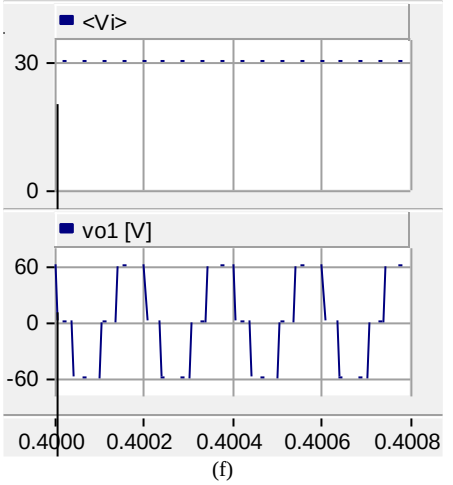
(c)



(d)



(e)



(f)

Fig. 19. Waveforms of voltage and current using third control method; (a) voltage and current of *L*; (b) voltage and current of *S*; (c) voltage and current of D_a; (d) voltage and current of D_b; (e) voltage and current of C and dc-link; (f) input and output voltage of inverter.

The harmonic spectrum results of the three proposed PWM techniques are provided in Table 3. According to this table, the first PWM technique is suitable for applications with petite sensitivity to the quality of the output voltage waveform. The THD value of the second PWM technique satisfies the IEEE standards and is within the allowed range, so this technique requires a smaller output filter and is considered a more suitable option for grid-connected applications. In the switching frequency, the THD value of the third PWM technique equals 28.18%, which can satisfy the demands in the electrochemical industries.

Table 3. Harmonic spectrum results of the three proposed PWM techniques

	First PWM Method (base frequency=50*Hz*)	Second PWM Method (base frequency=50*Hz*)	Third PWM Method (base frequency=5*kHz*)
1st	100%	100%	100%
3nd	33.35%	1.12%	5.87%
5nd	20%	0.87%	15.83%
7nd	14.31%	0.4%	15.81%
9nd	11.14%	0.12%	5.66%
11nd	9.13%	0.2%	4.6%
13nd	7.74%	0.29%	8.46%
15nd	6.73%	0.07%	5.22%
17nd	5.95%	0.06%	1%
19nd	5.34%	0.12%	5.18%
THD	47.78%	1.76%	28.18%

5. CONCLUSION

In this paper, first the analysis of switched boost inverter was reviewed in both ST and nST operation modes and the boost factor of the inverter was extracted. In addition, the key waveforms of the inverter were presented. Then, three new control methods based on PWM technique were presented for this inverter. For each control method, the details of extracting gate signals for switches were presented and the key waveforms of voltage and current of the inverter were given with complete analysis. Based on Table 3, the first and second control methods, the output voltage has low frequency (network frequency) and these control methods are suitable in gird tie application of SBI. But in the third control method, the output voltage has high frequency and this method is suitable for electrochemical applications. For all control methods, the effect of the short circuit was considered in the behavior of the inverter. Finally, the correctness of the given theoretical analyses and control methods were proved by simulation results using PSCAD-EMTDC software.

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