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Semiconductor Chipping Improvement via a Full Sandwich Wafer Mounting Technique

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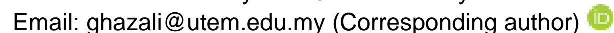
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ABSTRACT:
Silicon wafers have been widely used in semiconductor manufacturing, and chipping issues often highlighted during wafer dicing which affects device performance and reliability. The phenomenon of chipping has been observed to have detrimental effects on die strength, leading to the potential of crack formation. Cracks became a major concern because its sometimes undetected during testing and had been reported to cause malfunctions at user applications. This study aims to comprehensively analyze the fragile behavior of silicon concerning its chipping and flexural strength performance, providing valuable insights for engineering applications. The research employed new wafer mounting techniques, including chipping analysis, a three-point bending test and scanning electron microscopy (SEM) to reduce silicon die chipping and increase the flexural strength by evaluating the novel semi and full sandwich wafer mounting techniques. The study demonstrated that the implementation of novel full sandwich mounting technique had improved significantly the silicon die chipping and flexural die performance among all the wafer mounting techniques.

KEYWORDS: Chipping, Silicon, Three-Point Bending Test, Wafer Dicing, Wafer Mounting.

1. INTRODUCTION

Silicon has been widely used in wafer fabrication in semiconductor manufacturing [1]. The reason silicon is more popular for wafer fabrication is due to its abundant element on earth [2] which ensures a stable supply for wafer fabrication. Technology and innovation in the semiconductor sector have been developing at an incredible rate in recent years and silicon wafers have become the backbone of the integrated circuit industry. Silicon is a material that belongs in the category of semiconductors [3] because, under certain circumstances, it has the potential to conduct electricity. It

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is possible to alter its conductivity by a process known as doping, which involves the introduction of impurities. Additionally, silicon is preferable due to its higher melting point. Because of its high melting point [4], silicon has an additional advantage which can resist high temperatures [5] during the fabrication process. This feature is critical in the manufacture of integrated circuits, where silicon wafers are subjected to extreme heat.

However due to silicon brittle nature [6][7], it has a tendency to chip or crack [8] when subjected to mechanical stress or impact. It is a severe issue in silicon wafer manufacturing that may result in yield loss and lowering die strength [9] performance. Chipping was the main concern in the wafer dicing process since it is unavoidable [10] and could generate cracks during its application. Chipping is the term used to describe the area that is taken from the edge of the silicon die during the wafer sawing process [11] as per "Fig. 1" below. The most concerning scenario was the crack generated by the chipping that sometimes can not be detected during testing and failed during application on the customer side.

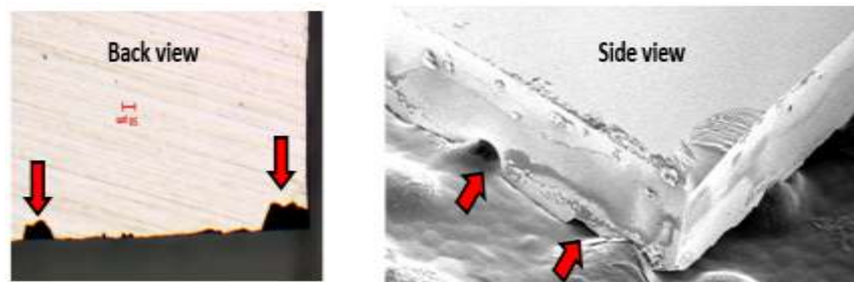

Fig. 1. Chipping definition.

Hong Zhang reported that the yield and reliability performance of the Integrated Circuit (IC) itself depends on the topside and backside chipping performance [12] thus both chipping must be minimised [13] either by wafer mounting process or wafer dicing process. Since the wafer mounting process has the potential to improve the chipping performance, the new mounting techniques will be evaluated and compared with the conventional wafer mounting method. Conventional wafer mounting is a process whereby a wafer is attached to a wafer ring by a mounting tape which acts as a carrier [14] for the wafer dicing process as described in "Fig. 2". The conventional mounting technique has its own weakness whereby the wafer does not have enough support during the dicing process which may cause more vibration resulting in higher chipping results.

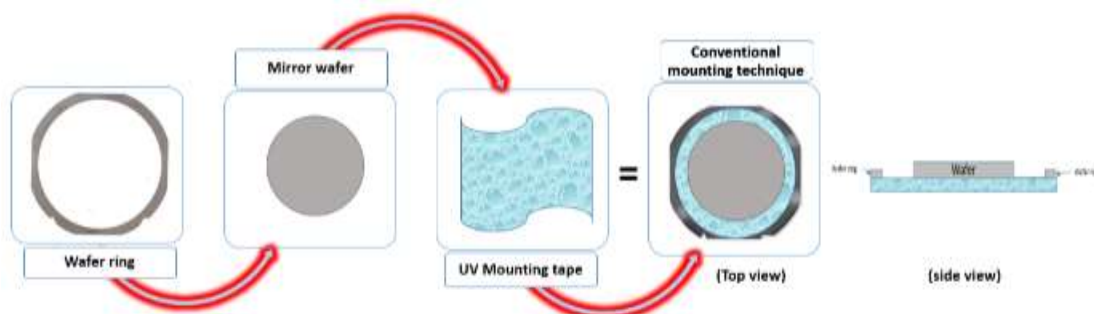

Fig. 2. Conventional wafer mounting technique.

During the wafer mounting process, both ultraviolet (UV) mounting tape and non-UV mounting tape were often utilized on the manufacturing floor. UV mounting tape, in comparison to non-UV mounting tape, has a stronger adhesion strength [15], which makes it possible to hold the back of the wafer firmly [16]. The adhesive on the surface of wafer mounting tape secures the wafer's position [17][18] during the wafer dicing procedure. The usage of high adhesive tape was done in order to reduce topside and backside chipping that occurred during the wafer dicing process. Bryan Christian [19] claimed that the vibrations created by severe chipping during mechanical dicing [20] can lead to cracks in the silicon die. This is why the UV tape was fixed for this activity in order to achieve the objectives of lower chipping and higher flexural strength performance. The assessment of novel semi and full-sandwich wafer mounting techniques was carried out, comparing both chipping and die strength performance against the conventional wafer mounting technique. The semi sandwich wafer mounting technique was designed to provide a cushioning effect during the wafer dicing process which may reduce the vibration and chipping as well. The semi sandwich wafer mounting technique process approach

was by applying the wafer surface with additional mounting tape which has been described in “Fig. 3”. The wafer surface was laminated first by the mounting tape and then continued as per the normal wafer mounting process.

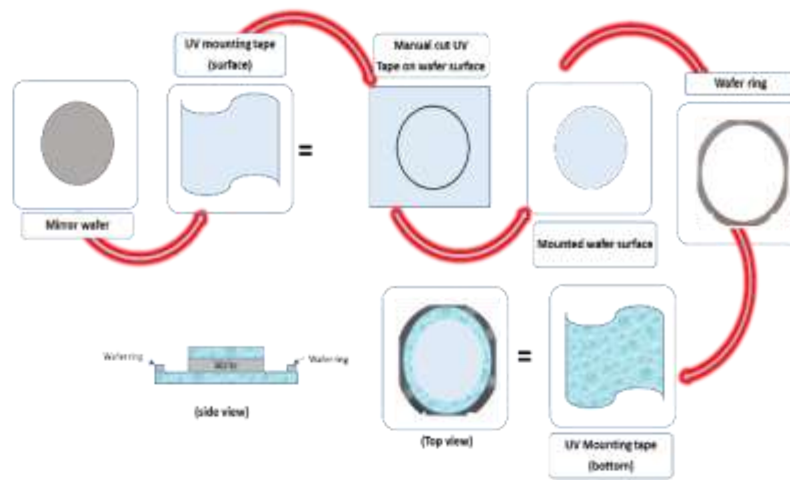

Fig. 3. Semi sandwich wafer mounting process.

The novel full sandwich wafer mounting technique was engineered to offer maximum wafer gripping with the expectation of the lowest chipping outcome during the dicing process. The technique is a combination of conventional mounting and further laminating the wafer surface up to the wafer ring area as shown in “Fig. 4”.

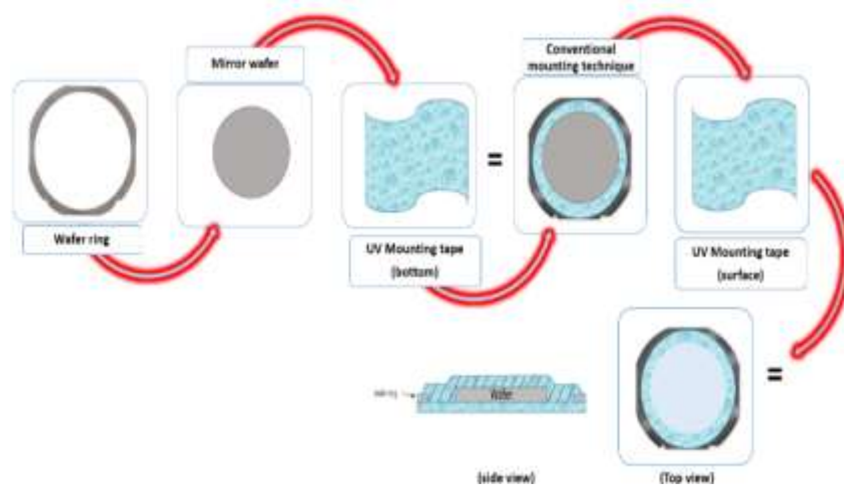

Fig. 4. Full sandwich wafer mounting process.

The wafer ring and mirror wafer were mounted using UV tape at the wafer's backside as a first step. The mounted wafers then were mounted again to cover the wafer surface up to the wafer ring area to provide extra interlocking between the UV tape with the wafer surface up to the wafer back area. By having this technique, the mounted wafer gained more stability during the dicing process and is expected to produce better chipping performance.

To summarize the process flow of all mounting techniques, “Fig. 5” displayed the comparison of steps to complete for each mounting process before the chipping measurements were performed. Among all the mounting techniques, semi sandwich mounting techniques had the longest process due to additional manual cutting on the surface mounting process before the normal wafer mounting continued to proceed.

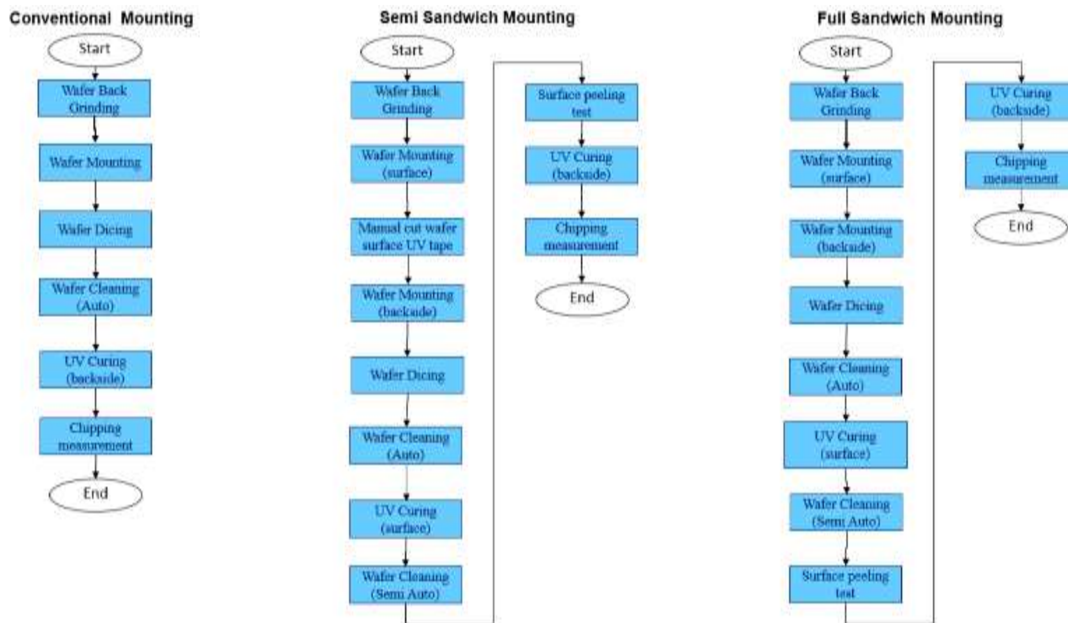

Fig. 5. Process flow of each mounting technique.

In this paper, once the silicon dies chipping results were obtained, the flexural strength evaluation using three-point bending test method then were analyzed. Flexural strength represents the maximum stress that a material can withstand before it fractures or breaks when subjected to a bending force. The unit of measure for 3-point bending flexural strength is typically expressed in Newton per millimeter square (N/mm2) or Mega Pascal (MPa) according to standard SEMI G86-0303 [21]. The purpose of this study is to investigate the relationship between die strength and chipping performance in implementing a novel sandwich mounting approach, as compared to the conventional mounting technique.

2. MATERIAL AND METHODOLOGY

This section revealed the materials that were used during evaluation, key parameters, and the equipment involved according to the process flow.

2.1. Wafer Back Grinding

In this activity, 8-inch non-circuitry, also known as mirror silicon wafers were used and ground to the final thickness of 300 µm. The back grinding machine parameters were fixed for all wafers and using Disco Fully Automatic Grinder/Polisher DGP 8760. All silicon wafers were ground with mechanical Z1 rough grind (360 grit) and then followed by Z2 mechanical fine grind (2000 grit) with the final results producing grinding marks as per "Fig. 6" below.

Fig. 6. Grinding marks.

The back grinding process produced initial mechanical stress on the silicon wafer [22] and the grinding marks produced weaker adhesion on mounting tape [23]. The unevenness of the wafer back is critical for silicon chipping performance during wafer dicing and optimization at the wafer mounting process is very important to hold the wafer firmly to minimize chipping which affects the die strength as well [24].

2.2. Wafer Mounting

To conduct the evaluation of the silicon wafer, UV and non-UV mounting tapes were evaluated for all assessment runs. The leveling and cleaning were executed to provide the optimum mounting outcomes on Lintec RAD-2500 wafer mounter before the evaluation started. To minimize the process variation, the wafer mounting orientation for each mounting technique was fixed. The types of mounting tape setup for all the assessment runs were according to Table 1 below.

Table 1. Wafer mounting technique setup.

Wafer Mounting Technique	Type of Mounting Tape on Wafer Surface	Type of Mounting Tape at Wafer Back	UV Curing after Dicing
1) Conventional Mounting	No mounting tape	UV Tape A	Yes
2) Semi Sandwich Mounting	Non UV Tape	Non UV Tape	No
	UV Tape A	UV Tape A	Yes
3) Full Sandwich Mounting	Non UV Tape	Non UV Tape	No
	UV Tape A	UV Tape A	Yes
	UV Tape B	UV Tape B	Yes

The conventional mounting technique is a single-sided mounting technique whereby the mounting tape is applied on the wafer backside area only as shown in "Fig. 2". To improve the wafer gripping on the surface and backside of the wafer, two novel double-sided full sandwich mounting techniques were introduced. In this mounting tape evaluation, two variants of UV mounting tapes and one non UV mounting tape were evaluated. The UV mounting tape was made with Polyolefin while the non-UV mounting tape was made with Polyvinylchloride.

Table 2 provides specific information regarding the mounting adhesion for reference purposes. Note that UV tape requires UV curing to reduce adhesion [25] for the die pick-up procedure. However, UV tapes were also used for surface peeling tests as part of this activity. Noteworthy is the fact that UV Tape A exhibits superior adhesion performance (before and after UV) compared to UV Tape B due to higher adhesion after UV specification. The rationale for employing both UV Tape A and B in the full sandwich technique was based on the surface peeling results, which were then elaborated upon in the subsequent discussion section. The utilization of Non UV tape obviates the need for UV curing procedures.

Table 2. Evaluated Mounting tape specifications.

Info		UV Tape A	UV Tape B	Non UV Tape
Tape thickness (µm)		85	85	80
Base film (µm)		80	80	70
Base film material		Polyolefin	Polyolefin	Polyvinylchloride
Adhesive layers (µm)		5	5	10
Adhesion (mN/25mm)	Before UV	4900	3100	940
	After UV	80	30	

The adhesion UV tape specification value before UV was used as a reference for dicing chipping performance while the value after UV was used as a reference for surface peeling test performance for both UV tape A and B. While for Non UV tape the "Adhesion 940 mN/25mm" was used for surface peeling test reference during the evaluation.

2.3. Wafer Dicing

During the wafer dicing process, a total of 3 wafers according to mounting techniques were sawn with fixed die size 6 x 6 mm using Disco DFD6362 Fully Automatic Dicing Saw machine. During the assessment, the wafer dicing parameters were fixed for all the 3 wafers. Dicing was using a single cut method with 30% depth of the total thickness of the mounting tape as displayed in Table 3.

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Table 3. Fixed dicing parameters on Disco DFD6362 machine.

Dicing parameters	Machine setting
Die Size	6.00 x 6.00 mm
Work Thickness	0.300 mm
Cut Mode	Single cut
Spindle Revolution	40K /min
Feed Speed	30 mm/s
Cut Depth	0.0065 mm

The selection of the single cut technique was based on its inherent difficulty in achieving a balanced performance in terms of topside and backside chipping [26]. However, if single cut wafer dicing is successfully executed, this technique has the potential to provide the most productive process, as indicated by a higher Unit Per Hour (UPH) indicator which is illustrated in "Fig. 7" below. In the evaluation, the same diamond dicing blade was utilised for wafer dicing process to minimize the process variation

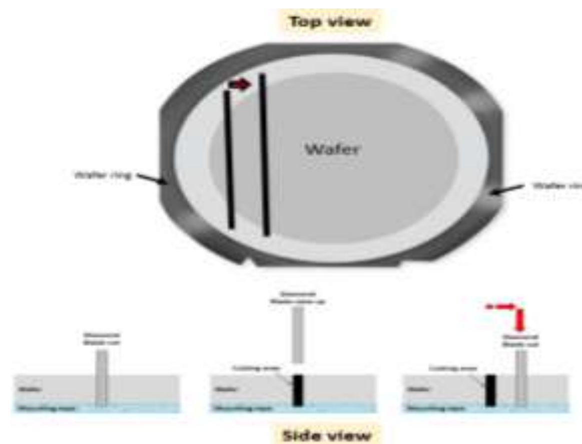

Fig. 7. Single cut illustration.

After the completion of the dicing process, the subsequent step involves the initiation of the cleaning procedure for non-UV tape application as illustrated in "Fig. 8". In the case of using the non-UV mounting tape, after the wafer has completed the dicing process it will be sent for the cleaning process.

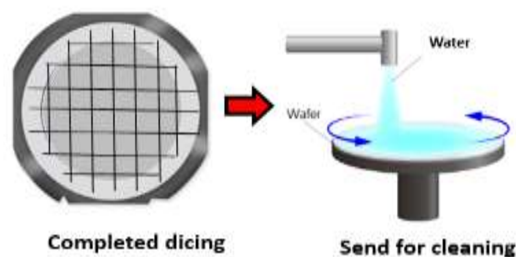

Fig. 8. Dicing process on non-UV mounting tape.

However, in the case of a wafer that has been affixed with UV mounting tape, it is necessary to carry out a UV curing process prior to reducing the adhesion of the tape on the wafer surface and wafer backside as well. The UV mounting tape on the wafer surface must be peeled off during the cleaning process as described in "Fig. 9" in order to proceed for the die chipping measurement process.

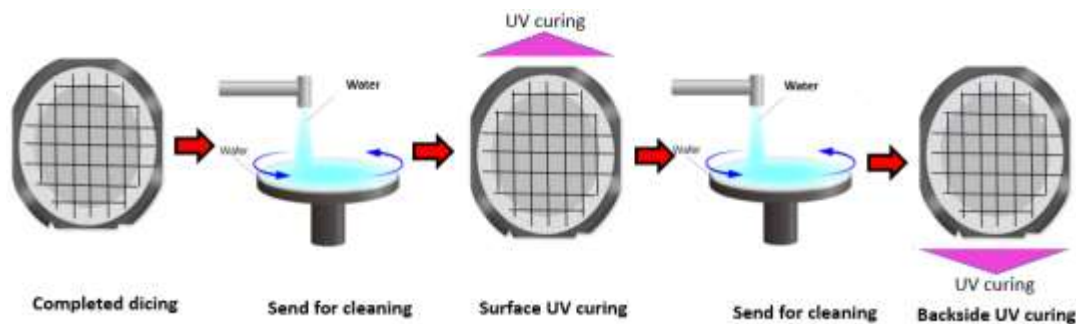

Fig. 9. Dicing process on UV mounting tape.

2.4. UV Curing

The basic UV curing usage was to reduce the adhesion of UV mounting tape for an easy pick-up process during die attach. However, for this activity, the UV curing process will continue the basic task with additional peeling off the surface mounting tape as well. UV curing activities require two times curing tasks for both the backside and surface area as illustrated in Fig. 9. The backside UV curing will use the normal UV curing parameter while surface UV will require a higher UV dosage to ensure the surface mounting tape will be easy to peel off. However, for all evaluations using UV mounting tape, the UV curing parameter had been fixed to minimize the variation during the evaluation. The UV curing was performed on Lintec RAD-2010 equipment as per “Fig. 10” below.

Fig. 10. Lintec RAD 2010 UV Curing machine

In this activity towards the UV curing process, the UV parameter below the setting in “Fig. 11” was evaluated during the evaluation. A number of UV curing will be evaluated according to the surface peeling test result. If the peeling results cover more than 90% of the surface area then the UV curing process will stop, otherwise the curing will keep repeating using the same parameter until the objective been achieved.

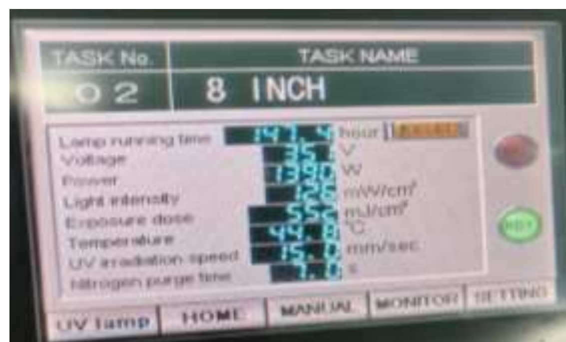

Fig. 11. Fixed UV Curing parameter.

2.5. Surface Peeling Test

The new introduced wafer surface peeling test is the main criterion for the success of this evaluation. Below in “Fig. 12” is how the wafer surface peeling test was conducted.

Fig. 12. Wafer surface peeling test procedure.

The wafer surface peeling test was conducted on the wafer dicing chuck table with condition vacuum ON. This is to ensure the wafers are held firmly during the test and eliminate additional chipping during the peeling process due to die movement and rubbing with the neighboring die. A cellophane tape was applied to the silicon wafer surface and then the peeling process was initiated. If the wafer surface mounting tape is able to peel > 90% of the total wafer areas, then the chipping measurement will continue and the UV curing parameter and procedure will be fixed. In the event that the peeling result is lower than 90% yield, it prompts the termination of the evaluation process and then stop the selection of the mounting tape.

2.6. High Power Scope

After the wafer dicing and wafer surface mounting peeling test process was completed, a Zeiss Axioscope 2 MAT optical microscope then was used for every silicon die inspection and chipping measurements activities. Before initiating the measuring activity, the scope was first put through the calibration procedures. For the purpose of measuring chipping areas, the scope setting was established at 50x magnification. In order to conduct a detailed inspection of cracks originating from the chipping area, a higher magnification level was employed to assess their condition. As part of the experimental procedure, a total of 30 dies were selected from each wafer, encompassing both mounting techniques.

The silicon dies were picked up using plastic tweezers and a vacuum pen to prevent chipping caused by handling. Since the die size is too large to capture the entire inspection area with a high-powered scope, the die areas were divided into 12 sections according to "Fig. 13". The images for each portion were saved according to section and then transferred to the "ImageJ" software for measuring the chipping areas. Similar to Shang Gao's method [27], the chipping area calculation was performed using Autocad instead of ImageJ. without making any physical contact. In order to determine what factors contribute to excessive chipping during the wafer dicing process, the topography of the wafer's backside was analyzed using a 3D profilometer.

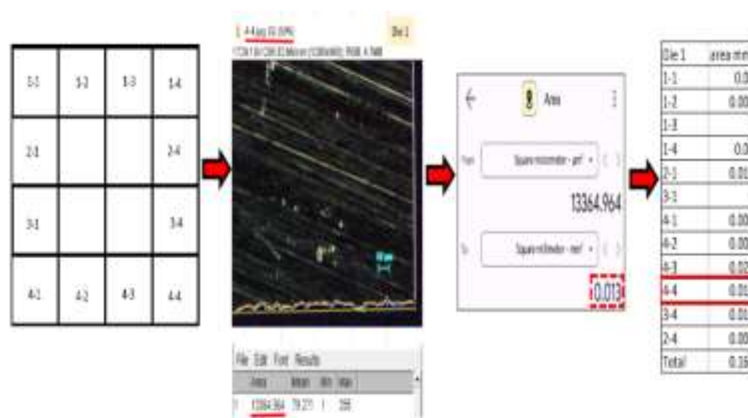

Fig. 13. Chipping area calculation.

The chipping areas were captured in sections and uploaded to "ImageJ" software, where the areas were measured in µm2 and then converted to mm2 to determine the overall chipping areas. The section chipping areas were then summed up to represent from overall chipping area per die unit (6 x 6 mm = 36 mm2) and this process was repeated up to 30 die samples for each mounting technique. Recent research by Shang Gao has suggested the same method of calculating the chipping edge measurement using area calculation method using software [27]. The only difference on both methods was the type of software used based on Autocad and for this assessment ImageJ is being applied to measure the chipping

area, however, the method is the same. For illustration of the methodology towards the overall evaluation could be referred in Fig. 14 for reference. Since there were 3 mounting techniques used in the evaluation, it required a total of 90 samples for chipping measurements. As illustrated in “Fig. 13” the chipping measurements were divided into 12 sections per unit. Due to chipping measurements required on topside and backside chipping it means that 1 unit was measured based on 24 chipping measurements. As there were 90 samples in this evaluation it means there were 2,160 measurements were taken for chipping analysis.

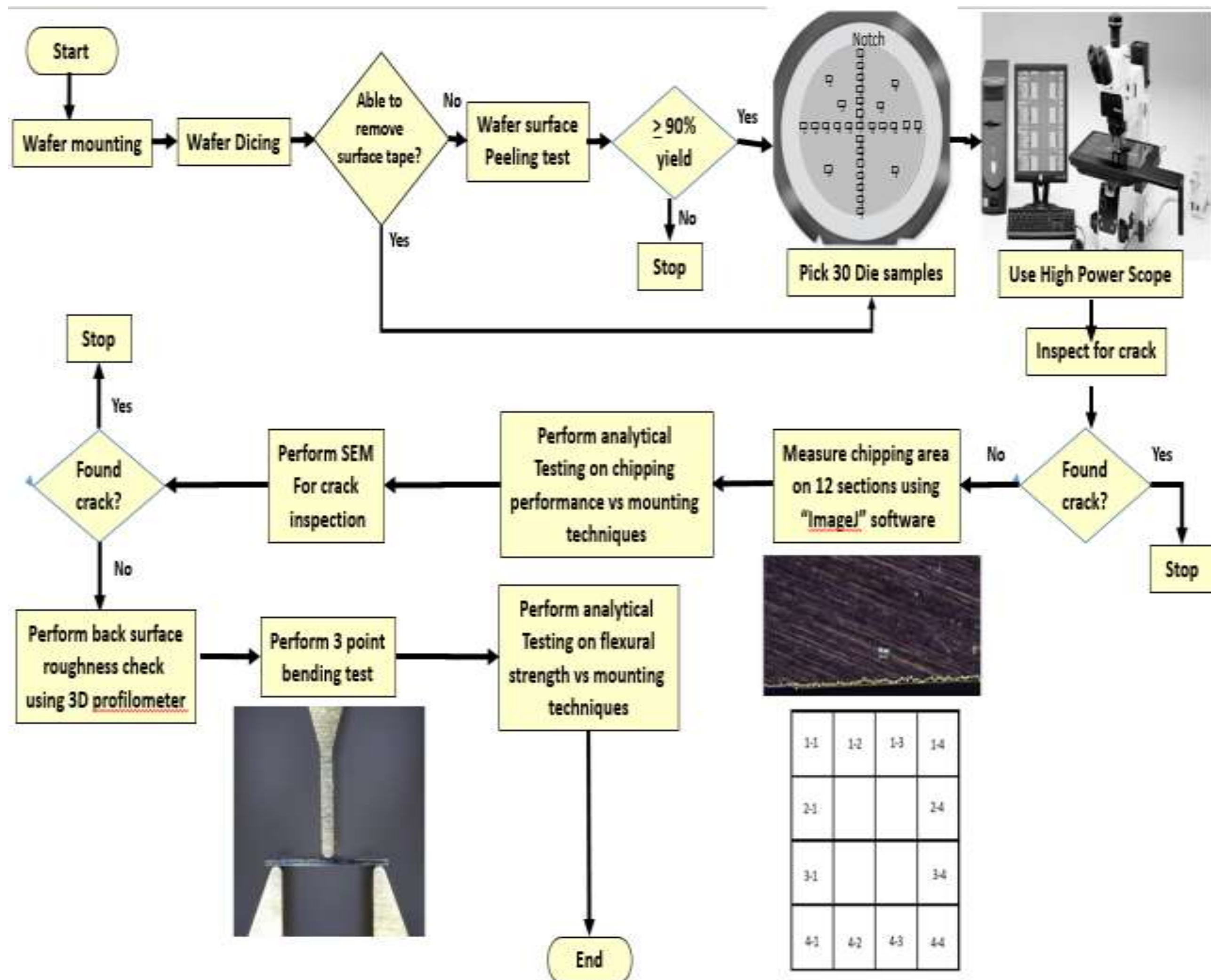

Fig. 14. Methodology for chipping area data collection.

2.7. Scanning Electron Microscope (SEM)

SEM was utilized to verify the presence of crack occurrence towards the silicon die after the wafer dicing process. The magnifications were based on 100 x, 400 x, and 1000 x which focused on areas that were suspected to have cracks since high power scope has its own limitations in terms of the magnification scale. This is to ensure the dicing quality during the developing of the novel full sandwich wafer mounting technique is crack-free.

2.8. 3D profilometer

A 3D profilometer based on a non-contact Shodensha GR3400 profiler was used to acquire three-dimensional measurements of the silicon die back surface topography. The system uses light to take measurements of the surface without really touching it. This was done to determine if the surface roughness and topography of the rear silicon grinding marks contribute to the wafers' tendency to chip excessively during the dicing process.

2.9. Three-point bending test

For the three-point bending test on the silicon die, the flexural strength (given the symbol σ) could be used according to the following equation (1) [23]:

$$\sigma_{3\,point} = 3sF / 2wh^2 \quad (1)$$

whereby F = Force of fracture

s = span

w = width of the die

h = thickness of the die

The definition of the equation above is illustrated below in “Fig. 15”.

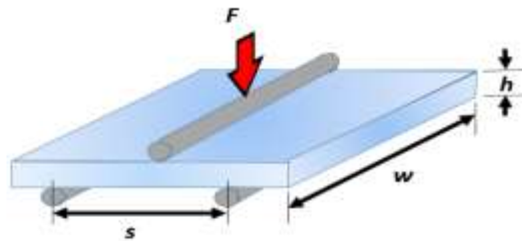

Fig. 15. Three-point bend test equation illustration.

The flexural strength of a material refers to its inherent ability to withstand deformation or fracture under the influence of an externally applied force acting perpendicular to its surface. Among the various techniques employed for the purpose of die strength characterization, the 3-point bending test [28] stands out as the most prevalent and widely adopted method within the semiconductor industry [29]. For this activity, the three-point bending test for flexural strength on the silicon die was done using 50N Shimadzu EZ-LX which can be referred to “Fig. 16” below.

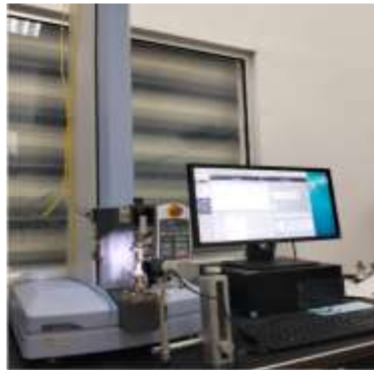

Fig. 16. Shimadzu 50N EZ-LX setup.

The jig was designed according to SEMI G86-0303 Standards. Since the jig was designed based on fixed span the span was set to 5mm [30], pin radius of 0.3 mm, and the test speed was fixed at 3mm/min. The three-point bending test operation was connected to a camera to ensure the die was placed evenly on the jig and the punch was aligned to the center of the die surface as per “Fig. 17”.

Fig. 17. Camera feature to ensure consistent die positioning on jig during three-point bending test.

3. RESULTS AND DISCUSSION

This section displays all the evaluation results according to the methodology set earlier stage by stage. The results were based on the application of UV and non-UV mounting tape to understand which tape is more suitable for the new full sandwich wafer mounting technique. It is important to acknowledge that the primary goals of this study were to enhance the new peeling process by increasing the tape removal on the wafer's surface through the mounting tape application, with a target of achieving an area coverage of over 90%. Additionally, the study aimed to minimize the measurement of the chipping area and improve the flexural strength of the silicon wafer

3.1. Wafer Cleaning

Wafer cleaning is considered one of the important factors during the evaluation. If the surface mounting tape is able to remove during wafer cleaning, then it becomes an advantage since the process flow can be shortened, and it is not necessary to perform a surface peeling test. The following results, as presented in Table 3, represent the outcomes achieved subsequent to the wafer cleaning procedure conducted on various wafer mounting techniques and the corresponding mounting tape employed.

From Table 4, a conclusion could be that the wafer cleaning process is not able to remove the surface mounting tape on all mounting techniques for both UV and non-UV mounting tape. Even for UV mounting tape, the lowest "Adhesion after UV curing 30 mN/25mm" compared to non-UV mounting tape "Adhesion 940 mN/25mm" still not able to remove the mounting tape from the wafer surface. Due to the small dimension of the die (6 mm x 6 mm), even a low adhesion tape adheres well to the wafer surface, making it difficult to remove during the washing process. As both UV and non-UV mounting tapes on full sandwich mounting technique produced negative results when attempting to remove the surface mounting tape, the surface peeling test then is required.

Table 4. Wafer cleaning results on surface mounting tape removal

Wafer Mounting Technique	Type of Mounting Tape on Wafer Surface	Type of Mounting Tape at Wafer Back	UV Curing after Dicing	Full surface mounting tape removal
Conventional Mounting	No mounting tape	UV Tape A (80 mN /25mm)	Yes	Not applicable. No mounting tape applied on wafer surface
Semi Sandwich Mounting	Non UV Tape (940 mN / 25mm)	Non UV Tape (940 mN / 25mm)	No	Unsuccessful
	UV Tape A (80 mN /25mm)	UV Tape A (80 mN /25mm)	Yes	Unsuccessful
Full Sandwich Mounting	Non UV Tape (940 mN / 25mm)	Non UV Tape (940 mN / 25mm)	No	Unsuccessful
	UV Tape A (80 mN /25mm)	UV Tape A (80 mN /25mm)	Yes	Unsuccessful
	UV Tape B (30 mN /25mm)	UV Tape B (30 mN /25mm)	Yes	Unsuccessful

3.2. UV Curing

The UV curing parameter had been fixed during the evaluation and the output response was based on the surface peeling test results. Since the mounting tape had different adhesive thicknesses, the results were based on Table 5 below.

Table 5. UV curing evaluation results on surface mounting tape removal.

UV mounting tape type / Adhesion after UV	UV Curing 1 X and peeling %	UV Curing 2 X and peeling %	UV Curing 3 X and peeling %	Pass / Fail
UV Mounting Tape A (80 mN /25mm)	20%	40%	70%	Fail for all
UV Mounting Tape B (30 mN /25mm)	50%	80%	100%	Pass when UV curing 3 times

Since the UV curing result had positive results on 3 times UV curing, then the activities were fixed with the procedure. The UV curing results showed that higher adhesion specification will encounter a lower percentage of surface mounting tape peeling results.

3.3. Peeling test

The performance of silicon wafer towards surface mounting peeling test was analysed for both UV and non-UV mounting tape. Since the novel full sandwich mounting technique was introduced in this activity, the tape peeling performance is crucial to ensure the effectiveness of the new mounting process for achieving lower chipping performance. The conventional mounting technique in which mounting tape is not applied to the wafer surface will not be evaluated for the peeling test. The overall peeling result of the novel full sandwich mounting technique based on two types of mounting tape can be referred below for reference in Table 6.

Table 6. Surface mounting peeling results

Wafer Mounting Technique	Type of Mounting Tape on Wafer Surface	Type of Mounting Tape at Wafer Back	Surface peeling test yield
Conventional Mounting	No mounting tape	UV Tape A	Not applicable. No mounting tape applied on wafer surface
Semi Sandwich Mounting	Non UV Tape (940 mN / 25mm)	Non UV Tape (940 mN / 25mm)	0% (fail)
	UV Tape A (80 mN /25mm)	UV Tape A (80 mN /25mm)	70% (fail)
Full Sandwich Mounting	Non UV Tape (940 mN / 25mm)	Non UV Tape (940 mN / 25mm)	0% (fail)
	UV Tape A (80 mN /25mm)	UV Tape A (80 mN /25mm)	70% (fail)
	UV Tape B (30 mN /25mm)	UV Tape B (30 mN /25mm)	100% (pass)

From Table 6, results showed the higher adhesion value had produced to lower percentage of surface peeling test results. For non UV tape with "Adhesion 940 mN/25mm", results showed 0% of the yield of surface peeling test results. The higher the mounting tape adhesion value caused higher gripping on the wafer surface which caused the peeling test to fail. Since the usage of Non-UV mounting tape failed on the peeling test, the assessment using the tape was

discontinued. For UV Tape A with lower adhesion value 80 mN/25mm showed improvement in terms of surface peeling test results with 70% yield however still not meeting the min 90% yield target. In order to achieve the surface peeling test yield target, the lowest adhesion value UV mounting was selected. UV Tape B, which exhibited the lowest "Adhesion of 30 mN/25mm", was chosen for the trial run to validate the aforementioned theory. The outcomes of this trial run are presented in "Fig. 18" below.

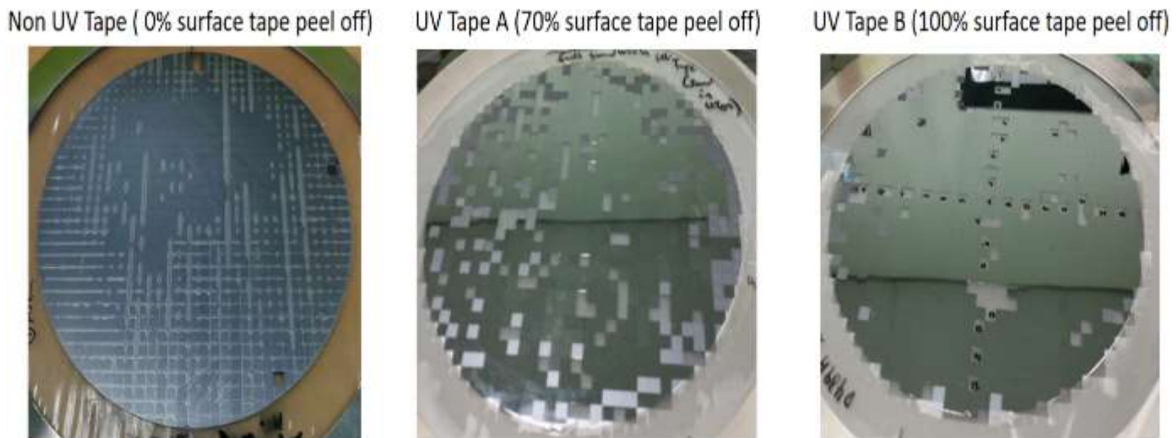

Fig. 18. Surface peeling test results on various tape adhesion level.

UV Tape B, which has exhibited favorable outcomes in the surface peeling test, has been selected for the assessment of its chipping performance. In order to gain insight into the performance of the novel full sandwich mounting technique in minimizing silicon wafer topside and backside chipping during the wafer dicing process, a comparative analysis was conducted between the conventional and novel full sandwich mounting techniques. This analysis is presented in "Fig. 19" based on a 95% confidence level using JMP statistical software.

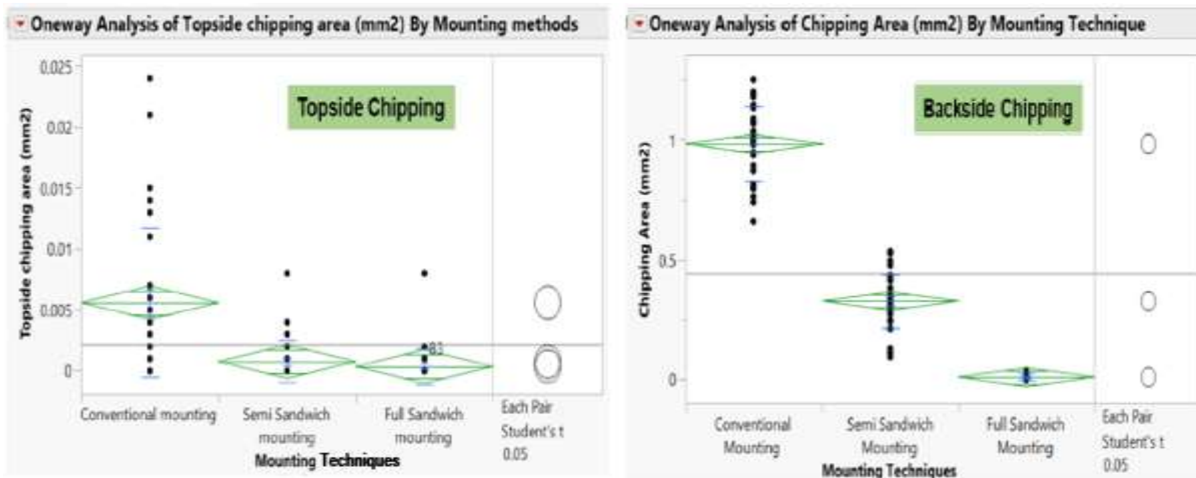

Fig. 19. Topside and backside chipping comparison between conventional, semi, and full sandwich mounting techniques.

According to JMP statistical software, a conclusion could be made that the full sandwich mounting techniques demonstrated significantly lower topside and backside chipping performance compared to the conventional mounting technique. This showed that the chipping behavior of the fragile silicon wafer may be mitigated by applying mounting tape on the wafer surface up to the wafer ring area, also known as the full sandwich wafer mounting technique. The additional gripping and interlocking by the mounting tape on the silicon wafer surface developed wafer stability during the wafer dicing process resulting in the lower topside and backside chipping performance. While conventional wafer mounting technique, which does not apply any mounting tape on the wafer surface is expected to have higher vibration and movement during wafer dicing process resulting in higher chipping results. The illustration for both conventional and full sandwich mounting techniques after the mounting process can be referred to "Fig. 20" below.

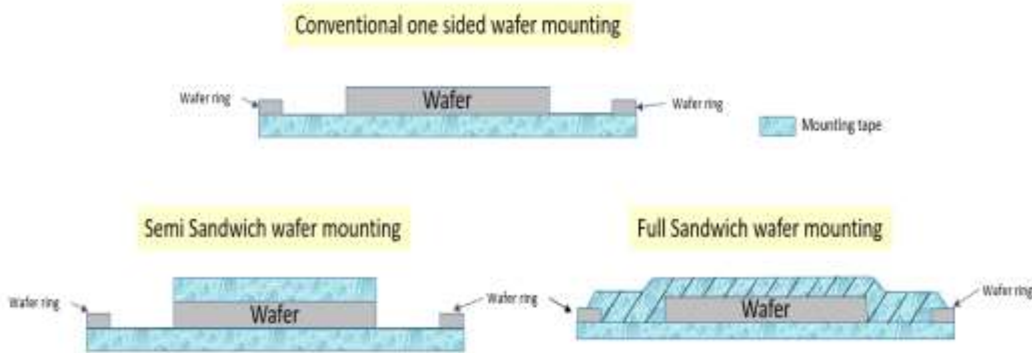

Fig. 20. Illustration of UV mounting on wafer surface for all wafer mounting techniques.

An in-depth investigation was undertaken to assess the crack performance subsequent to the dicing process implemented on the full sandwich method, utilizing UV mounting tape B. During the course of the inspection utilizing high power scope, no instances of crack-related concerns were identified for any of the mounting techniques employed. In order to validate these findings, additional examinations were conducted using a scanning electron microscope (SEM). The inspection using SEM was conducted to assess the occurrence of chipping on the topside and backside of the selected samples. The results revealed a higher frequency of chipping in the conventional mounting technique as compared to the full sandwich mounting technique. However, no evidence of crack occurrence was observed on either the topside or backside areas for both mounting techniques. "Fig. 21" provides an overview of the SEM findings at 100x, 400x, and 1000x magnifications. The silicon die chipping appearance on the full sandwich mounting technique showed improved chipping performance, indicating that chipping improvement could be accomplished with this technique.

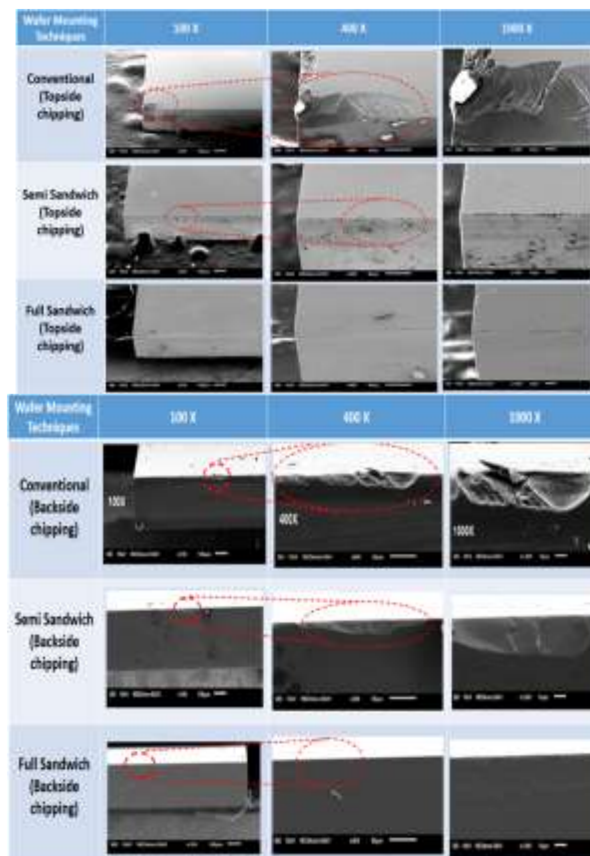

Fig. 21. Topside and backside chipping SEM results for conventional, semi and full sandwich wafer mounting.

From all the 30 samples that used for chipping measurement, the backside area then was analyzed to understand the chipping performance versus the grinding marks pattern. The surface roughness of silicon backside grinding marks was examined through the utilization of a 3D profilometer since it was reported will affect the die strength [31]. Upon observation, it was noted that two distinct types of grinding patterns were observed in the chipping areas. The presence of chipping, both parallel and perpendicular to the grind marks, was observed, as illustrated in "Fig. 22".

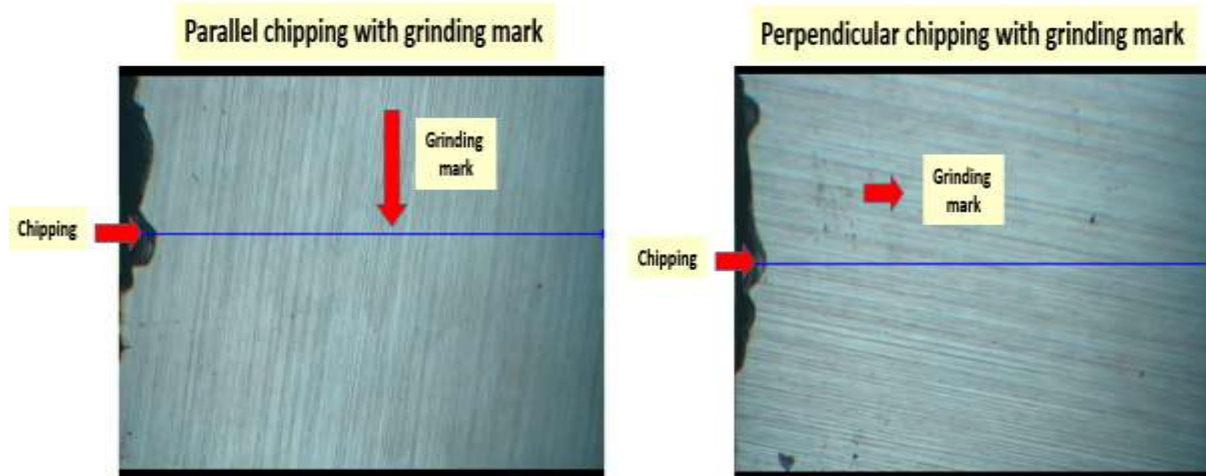

Fig. 22. Parallel and perpendicular chipping definition with grinding mark.

An analysis was conducted to investigate the influence of parallel and perpendicular grinding marks on surface roughness and their respective contributions to the chipping behavior. In order to evaluate the response of two chippings with respect to grinding marks, the arithmetical mean roughness value (Ra) and mean roughness depth (Rz) were measured. The parameter Ra represents the arithmetic mean of the surface roughness, while Rz quantifies the maximum vertical distance between the highest peak and lowest valley on the surface. The results of the silicon die chipping area with parallel grinding marks data were analyzed as per "Fig. 23" below. The surface roughness results on higher chipping area for parallel grinding marks showed "Ra = 3.1 µm" and "Rz = 23.5 µm".

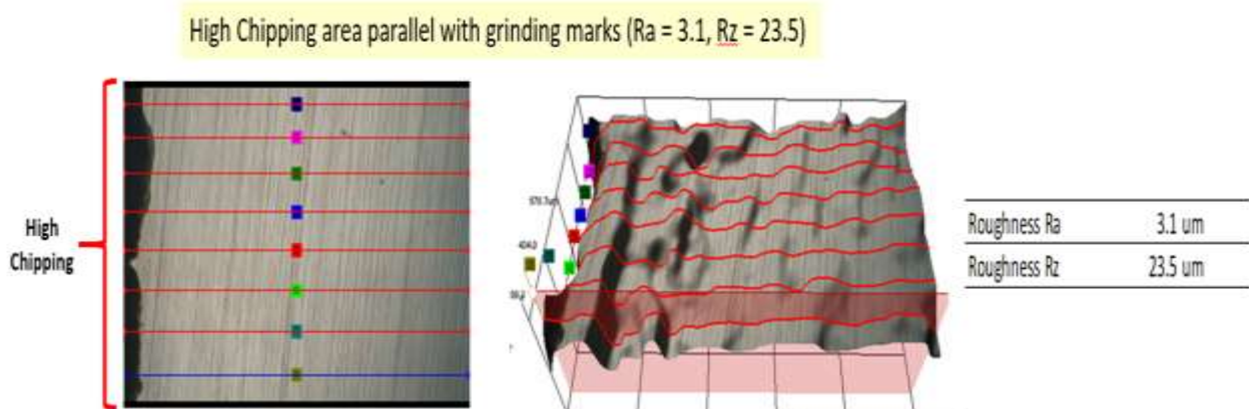

Fig. 23. Surface roughness on high chipping area with parallel grinding marks.

Then the silicon back grinding mark which is perpendicular to higher chipping conditions were analyzed as per Fig. 24 and observed the results "Ra = 0.8 µm" and "Rz = 5.2 µm". The low reading of the surface roughness on the perpendicular grinding mark is due to the non-contact lighting of the machine that was in line with the grinding mark causing a lower reading which was different from the parallel grinding that has more bulging area during measurement and causes higher reading. It was discovered that Hao Nan Li also utilized Ra and Rz for surface measurement monitoring [32] in their group analysis.

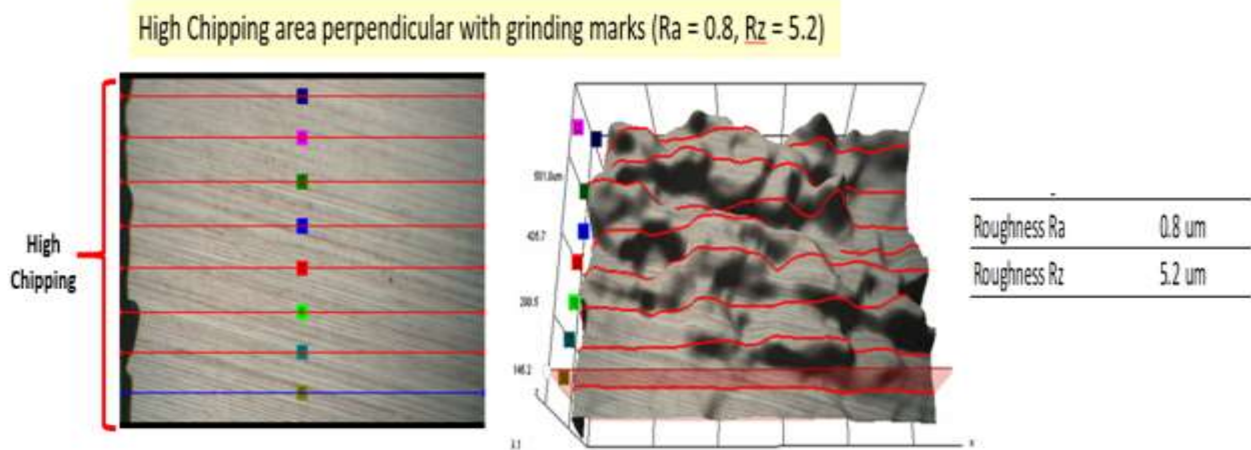

Fig. 24. Surface roughness on high chipping area with perpendicular grinding marks.

On the basis of 30 samples, a statistical test was conducted to determine if the parallel and perpendicular grinding marks had any effect on the chipping behavior. The test's statistical significance was determined using the T-test with a confidence level of 95%. According to the T-Test results depicted in “Fig. 25”, there is no significant difference between the chipping and grinding mark patterns.

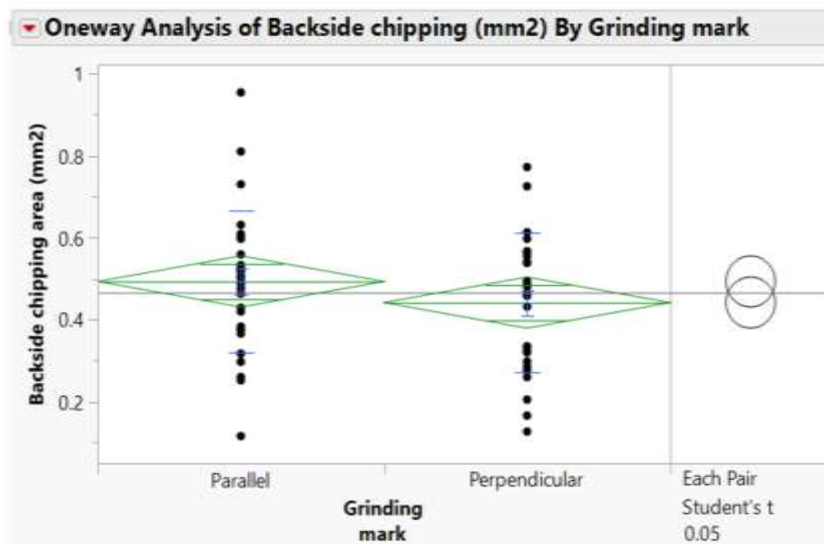

Fig. 25. T-Test results comparing parallel and perpendicular chipping toward grinding marks.

In a previous study conducted by Shang Gao [18], similar observations were made regarding the crystal orientation and chipping edge size at various locations. The results obtained in this study align with those reported by Gao, indicating no significant differences between the two sets of findings. Subsequently, a total of 30 samples were obtained for each conventional, semi, and full sandwich wafer mounting techniques. These samples were subjected to a 3-point bending test in order to examine the potential relationship between the improvement in chipping and the performance of die flexural strength. The test speed was standardized at 3 mm/min in order to obtain consistent and comparable flexural strength results for all die samples. These results can be found in “Fig. 26”, which serves as a point of reference for further analysis and discussion.

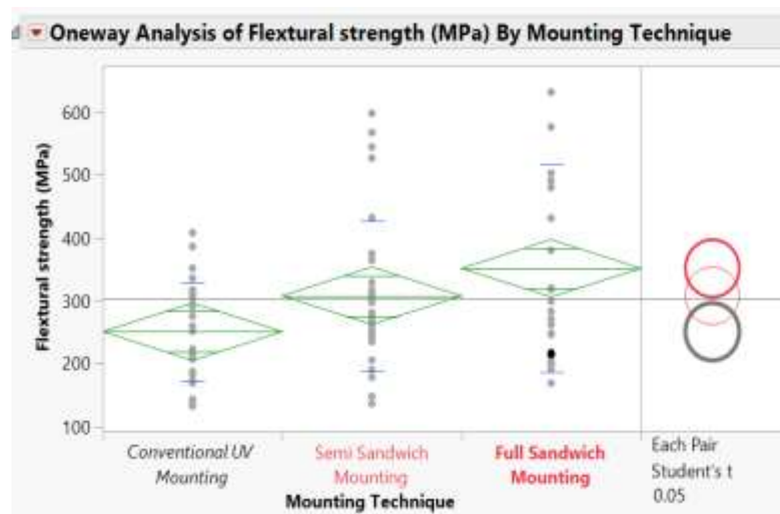

Fig. 26. Flexural strength performance based on mounting technique

"Fig. 26" demonstrates that the flexural strength of the full sandwich mounting technique has significantly greater results compared to the conventional mounting. This demonstrated that the maximal flexural strength of silicon die can be attained using a novel full sandwich mounting technique during wafer mounting process which produces lower chipping results as well. The utilisation of the conventional mounting technique has been observed with higher chipping during the dicing process. Consequently, this has led to a reduction in the flexural strength of the material. It is worth noting that this decrease in flexural strength is comparable to the outcomes observed in the case of Shinya Takyu [9], where higher levels of crack have been observed. This heightened chipping tendency may potentially lead to the formation of cracks and subsequently result in a decrease in flexural strength.

4. CONCLUSION

Based on the comprehensive analysis of the collected data, it can be deduced that the utilization action of the novel full sandwich mounting technique can lead to a notable improvement in the chipping performance of silicon dies and simultaneously enhance their flexural strength. Through a comparative analysis between the conventional mounting technique of silicon wafers, with no mounting tape on the wafer surface, and the novel semi and full sandwich wafer mounting technique, wherein mounting tapes were laminated onto the wafer surfaces, it becomes evident that the presence of tape imparts an additional cushioning effect. This effect reduces vibrations during the process of wafer dicing, thereby resulting in a noteworthy reduction in topside and backside chipping performance regardless of the grinding mark patterns.

The flexural strength of silicon dies was studied and found to have an inverse correlation with die-chipping performance after the full sandwich wafer mounting technique was implemented. The successful implementation of full sandwich wafer mounting necessitates careful consideration of the adhesion properties of UV mounting tape. The selection of UV tape should prioritize tape with a high adhesion "before UV curing" specification and a low "after UV curing" adhesion value in order to enhance the performance of chipping and surface peeling test results. The achievement of a minimized silicon die chipping area leads to an enhancement in flexural strength performance. However, further study is required on the usage of the UV mounting on the wafer surface towards full swing of manufacturing condition in order to understand the wafer dicing and wire bonding performance in the longer run. This is because the diamond blade loading during wafer dicing may increase when cutting on the additional layer of mounting tape which adhesive may stick on the diamond blade which may affect the chipping towards the active die circuitry area. The wire bonding process needs further monitoring towards the bonding ability since the concern of mounting tape adhesion remains on the bond pad area. However, the novel double-sided full sandwich wafer mounting technique has given an idea to the industries on how to improve the chipping and the flexural strength performance on the silicon wafers.

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Ethics. The authors declare that the present research work has fulfilled all relevant ethical guidelines required by COPE.

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REFERENCES

[1] JV. Lindroos, A. Lehto, T. Motooka, and M. Tilli, "**Handbook of Silicon Based MEMS Materials and Technologies**". 2010.

[2] J. G. Croissant, K. S. Butler, J. I. Zink, and C. J. Brinker, "**Synthetic amorphous silica nanoparticles: toxicity, biomedical and environmental implications**," Nat. Rev. Mater., vol. 5, no. 12, pp. 886–909, 2020, doi: 10.1038/s41578-020-0230-0.

[3] M. Paulasto-Kroâckel, M. Tilli, G. Ross, and H. Kuisma, "**Where is silicon based MEMS heading to? Handbook of Silicon Based MEMS Materials and Technologies**". pp. xxi–xxix, 2020, doi: 10.1016/B978-0-12-817786-0.00062-1.

[4] C. Control and C. July, "**Surface Position Detection Method of Silicon Melt in CZ Furnace**," pp. 5021–5026, 2016.

[5] Y. Zhao, X. Zhao, M. Roders, A. Gumyusenge, A. L. Ayzner, and J. Mei, "**Melt-Processing of Complementary Semiconducting Polymer Blends for High Performance Organic Transistors**," Adv. Mater., vol. 29, no. 6, pp. 1–7, 2017, doi: 10.1002/adma.201605056.

[6] F. Inoue et al., "**Morphological characterization and mechanical behavior by dicing and thinning on direct bonded Si wafer,**" J. Manuf. Process., vol. 58, no. January, pp. 811–818, 2020, doi: 10.1016/j.jmapro.2020.08.050.

[7] F. Inoue et al., "**Influence of Si wafer thinning processes on (sub)surface defects,**" Appl. Surf. Sci., vol. 404, pp. 82–87, 2017, doi: 10.1016/j.apsusc.2017.01.259.

[8] J. Shen, X. Zhu, J. Chen, P. Tao, and X. Wu, "**Investigation on the edge chipping in ultrasonic assisted sawing of monocrystalline silicon," Micromachines**," vol. 10, no. 9, 2019, doi: 10.3390/mi10090616.

[9] S. Takyu et al., "**A Novel Dicing Technologies for WLCSP Using Stealth Dicing through Dicing Tape and Back Side Protection-Film**," Proc. - Electron. Components Technol. Conf., vol. 2016-Augus, pp. 1241–1246, 2016, doi: 10.1109/ECTC.2016.138.

[10] D. Xue, C. Zhong, E. Zhang, W. Jiang, and C. Zhang, "**Die chipping FDC development at wafer saw process**," 2021 22nd Int. Conf. Electron. Packag. Technol. ICEPT 2021, 2021, doi: 10.1109/ICEPT52650.2021.9568039.

[11] M. Xue, T. Chen, X. Zhang, L. Gao, and M. Li, "**Effect of Blade dicing parameters on Die Strength**," Proc. - 2018 19th Int. Conf. Electron. Packag. Technol. ICEPT 2018, pp. 180–183, 2018, doi: 10.1109/ICEPT.2018.8480532.

[12] H. Zhang, W. F. Wang, and P. Y. Huang, "**Optimization of Wafer Dicing-Saw to Reduce the Chipping Defect by Using the Response Surface Methodology**," 2022 China Semicond. Technol. Int. Conf. CSTIC 2022, pp. 24–27, 2022, doi: 10.1109/CSTIC55103.2022.9856868.

[13] T. J. Su, Y. F. Chen, J. C. Cheng, and C. L. Chiu, "**An artificial neural network approach for wafer dicing saw quality prediction,**" Microelectronics Reliability, vol. 91. pp. 257–261, 2018, doi: 10.1016/j.microrel.2018.10.013.

[14] K. J. Kim, "**Development of waxless wafer mounting system for silicon wafer polishing process**," Appl. Mech. Mater., vol. 339, pp. 762–765, 2013, doi: 10.4028/www.scientific.net/AMM.339.762.

[15] M. K. Bin Zainal, A. Bin Abdul Aziz, and V. Ramalingam, "**Backside Chipping Investigation & Improvement on TiNiVAg Back Metal Silicon Die**," Proc. IEEE/CPMT Int. Electron. Manuf. Technol. Symp., vol. 2022-Octob, pp. 0–3, 2022, doi: 10.1109/IEMT55343.2022.9969494.

[16] M. A. Mendoza, A. G. S. Gablan, H. L. Tierra, and F. R. I. Gomez, "**Process Simplification on Integration of UV Cure Machine with Tape Saw Singulation**," J. Eng. Res. Reports, vol. 20, no. 10, pp. 1–5, 2021, doi: 10.9734/jerr/2021/v20i1017382.

[17] C. P. Orlando, J. L. Goodrich, and E. L. Gosselin, "**Backside Mounting Procedures for Semiconductor Wafer Processing**," 2001.

[18] C. S. Premachandran et al., "**Wafer level high temperature reliability study by backside probing f or a 50um thin TSV wafer,**" Proc. - Electron. Components Technol. Conf., vol. 2015-July, pp. 2144–2148, 2015, doi: 10.1109/ECTC.2015.7159899.

[19] B. C. S. Bacquian, "**Dicing before Grinding : A Robust Wafer Thinning and Dicing Technology,**" vol. 11, no. 4, pp. 25–34, 2020, doi: 10.9734/JERR/2020/v11i417067.

[20] Fabiana Meijon Fadul, "**Analysis of Crystalline in GaN Epitaxial Layer after the Wafer Dicing Process**," vol. 1593, pp. 1–6, 2019.

[21] H. Sekhar et al., "**Mechanical strength problem of thin silicon wafers (120 and 140 µm) cut with thinner diamond wires**

(Si kerf 120 → 100 µm) for photovoltaic use," Materials Science in Semiconductor Processing, vol. 119. 2020, doi: 10.1016/j.mssp.2020.105209.

[22] H. Liu, T. Yang, X. Tian, S. Chen, F. Dong, and J. Han, "**Iterative method for obtaining nonuniform grinding-induced residual stress distribution of silicon wafers based on global deformation**," Mater. Sci. Semicond. Process., vol. 150, no. July, p. 106971, 2022, doi: 10.1016/j.mssp.2022.106971.

[23] Z. M. Chang and H. M. Ler, "**Effect of Wafer Back Metal Thickness and Surface Roughness towards Backend Assembly Processes,**" Proc. IEEE/CPMT Int. Electron. Manuf. Technol. Symp., vol. 2022-Octob, 2022, doi: 10.1109/IEMT55343.2022.9969478.

[24] H. Sekhar, T. Fukuda, K. Tanahashi, and H. Takato, "**The impact of silicon brick polishing on thin (120 µm) silicon wafer sawing yields and fracture strengths in diamond-wire sawing**," Mater. Sci. Semicond. Process., vol. 105, no. September 2019, p. 104751, 2020, doi: 10.1016/j.mssp.2019.104751.

[25] X. Wu, F. Ren, and H. Ma, "**The effect of surface morphology on the peel performance of UV-induced adhesion-reducing adhesives The effect of surface morphology on the peel performance of UV- induced adhesion-reducing adhesives**," 2022.

[26] H. Liu, Y. Wei, J. Wang, and S. Xu, "**Investigation of single cut process in mechanical dicing for thick metal wafer**," 2016 17th Int. Conf. Electron. Packag. Technol. ICEPT 2016, pp. 26–30, 2016, doi: 10.1109/ICEPT.2016.7583083.

[27] Gao, R. Kang, Z. Dong, and B. Zhang, "**Edge chipping of silicon wafers in diamond grinding**," International Journal of Machine Tools and Manufacture, vol. 64. pp. 31–37, 2013, doi: 10.1016/j.ijmachtools.2012.08.002.

[28] M. Y. Tsai and P. S. Huang, "**Correction factors to strength of thin silicon die in three- and four-point bending tests due to nonlinear effects**," Microelectron. Reliab., vol. 128, no. September 2021, p. 114424, 2022, doi: 10.1016/j.microrel.2021.114424.

[29] J. Talledo, "**Comparison of Silicon Die Strength Using Different Loading Anvil Shapes**," J. Eng. Res. Reports, vol. 20, no. 6, pp. 17–23, 2021, doi: 10.9734/jerr/2021/v20i617323.

[30] J. Talledo, "**Effect of Silicon Die Condition on the Breaking Load Performance of a Dam and Fill Semiconductor Package**," J. Eng. Res. Reports, vol. 20, no. 6, pp. 64–69, 2021, doi: 10.9734/jerr/2021/v20i617328.

[31] S. E. Nikitin et al., "**Fracture strength of silicon solar wafers with different surface textures**," Mater. Sci. Semicond. Process., vol. 140, no. November 2021, p. 106386, 2022, doi: 10.1016/j.mssp.2021.106386.

[32] H. N. Li, T. B. Yu, L. Da Zhu, and W. S. Wang, "**Analytical modeling of ground surface topography in monocrystalline silicon grinding considering the ductile-regime effect**," Arch. Civ. Mech. Eng., vol. 17, no. 4, pp. 880–893, 2017, doi: 10.1016/j.acme.2017.03.010.