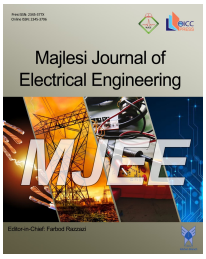

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Triple gain switched-capacitor based inverter with reduced component count

Gangadhar Dhal[1], Kasinath Jena[2,*], Krishna Kumar Gupta[3], Chinmoy Kumar Panigrahi[1], Dhananjay Kumar[4], Pradeep Kumar Sahu[1], Lipika Nanda[1]

[1]*School of Electrical Engineering, KIIT University, Bhubaneswar, India.*
[2]*Department of Electrical and Electronics Engineering, ARKA JAIN University, Jharkhand, India.*
[3]*Department of Electrical & Instrumentation Engineering Thapar Institute of Engineering & Technology Patiala, India.*
[4]*Department of Electrical Engg, Government Engineering College, Siwan, India.*

[*]**Corresponding author:** kasi.jena@gmail.com

Original Research

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Abstract:

Multilevel inverters (MLIs) are commonly used in photovoltaic power stations, wind farms, and other forms of renewable energy generation. This study presents a new novel multi-gain switched capacitor (SC) based structural approach. The voltage gain of the proposed design (PD) can be increased threefold by utilizing two switching capacitors and nine switches. Additional significant benefits of the PD include lower voltage stress, an inherent self-balancing of the capacitor voltage, and a minimal amount of switching components. A backside H-bridge is not required to generate negative voltage levels. The PD provides a detailed explanation of the structural analysis, the self-balancing mechanism, the optimum capacitance value, and the control approach. In order to highlight the advantages of the PD, a fair comparison is presented with the most recent seven-level single-source topologies. Finally, Simulation results confirm the accuracy of the theoretical analysis and a prototype has been constructed to demonstrate that the practical findings are doable and successful, with the efficiency tested reaching 96.95%.

Keywords: Cost-function; Multilevel inverter; Self-balanced; Switched capacitor; Part count

1. Introduction

The focus on addressing the growing energy and environmental pollution problems in recent years has given significant attention to the research, development, and implementation of clean and renewable energy sources. The increasing adoption of renewable energy sources, like wind and solar panels, is primarily due to their reliability, minimal environmental impact, and easy accessibility. The MLIs are crucial in converting power in a solar power-generating system. MLIs possess notable characteristics, including decreased dv/dt stress, enhanced waveform, increased efficiency, and simplified filtering circuitry [1]. Traditional MLIs are classified into three types: NPC (*neutral point clamped*), FC (*flying capacitor*), and CHB (*cascade H-Bridge*). These inverters are widely used for commercial and industrial applications. Nevertheless, these technologies exhibit several limitations, such as the absence of boosting capability, the challenging task of capacitor voltage balancing in FC and NPC topologies, and the requirement for multiple independent DC sources in CHB configurations [2, 3]. These drawbacks are significant constraints, hindering their extensive adoption in various applications.

A high-quality power supply and a high-voltage input boost are crucial for renewable energy applications. Switching capacitor-based boost topologies were developed to use renewable energy sources for applications that require a greater voltage magnitude. The output voltage is increased above the supply voltage through the boosting process. The series/parallel technique enhances the capability of voltage gain in SC topologies. The output voltage rises when many switched capacitor units are connected in series, with or without power.

One common approach among several families of updated MLIs is using SC-based circuits. The SCMLI offers various advantages compared to its competitors, such as its functioning without an inductor or transformer, its capacity to raise voltage, and its inherent capability to balance the

voltage of its capacitors [4–7]. The shared feature of these classes of topologies is the presence of a two-stage structure. A switched-capacitor DC-DC converter is used in the first stage to generate positive voltages, and an H-bridge is used in the second stage to change the polarity of the output voltage. The switching components experience a higher peak voltage when an H-Bridge is present. The situation is unsavory.

In the paper [8], the authors present a single-source boost inverter design. With only 19 switches and three capacitors, this design yields a voltage gain of 4. The article introduces a novel MLI topology [9]. Using a voltage-boosting gain of 3, the proposed approach may generate seven separate voltage levels from a single DC source. In addition, the design limits the voltage across each power switch to the DC source voltage, which is halved from the maximum allowable voltage. The design also has no trouble balancing voltage because capacitor charges are automatically balanced.

Within the new family of MLIs presented in [10], generating seven distinct voltages with only one or two floating capacitors and ten power switches is possible. Since the PIV of all power switches is less than the load voltage, increasing the output voltage does not place any switches under high-voltage stress. By utilizing two inverters of the T-type, an ANPC topology can be created [11]. The integration of two self-balancing floating capacitors yields a 1.5-volt voltage boost. In addition to that, the architecture can produce seven different voltage levels.

The authors of [12] present a 7-level inverter based on SC and employ a hybrid PWM algorithm to enhance the inverter efficiency. The 7-level inverter circuit features can be adjusted to decrease capacitor voltage ripples. The modulation and perfect design significantly reduce the capacitance of the two capacitors employed in this MLI, enhancing the output voltage quality. A significant limitation of the system is the elevated voltage stress experienced by the four power switches in the second stage. Most published papers on SC-based MLIs have thus far concentrated on topology studies. By optimizing the series/parallel SC circuit arrangement, the work [13] created a new topology of MLIs, allowing for fewer components to achieve higher output levels. An inverter with 13 levels and a gain of six times can be built quickly using a single series/parallel SC unit. A 7-level inverter, demonstrated in [14], can produce an output voltage three times higher than the input voltage. The SCMLIs published in [15, 16] enable a 3-x boost, resulting in a 7-level output voltage. Nevertheless, their TSV and PIV are higher. The paper [17] introduces a novel SCMLI using a single DC voltage source. This design works exceptionally well for low-voltage applications involving renewable sources of energy. By utilizing two SC and ten switches, obtaining a 7-level output voltage with a voltage gain of three is feasible. Reference [18] suggests using a 7-level inverter with a single DC supply. It can extend itself in a cascading fashion to produce even more levels. At the same time, the architecture does not require a sensor to energize the capacitor. To achieve 7-levels of output voltage, the SCMLI described in the paper [19] uses reduced devices and has a boosting factor 3. However, their TSV and PIV are greater. However, the topologies [17–19] require more power components. To minimize additional SC requirements, they are integrated into a unified design [20]. To accomplish voltage gain by a factor of two, another 5-level boost inverter uses two SC in conjunction with eight switching devices [21]. Adding a rear half bridge to an SC in a series/parallel configuration is one such topology, as presented in reference [22]. High voltage applications are limited because switches used in cross connections must have a voltage rating equivalent to the highest output voltage. The article [23] provides an extra architecture for a boost inverter that uses a single source. The configuration uses a trio of capacitors and twelve switches to boost the voltage by a factor of three, resulting in a seven-level output voltage. Although [24] has a fairly basic design, it always uses a series connection between two capacitors to split the input voltage. If the currents generated during the positive and negative halves of a cycle are not identical, an imbalance in the resulting voltage across the capacitors will occur. This issue was addressed in [25]; however, further switches are needed for full implementation. This article [26] introduces a six-level SCMLI achieving 2.5x VG from a single DC source, designed for compact, transformerless PV systems with minimized line filters. The MLI features capacitor voltage balance, reduced harmonics, and closed-loop control for effective grid integration, achieving a peak efficiency of 95.79%. This article [27] proposes a five-level SC inverter for PV applications designed to eliminate leakage current by connecting the DC bus directly to the grid neutral. The topology supports self-voltage balancing, reactive power processing, and full DC-bus utilization. Simulation and experiments demonstrate its practical advantages over conventional inverters. This article [28] presents a nine-level ANSCMLI with a minimized capacitor charging current, enhancing its sensible use. A modified switching sequence reduces switching loss, improving efficiency to 98.03% at 583.91 W. Experimental results confirm stable capacitor voltages and reduced losses under various loads. The article [29] introduces a six-level transformerless inverter for grid-connected PV systems, addressing leakage current issues and offering VB without an added boost converter. Key features include reduced filter size, lower THD, and full reactive power support. A 770 W lab prototype validates its performance and practical feasibility. This article [30] proposes a flexible multilevel topology for open-end winding motor drives, similar to CHB inverters, combining three-phase and single-phase HB inverters. The modular design allows easy voltage level extension, enabling higher motor voltages or lower DC voltage use. Experimental tests validate its performance and compatibility with SPWM modulation. A voltage gain of just 1.5 is achieved by the seven-level MLI described in [31] and [32] using ten switches, two diodes, and three capacitors.

Nevertheless, it requires components with a high rating due to its high TSVpu. Achieving voltage increases of 2.0 and 1.0 are also detailed in [33] and [34] for the common ground five-level MLI. This study presents a single-source, high-voltage-gain SC-MLI to overcome these restrictions. With

its flexible architecture, the suggested six-level SC-MLI can handle various tasks.

The literature above clarifies that the newly designed 7-level SCML topologies have several limitations. Some of these difficulties are increased voltage stress, decreased boosting factors, and more active and passive components. Here are the key reasons behind the PD:

1. A decreasing number of semiconductor devices are required.
2. The switches have reduced voltage stress.
3. Utilizing a single direct current source makes it feasible to achieve a maximum voltage gain of three.
4. The capacitor voltages are inherently self-balanced.
5. Minimal switching and conduction losses are achieved since half of the switches can be employed with any voltage.
6. The creation of polarity does not necessitate the use of an H-bridge.

Following this section, the recommended paper is organized in the following manner: In section 2, the PD is explained in detail, including its operating principle, self-balancing mechanism, and the determination of optimum capacitance values. Section 3 illustrates a technique of modulation. Section 4 covers loss analysis. Section 5 includes simulation and experimental assessments to guarantee the viability and performance. Section 6 offers a comprehensive evaluation of the PD. Lastly, this paper finishes with section 7.

2. Proposed SC design

(A) Design description

The design representation of the multi-gain 7-level topology that is based on the SC approach is shown in Fig. 1. Two capacitors denoted as (C_1, and C_2), a single-input DC source with a magnitude of V_{dc}, and nine active power switches, denoted as (S_1 to S_9) are the components that comprise the proposed design (PD). In this case, the switches are of two different types: standard IGBTs with antiparallel diode and IGBTs without antiparallel diode (also known as reverse blocking technology).

In order to generate seven-level (0, $\pm 1V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$) alternating output voltage (v_0), as well as three times the voltage-boosting capability $3V_{DC}$, a single input DC source of magnitude V_{DC} and two switched capacitors C_1 and C_2 are utilized. The switching pattern for both positive and negative levels is illustrated in Table 1. The first capacitor, C_1, has been charged to V_{DC} via S_1 and S_5, while the second capacitor, C_2, being charged to $2V_{DC}$ via S_2 and S_4, respectively.

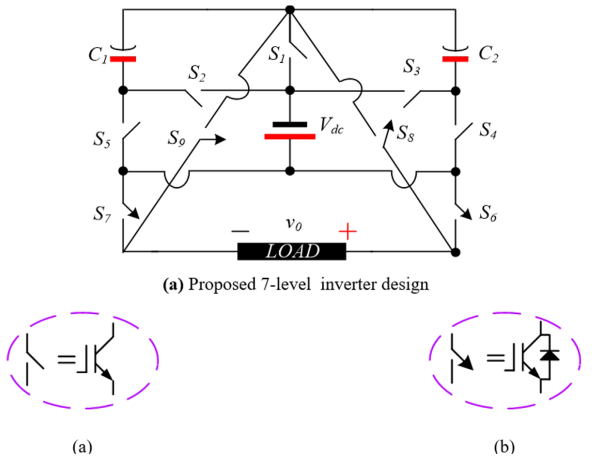

Figure 1. Illustrates two configurations: (a) proposed 7-level inverter design; (b) a switch without an anti-parallel diode and (c) switches equipped with antiparallel diodes.

Table 1. Switching pattern of PD.

State	Active switches	v_0	C_1	C_2
γ_1	$S_1S_5S_6S_7$	0	Δ	-
γ_2	$S_1S_5S_6S_9$	$1V_{dc}$	Δ	-
γ_3	$S_2S_4S_6S_9$	$2V_{dc}$	∇	Δ
γ_4	$S_3S_6S_9$	$3V_{dc}$	-	∇
γ_5	$S_1S_5S_7S_8$	$-1V_{dc}$	Δ	-
γ_6	$S_2S_4S_7S_8$	$-2V_{dc}$	∇	Δ
γ_7	$S_3S_7S_8$	$-3V_{dc}$	-	∇

Δ = charging, ∇ = discharging, "-" = idle, v_0 = output voltage

A blue and red dotted arrow headline represents the charging path of the capacitors and the voltage level path. The voltage stress on the switching components is listed in Table 2.

Table 2. Voltage stress.

Switches	Stress
S_4, S_5	$\mathbf{1V_{dc}}$
$S_1, S_2S_3S_6, S_7$	$\mathbf{2V_{dc}}$
S_8, S_9	$\mathbf{3V_{dc}}$

(B) Voltage level explanation

This section presents the results of an investigation of the various potential voltage levels for the positive half cycle of the PD, as follows:

State-γ_1($v_0 = \mathbf{0}$): In this state, the load is effectively bypassed by the activating switches the S_6 ,and S_7. C_1 is being charged to V_{dc} by S_1 and S_5, as shown in Fig. 2 (a).

State-γ_2($v_0 = \mathbf{+1V_{dc}}$): By turning on S_1- S_6- S_9 all at once, the input voltage is accessible at the load terminal under this switching condition. C_1 is being charged to V_{dc} by S_1 and S_5 as shown in Fig. 2 (b).

State-γ_3($v_0 = \mathbf{+2V_{dc}}$): In this configuration, $v_0 = +2V_{dc}$ is attained by connecting capacitor C_1 to the input source. C_2 is charged through $C_1 - S_2 - V_{dc} - S_4 - C_2$ to $2V_{dc}$ as shown in Fig. 2 (c).

State-γ_4($v_0 = \mathbf{+3V_{dc}}$): As illustrated in Fig. 2 (d), the output voltage $v_0 = +3V_{dc}$ across the load terminal is achieved in this state by connecting the capacitor C_2 in series with the input source. Referring to Fig. 2 (e-g), the approach may perform an analogous analysis for the negative voltage level and their corresponding circuit.

(C) Capacitance optimization and self-balancing mechanism

As illustrated in figure 2, capacitor C_1 charges when the voltage level is $\pm 1V_{dc}$, and 0 while C_2 charges to $2V_{dc}$ when the voltage level is $\pm 2V_{dc}$. Capacitors C_1 and C_2 discharge their stored energy when the voltage level reaches $\pm 2V_{dc}$

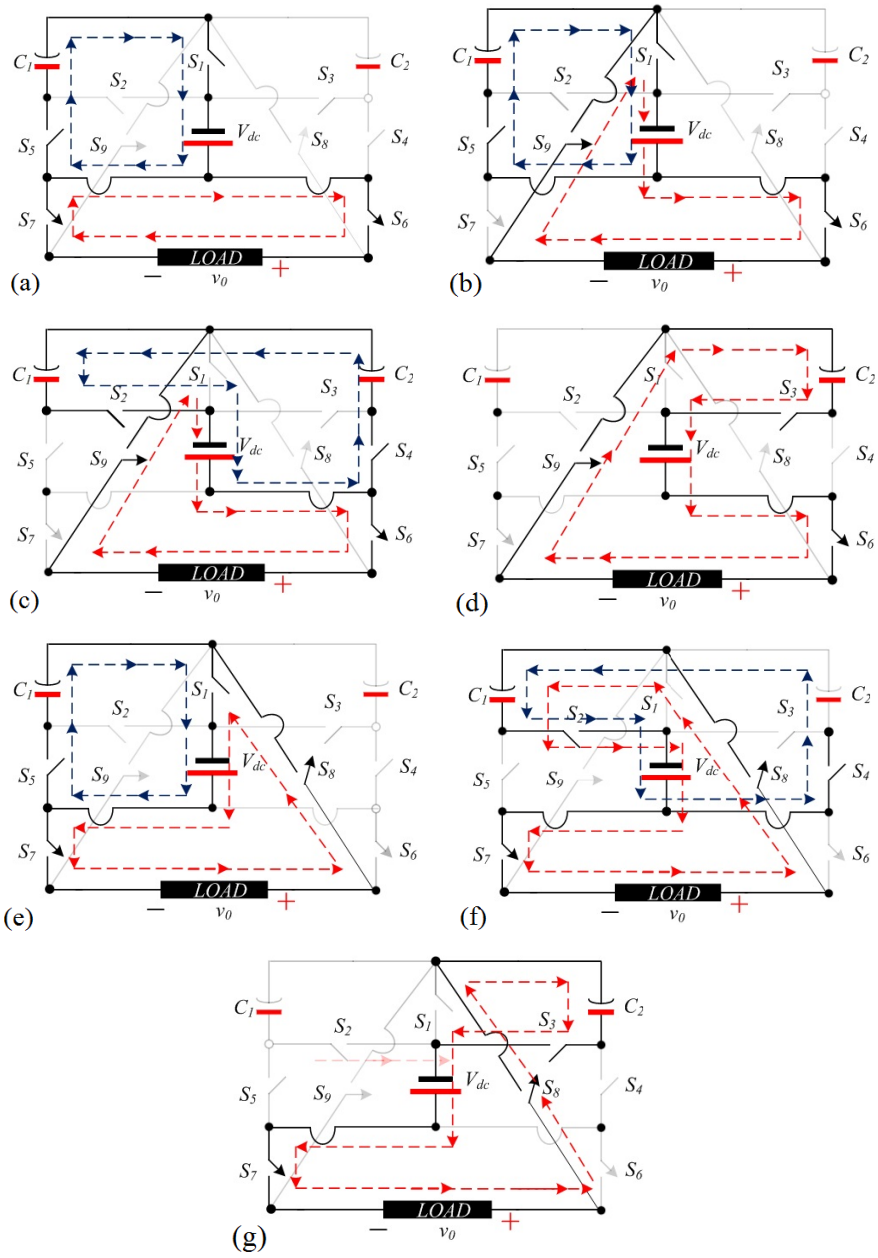

Figure 2. Different switching states (a) $v_0 = 0$, (b) $v_0 = V_{dc}$, (c) $v_0 = 2V_{dc}$, (d) $v_0 = +3V_{dc}$, (e) $v_0 = -1V_{dc}$, (f) $v_0 = -2V_{dc}$, (g) $v_0 = -3V_{dc}$.

and $\pm 3V_{dc}$ respectively. The continuous charging and discharging process throughout one fundamental voltage cycle allows the capacitor to automatically self-balance, regardless of the load [6].

Capacitors in SCMLIs serve a crucial function in transmitting and converting electrical power. Their voltage fluctuations should be kept under control. The capacitance, load value, and discharging times of capacitors are all interconnected and contribute to the voltage ripple they produce. The output voltage quality, ripple losses, and inverter efficiency can all benefit from lower voltage ripple. The suggested seven-level inverter utilizes two capacitors with identical capacitance. Two capacitors were chosen using the same criteria. Therefore, capacitor voltage ripples are crucial in designing SC inverters and must be within acceptable limits. Some variables that affect

$$C_i \geq \frac{\Delta Q_{Ci}}{\Delta V_{Ci}} \tag{1}$$

$$\Delta Q_{C1} = \frac{1}{2\pi f} \int_{\theta_1}^{\pi-\theta_1} I_P \sin(\omega\theta) d\theta \tag{2}$$

$$\Delta Q_{C2} = \frac{1}{2\pi f} \int_{\theta_2}^{\pi-\theta_2} I_P \sin(\omega\theta) d\theta \tag{3}$$

these ripples are the capacitance, the maximum discharge period of the capacitors, and the load value. The longest discharge times for capacitors C_1 and C_2 are shown in Fig. 3 (b) as$(\theta_1, \pi - \theta_1)(\theta_2, \pi - \theta_2)$ respectively. Consequently, the discharge amounts for capacitors C_1 and C_2 can be calculated as:

A fully resistive load yields a voltage ripple of;

$$\Delta V_{C1} = \frac{1}{2\pi f c_1} \int_{\theta_1}^{\pi-\theta_1} \frac{2V_{dc}}{R} d\theta \tag{4}$$

$$\Delta V_{C1} = \frac{V_{dc}}{\pi f R C_1} [\pi - 2\theta_1] \tag{5}$$

$$\Delta V_{C2} = \frac{3V_{dc}}{2\pi f R C_2} [\pi - 2\theta_2] \tag{6}$$

The conducting angle (θ_1, θ_2) can be calculated as:

$$\theta_1 = \frac{\sin^{-1}(\frac{1A_C}{A_{ref}})}{2\pi f} \tag{7}$$

$$\theta_2 = \frac{\sin^{-1}(\frac{2A_C}{A_{ref}})}{2\pi f} \tag{8}$$

The capacitance value can be determined as follows:

$$C_1 \geq \frac{V_{dc}}{\pi f R \Delta V_{C1}} [\pi - 2\theta_1] \tag{9}$$

$$C_2 \geq \frac{3V_{dc}}{2\pi f R \Delta V_{C2}} [\pi - 2\theta_2] \tag{10}$$

3. Switching strategy

The switching signals in this work are generated using phase-disposition pulse width modulation(PD-PWM), **a** subset of carrier wave PWM. Due to its ease of construction, this method streamlines the control circuit.

By comparing carrier waves with a sinusoidal wave, generating the pulse required for the switches is possible. A distinct logic combination of these pulses governs each switch on/off state. Fig. 3 (a) illustrates the modulation strategy used for the positive half of the cycle, and a comparable method is employed for the opposite side of the cycle. Each carrier is transmitted with a consistent amplitude (A_C) and frequency (f_C). A sinusoidal modulation wave is characterized by its output frequency (f_0) and reference amplitude (A_{ref}). Table 3 illustrates the correlation between the modulation index and the resultant output level.

4. Loss analysis

There are three distinct types of assessments performed on substantial power losses in SCMLIs. Here is a detailed analysis of these losses.

(A) Switching losses

During the transition between states, power is lost, referred to as switching loss. Consequently, the total switching losses can be written as [3].

$$P_{sw,loss} = \frac{f_{sw}}{6} V_{off} i(t) [t_{on} + t_{off}] \tag{11}$$

The switching frequency is denoted by f_{sw}, the current during conduction is denoted by $i(t)$, the blocking voltage is V_{off}, and the times t_{on}, and t_{off} are the times the switch is on and off, respectively.

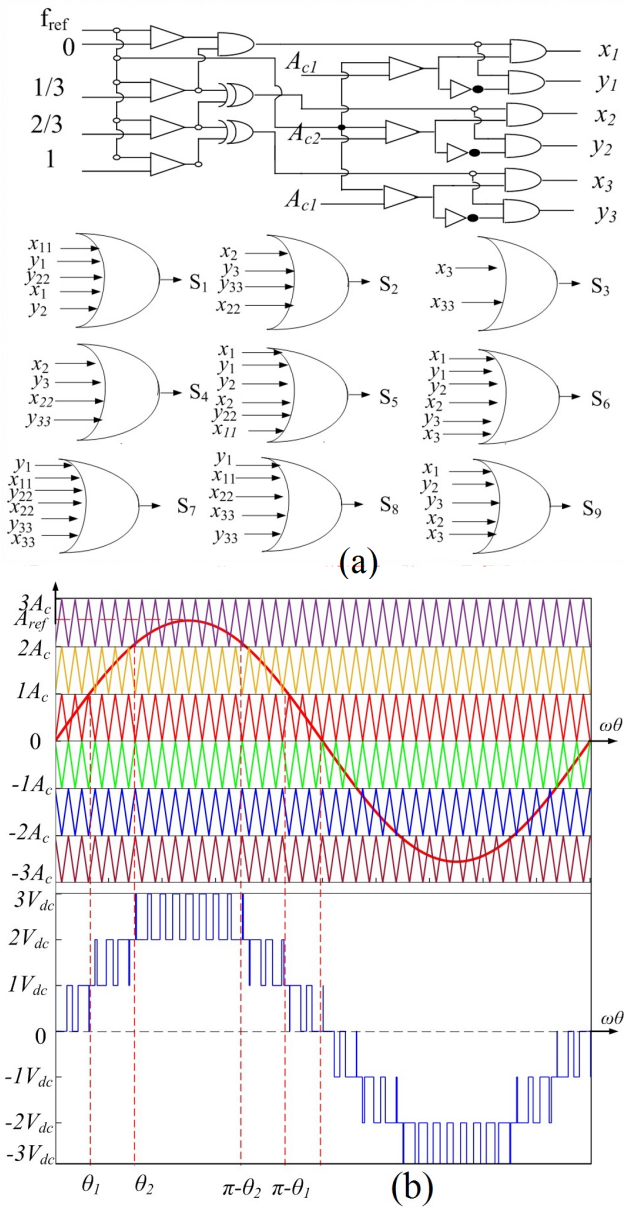

Figure 3. (a) Modulation scheme (b) Reference, carrier signal & load voltage.

(B) Conduction losses

The phenomenon of power dissipated into heat due to the intrinsic resistance or on-state voltage drop of electronic components, such as diodes and transistors, is called conduction loss.

$$P_{con,loss,sw} = V_{on,sw} I_{sw,avg} + R_{on,sw} I^2_{sw,rms} \tag{12}$$

$$P_{con,loss,d} = V_{on,d} I_{d,avg} + R_{on,d} I^2_{d,rms} \tag{13}$$

Table 3. Output level and modulation index parenthesis.

Modulation index (M)	Output level
0<M<1/3	3
1/3<M<2/3	5
2/3<M<1	7

On state, transistor and diode voltage drops are $V_{on,sw}$,$V_{on,d}$ respectively.
$I_{sw,avg}, I_{sw,rms}$: average and RMS current of transistor respectively.
On-state transistor and diode resistances: $R_{on,sw}, R_{on,d}$, respectively.

(C) Ripple losses (P_{rip})

With the proposed inverter, switched capacitors supply voltage and current to the load simultaneously. It is primarily the input voltage V_{dc} that determines their output voltages. However, the output current affects them as well. The discharge durations of different capacitors are not identical, and the output current fluctuates with time, all of which contribute to the fact that the voltage ripples produced by the capacitors can seem very different. The fluctuating voltage of the capacitor brings on these losses, and the equation that may be used to determine them is [5];

$$P_{rip} = fC_i\Delta V_{Ci}^2 \tag{14}$$

5. Results and discussion

(A) Simulation result verification

To authenticate the theoretical concept behind the PD, MATLAB/Simulink software was employed. The parameters used for the MATLAB/Simulink model are tabulated in Table 4.
Fig. 4 shows the simulation outcomes for the PD. Under steady-state analysis, it can be observed that the PD generates a 7-level voltage with equal steps, as shown in Fig. 4 (a). Each step has a magnitude of 50 V. The waveform maximum values are 150 V. The capacitors C_1 and C_2 are balanced within their pre-determined ranges.

Table 4. Simulation and experiment model parameters.

Model parameters	Values
Input source (V_{dc})	50V
Switching frequency	200 Hz, 5 kHz
Fundamental frequency	50 Hz
Modulation index (M)	0.95,0.5,0.2
Capacitors (C_1,C_2)	470 μF, 1600 μF
Loads	40 Ω, 120 mH
Switches (IGBTs)	FGW30XS65, FGW30X65C

The performance of an inverter depends on its ability to adapt to varying inputs and outputs. The following simulations have further assessed PD performance in dynamic situations.
The simulation results in Fig. 4 (b) demonstrate that the output voltage level and the capacitor balancing remain stable despite sudden changes in the load.
Sensors or additional strategies are unnecessary since the voltage on capacitors C_1 and C_2 is naturally balanced at 50 V and 100 V, respectively.
These results illustrate the inverter performance throughout a variety of loads. The proposed inverter is flexible enough to adjust to new parameters when the modulation wave frequency shifts. Fig. 4 (c) illustrates the relationship between output voltage and current concerning frequency. The inverter can transition from 200 to 5000 Hz with a rapid transient response.
Furthermore, Fig. 4 (d) displays the changed value of "M" for the PD in the simulation. "M" is modified two times between about 0.1 and 0.14 seconds. The number of output

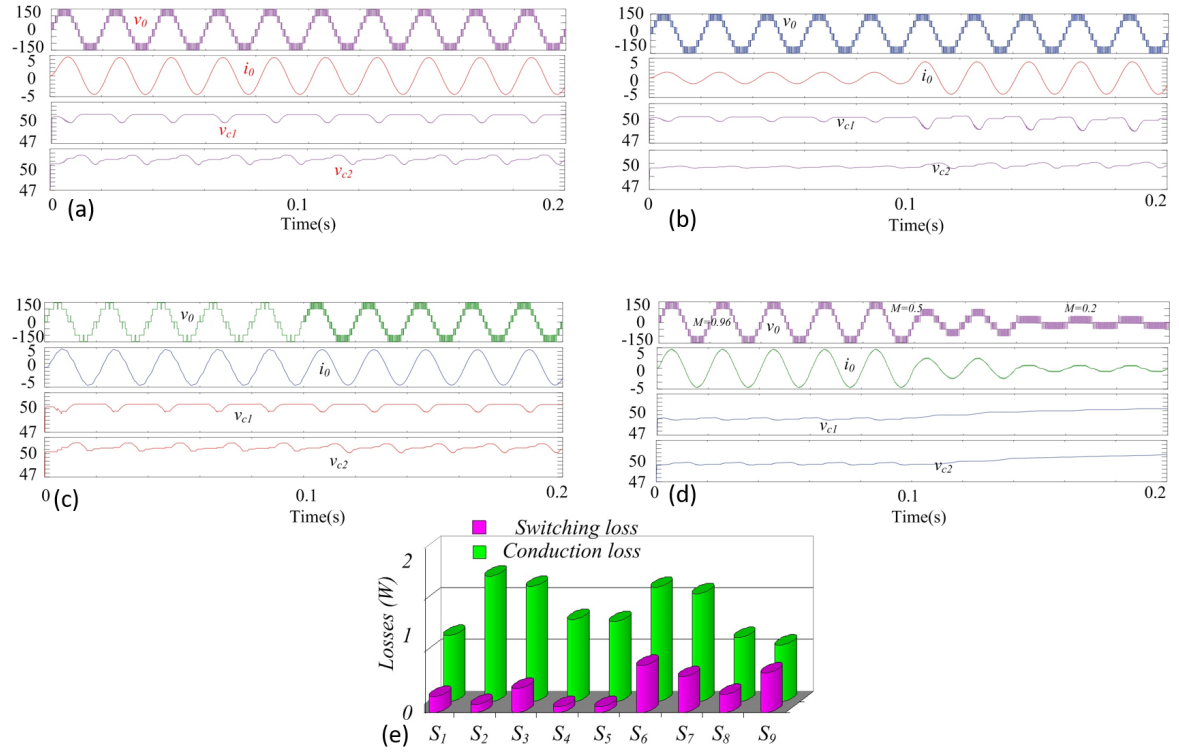

Figure 4. Results: (a) constant load, (b) variation load, (c) frequency variation, (d) modulation index variation, (e) losses distribution graph.

levels also changes alongside the alterations in "M". The natural equilibrium of the capacitors does not shift regardless of whether or not "M" is set to a value of 0.95, 0.5, or 0.2. The modulation will not affect the practicability of maintaining a natural equilibrium between C_1 and C_2. Consequently, the natural balance can be applied to the suggested topology with various output levels. The rapid convergence of transient processes demonstrates the superior dynamic performance of the proposed inverter.

To assess its losses, the PD has been simulated using Plexim software. Fig. 4 (e) displays the distribution of losses as a graph. The ripple loss is determined to be 2.115 W based on the peak-to-peak ripple values of the capacitors, which are 2.6 V and 3 V. As a result, the PD has an overall efficiency of 97.3%.

(B) Experimental validation

Stand-alone mode:

Table 4 presents a concise overview of the specifications of the laboratory prototype (Fig. 5). The PD has undergone laboratory testing and has demonstrated proper functionality under various settings. Fig. 5 (a-e) presents the experimental outcomes under multiple conditions.

The steady-state performance of the PD system is illustrated in Fig. 5 (a). The PD generates a 7-level output with a maximum voltage of 150 V based on observations. Additionally, both capacitors are self-balanced and have minimal voltage fluctuations. The voltage between capacitors C_1 and C_2 is equilibrated at 50 V and 100 V, respectively, without needing sensors or further methods.

Fig. 5 (b) displays the experimental outcome of the sudden change in load condition. The voltage level has been verified to remain consistent at its peak value of 150 V. The fluctuation in load impacts the discharging current of the capacitors, leading to a reduction in the value of the capacitors voltage ripples.

Fig. 5 (c) illustrates a corresponding shift in the modulation index. It has been noted that it produces modulation levels of 7, 5, and 3 for modulation indices of 0.95, 0.5, and 0.2, respectively.

The adjustment of the switching frequency (200 Hz to 5 kHz) is effectively managed by the PD, as illustrated in Fig. 5 (d). The waveform also shows that the PD swiftly adapts its transient response at both switching frequencies. As a result, the PD can leverage the inherent balance across different output values. The quick convergence during tran-

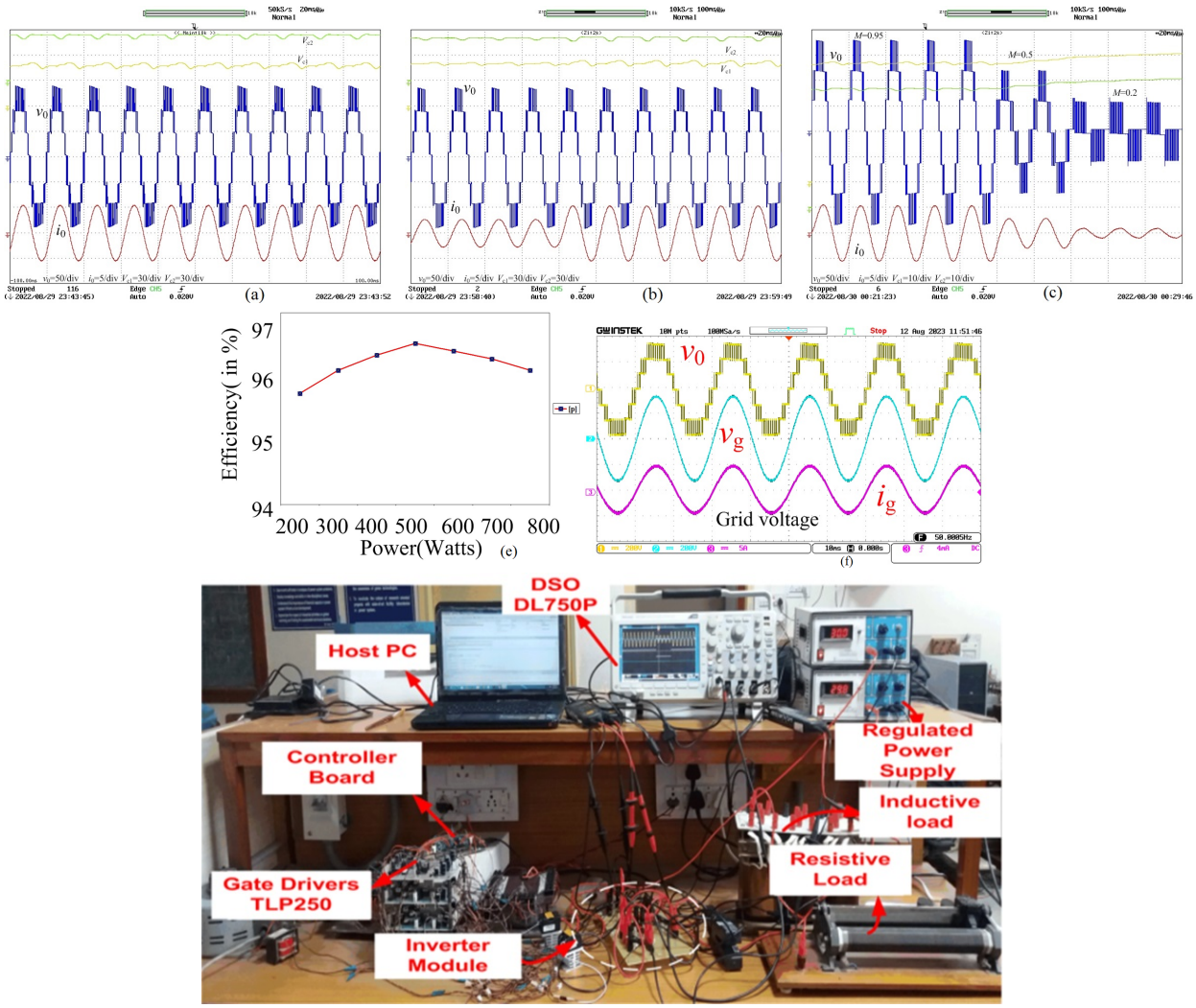

Figure 5. Displays the experimental results, including (a) constant load, (b) load variation, (c) switching frequency variation, (d) modulation index variation, (e) efficiency curve, (f) grid-connected results, and (g) the prototype module.

sient phases demonstrates the high dynamic performance of the PD.
In addition, an analysis of the proposed topology efficiency has also been incorporated, i.e., maximum measured efficiency reaching 96.95%.
Fig. 5 (e) illustrates the relationship between efficiency and output power. The topology that has been proposed offers the highest efficiency, which can reach 500 W, as shown in Fig. 5 (f). Fig. 5 (g) is a model of the prototype modules that would constitute the PD. The PD has demonstrated efficacy in several experimental situations.

Grid-connected mode

When the system is connected to the grid, the control strategy's main objective is to generate a sinusoidal current with minimal deviations to minimize harmonic distortion in the grid voltage.

Control technique

Consequently, the PD employs a Proportional-Resonant (*PR*) controller, which offers significant amplification at a specific frequency to accurately follow the reference sinusoidal current with no deviation, as mentioned in reference [26].
Here is a rephrased version of the transfer function description for the *PR* controller:

$$G_{PR}(s) = K_P + \frac{2K_r\omega_c s}{S^2 + 2\omega_c s + \omega_0^2} \tag{15}$$

where k_P, $k_r\omega_c$: denote the proportional gain, the infinite gain, and the resonant frequency, respectively. k_P: governs the controller responsiveness, k_r: determines the level of signal amplification at the resonant frequency and ω_c: sets the controller operational bandwidth around that frequency. These parameters shape the controller's behavior and performance within the control system.
The recommended configuration was tested in the prototype model to confirm the suitability of employing the *PR* controller in grid-connected mode. Table 5 provides a list of the parameters utilized during the experimentation. Fig. 6 shows the results of the grid-tied model experiment. The inverter output voltage exhibits a 7-level waveform, peaking at 400 V. The experimental findings verify the unity power factor operation of the recommended SC inverter by showing that the grid voltage (v_g) and current (i_g) are in phase when the inverter injects 1.5 kW of real power. This study proves that the PD functions normally when linked to the grid.
Filter Design

Table 5. Grid-connected mode simulation parameters.

Parameters	Value
Specified power	1.5 kW
Inductance parameter	3 mH
RMS voltage of the grid	250 V
Grid frequency	50 Hz
Switching frequency	2 kHz
Resistance of the winding in a filter inductance	0.1 Ω

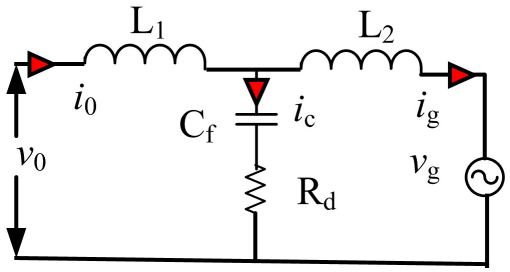

Figure 6. LCL filter with damping resistor for grid interfacing.

Compared to L or LC filters, an LCL filter is better at reducing harmonics at high frequencies, making it ideal for meeting the power quality standards of IEEE Std 1547-2018 (Fig. 6). Each LCL filter has four parts: an inductor on the inverter side (L_1), an inductor on the grid side L_2, a capacitor (C_f), and a damping resistor (R_D) [**?**]. The following formula can be used to get the filter resonant frequency (ω_r).

$$\omega_r = \frac{1}{\sqrt{C_f L_p}} \tag{16}$$

$$L_P = \frac{L_1 L_2}{L_1 + L_2} \tag{17}$$

The equation below defines the minimum required inductance for the filter.

$$L_{min} = \frac{v_{fs}}{i_{gf} \times \omega_s \times [1 - (\omega_s/\omega_r)^2]} \tag{18}$$

To restrict the maximum harmonic current distortion (i_{gf}) to 0.3% of the rated RMS output current (i_g)at the switching frequency (f_{sw}), the harmonics at the switching frequency per unit of the fundamental RMS inverter output voltage before the filter (V_1) should be maintained at 21.7% of v_0. If the peak voltage drops per unit of the rated RMS grid voltage (v_g) is Δv_L, then the maximum allowable filter inductance ($L_{\max}$) can be determined as follows:

$$L_{\max} = \frac{\Delta v_L \times v_g}{2 \times \pi \times f \times i_g} \tag{19}$$

The range from $L_{\min}$ to $L_{\max}$ should be used to pick the inductance L_P. For each side of the filter, the inductances are represented as $L_P/2$. For a maximum reactive power Q per unit of the rated power S, the minimum $C_{\min}$ and maximum $C_{\max}$ values of the filter capacitance can be calculated using the following expressions.

$$C_{\min} = \frac{4}{\omega_r \times f_r} \tag{20}$$

$$C_{\max} = \frac{\Delta Q_{Cf} \times S}{\omega \times v_g^2} \tag{21}$$

The filter capacitance C_f is selected within a specified range from $C_{\min}$ to $C_{\max}$. The damping resistance R_D , calculated based on a target quality factor Q_f is determined as follows:

$$R_d = \sqrt{\frac{L_P/(4 \times C_f)}{Q_f^2 - 1}} \tag{22}$$

Table 6. Comparative analysis of switched capacitor-based 7-level MLI topologies.

Ref.	N_l	N_{sw}	N_c	N_{dri}	N_{ad}	A	B	C	CF	
									$\alpha = 0.5$	$\alpha = 1.5$
[8]	**7**	14	2	14	2	3	4.57	4.5	4.89	5.53
[9]	**7**	16	2	14	-	3	4.57	5.3	4.57	5.7
[10]	**7**	10	4	8	-	1.5	3.14	5	3.5	4.21
[11]	**7**	10	4	10	-	1.5	3.14	6.3	3.59	4.49
[12]	**7**	8	2	8	2	3	2.85	6.3	3.3	4.2
[14]	**7**	12	3	12	-	3	3.85	5.3	4.23	5
[15]	**7**	10	3	10	-	3	3.28	6.6	3.75	4.7
[17]	**7**	10	2	10	-	3	3.14	6	3.57	4.42
[19]	**7**	10	3	10	-	1.5	3.28	5.3	3.66	4.46
[18]	**7**	9	3	9	2	3	3.28	5.6	3.64	4.36
[20]	**7**	9	2	9	-	1.5	2.85	6	3.3	4.14
[26]	**9**	10	4	10	4	1	3.11	8.5	3.58	4.52
[27]	**5**	7	3	7	-	1	3.4	6.5	4.05	5.35
[28]	**6**	7	5	7	2	2.5	3.5	6	4	5
[29]	**6**	6	4	5	2	1.5	2.83	4.6	3.21	4
[31]	**7**	10	3	10	2	1.5	3.57	7.56	4.11	5.19
[33]	**5**	8	2	8	0	2	9	6	4.2	5.4
[32]	**7**	10	3	10	2	1.5	3.57	9.33	4.2	5.57
[34]	**5**	7	2	7	0	1	3.2	6	3.8	5
[PD]	**7**	9	2	9	-	3	2.85	6	3.28	4.14

N_{sw}: No. of switches, N_c: No. of capacitors, N_{dri}: No of the driver, N_{ad}: No. of an auxiliary diode, A: gain, B: component count per level, C: per unit total standing voltage.

6. Comparative analysis

The most cutting-edge 7-level topologies that use switched capacitors are compared in this section. All topologies' performance is displayed in Table 6, which provides a fair comparison. The 7-level selected topologies share standard features such as unity input DC source and the ability to raise voltage. The comparison has been conducted using the primary indicators, including the number of switching components, TSV, gain, and cost function (CF). The number of components per level ($F_{c/l}$), and CF can be expressed as stated in reference [19].

$$F_{C/L} = \frac{N_{sw} + N_{dri} + N_c + N_{ad}}{N_l} \tag{23}$$

$$\mathrm{CF} = \frac{N_{sw} + N_{dri} + N_c + N_{ad} + \alpha TSV_{pu}}{N_l} \tag{24}$$

The weight factor α can take on one of three possible values ($\alpha < 1$, $\alpha > 1$, $\alpha = 1$) based on the value of the device count or TSV. $\alpha < 1$ indicates that the switching components are prioritized above TSV.
When $\alpha > 1$, it indicates that the TSV is prioritized above the switching components. TSV_{pu} defined as:

$$TSV_{pu} = \frac{[\mathrm{TSV} + \mathrm{PIV}]}{V_{\max}} \tag{25}$$

Table 6 shows that the topology [12] necessitates a backend H-bridge; however, one with fewer parts than is specified. Four higher-voltage switches are necessary for the H-back bridge end. More switches are needed for the other studied topologies than for the PD. In addition, the proposed topology does not necessitate the utilization of any power diodes; in contrast, the topologies presented in [8–10, 14]and [18]

Table 7. Cost analysis of the PD vs other topologies.

Component	Part number	Rating	Unit price ($)	[18]	[17]	[16]	[14]	[12]	[PD]
IGBT*	IRGP4086PBF	300 V, 70 A	1.87	-	-		-	-	5
	FGPF30N30D	300 V, 30 A	4.68	5	4	8	8	-	2
	IKW30N60T	600 V, 60A	5.65	2	4	2	4	4	-
	STGWA15H129DF2	1200 V, 30 A	8.67	2	2		-	4	-
Diode*	VS-20ETF06SLHM3	600 V, 20 A	3.1	2	4	4	-	2	2
Capacitor*	ALF20G102KL600	600 V, 1000 μF	48.62	-	-	-		-	
	ALS81H102DE350	300 V, 1000 μF	10.55	-	-	-		-	2
	ALF20G102EC200	200 V, 1000 μF	7.31	2	2	2	2	2	2
	ELG108M100AR2AA	100 V, 1000 μF	3.18	-	-	-			
Gate driver	IR2110		1.8	9	10	10	11	8	9
		Total cost($)		168.2	103.7	93.76	94.46	92.5	76.83

*www.digikey.com

each need the utilization of two diodes.
As per Table 6, the PD has the least $F_{C/L)}$ among [8–20]. The PD has a more significant boosting factor compared to [10, 11], [18], and [20]. In contrast to the PD, the topologies [10, 11], [12–17], and [19] all share the same boosting factor. Moreover, except for the topologies described in [8–10] and [14, 18], the TSV_{pu} of PD is lower. However, the PD only requires nine switches, while other topologies require many more.
After considering these aspects, it is clear that the PD is the most cost-effective among the present topologies. Table 7 presents the cost analysis results that further emphasize PD many benefits. All topologies have been configured with the same voltage parameters for this cost analysis. Furthermore, in the cost analysis, all factors have been considered equally. Compared with the PD except [29], the topologies [26–34] have a higher cost function, more switching components, and reduced gain. However, the topology has less voltage gain and lower levels [29]. As depicted in Table 7, it is evident that the component cost of the PD is the most economical compared to alternative topologies.

7. Conclusion

This paper introduces a new SCMLI topology characterized by minimal part count, self-balancing properties of capacitors, voltage-boosting capability, and the capacity to provide power to inductive loads. Furthermore, the PD possesses a cost-effective capability and exceptional characteristics, enhancing its appeal and affordability for low-voltage applications. Experimental and modeling data support the claims made above about the benefits of PD. Both the results of the PD show excellent stability under different conditions.

Authors contributions
All authors have contributed equally to prepare the paper.

Availability of data and materials
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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