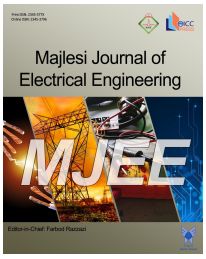

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A zero voltage transition interleaved DC-DC converter with reduced voltage stress

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Original Research

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Abstract:

This paper presents an interleaved converter designed to achieve a high voltage gain using a combination of coupled inductors and switched capacitors. Additionally, the converter incorporates winding-cross-coupled inductors to reduce input current ripple and enhance voltage gain. The use of switches with smaller RDS(on) can be achieved by reducing the switch voltage stress through the high voltage gain. Additionally, the switches operate under zero-voltage (ZV) conditions and do not have capacitive turn-on losses, resulting in reduced conductive losses. The proposed auxiliary circuit has a small number of elements and can be expanded to include more parallel branches. The converter's theoretical analysis was thoroughly examined and confirmed through the development of a prototype. Experimental results demonstrate a 6% improvement in efficiency and a 14 dBμV reduction in EMI in comparison to the conventional hard-switching design without auxiliary circuit.

Keywords: Interleaved converter; High step-up; Zero voltage transition; Winding-cross-coupled-inductor

1. Introduction

Nowadays, there has been an increase in the use of converters with high gain as a solution to the problems faced by boost converters. These problems include diode reverse recovery problem, switch elevated stress, switching losses, and diode elevated current. High gain converters are commonly applied in green energy systems like photovoltaic systems and fuel cells [2, 3]. One effective approach to boost the gain involves using coupled inductors. Increasing the turn ratio of these inductors enhances the gain while also lowering the stress on the switch [4, 5]. However, it is necessary to incorporate passive or active clamp circuits to absorb the leakage inductance energy in these circuits. Passive clamp circuits tend to have higher losses due to resistance present in their structure [6].

Additionally, while active clamp circuits effectively absorb leakage inductance energy and ensure zero voltage switching, they encounter issues such as duty cycle losses, a high number of auxiliary switches, and increased circulating current in the added circuit. Another challenge with other coupled inductors is the fluctuation of the input current. To reduce input current ripple and enhance power output in high step-up converters, utilizing an interleaved structure is recommended [7, 8].

However, this current ripple is still inappropriate for solar cell and fuel cell applications. Hence, winding-cross-coupled-inductors (WCCI) were proposed. In this structure, three windings are implemented, with the third winding not only contributing to gain enhancement but also helping to decrease input current ripple [1, 7, 8].

In [8], a cross-winding interleaved converter with an active clamp is presented, yet despite enjoying high gain and small input current ripple, a large number of power switches and duty cycle losses are present in this converter. In [9], a converter with interleaving with a ZVT supplementary circuit is offered. In this converter, the third winding is employed in the auxiliary circuit to release the snubber capacitors, yet the extra switch in this structure operates ZC, and it suffers capacitor turn-on losses. In [10], a design features a multi-phase boost is proposed, incorporating both coupled-inductors and a voltage doubler circuit. Notably, the input and output are electrically isolated, and the converter functions under hard switching conditions. The converter described in [11] incorporates soft switching con-

ditions without the need for extra switches. However, its main drawback is the uncommon ground input and output, which severely limits its practical application. However, the major problem of such a converter is that the capacitive switching loss in the main semiconductor. Otherwise, the soft-switching operation of switches depends on the load. References [12–18] introduce highly efficient interleaved high-step-up converters featuring soft switching. These designs utilize auxiliary circuits to facilitate soft switching and recover energy from leakage inductances. The high voltage gain is achieved through the combination of coupled-inductor and switched capacitor techniques. In [17] a novel interleaved converter featuring a symmetrical structure and exceptionally high voltage gain is presented. The converter utilizes active clamp circuits for both phases, resulting in an increased switch count of four. However, the high input current ripple makes this design less suitable for photovoltaic applications, in addition to the loss of soft-switching capability under light load conditions. [18] introduces a converter with a symmetrical structure that effectively minimizes input current ripple. Zero-current switching (ZCS) for the switches is accomplished using leakage inductance, which helps reduce the overall component count. However, the converter experiences hard switching turn-off for the switches, and the capacitive turn-on loss adversely affect its efficiency.

This paper proposes a converter with a high voltage gain engineered using an interleaved structure to decrease current stress and a modular supplementary circuit to provide zero-voltage (ZV) conditions for turning on and off the fundamental switches and ZVZC conditions for turning on the assisting switch. This structure removes capacitive switching losses in all semiconductor elements. and eliminates the reverse recovery problem by turning off circuit diodes under ZC. The voltage burden on the fundamental switches is also greatly shortened, allowing for the use of switches with low RDS(on) and further reducing conduction losses. Lastly, another characteristic of this converter is that the power MOSFETs have grounded sources, which streamlines the drive circuit architecture. The converter introduces several key innovations, such as utilizing a cross-coupled inductor to boost voltage gain while reducing input current ripple. It also incorporates a modular auxiliary circuit that facilitates soft switching of all semiconductor elements, minimizing losses in the main converter. Additionally, the converter design allows for increasing the number of parallel branches and overall power capacity without necessitating significant changes to the auxiliary circuit.

In this paper, the suggested converter is first illustrated in section 2 and its functionality is thoroughly explained. Then, the designing process of passive elements in addition to voltage stress of converter elements are explained in section 3. Afterwards, the practical results to prove the accuracy of the analysis are mentioned in section 4. Finally, section 5 discusses the transient response of the converter, while section 6 provides an evaluation of the converter with other similar ones.

2. The proposed interleaved WCCI converter

One approach to reducing input current ripple and enhancing voltage gain is the utilization of the WCCI technique, as demonstrated in [1] (Fig. 1a). The primary drawback of this converter is the high number of switches and the continuous operation of auxiliary switches during the entire off-time of the corresponding main switch, which increases circulating current in the auxiliary circuit. In the proposed converter, shown in Fig. 1(b), the number of auxiliary switches is reduced by one, and the operating duration of the auxiliary switch is significantly shortened. Additionally, by integrating the WCCI technique with switched capacitors, the voltage gain is further improved. The converter is made up of two parts. The first part is the voltage multiplier circuit, which consists of the coupled inductors L_{11}-L_{12}-L_{13} and L_{21}-L_{22}-L_{23}, capacitors C_1-C_4, and diodes D_1-D_4. As can be witnessed, the coupling inductors have three windings and one core and are arranged in a crossed manner so as to reduce the input current ripple in addition to increasing the voltage gain. The second part is the ZVT auxiliary circuit. Auxiliary switch S_a includes capacitors C_{a1} and C_{a2}, snubber capacitors C_{S1} and C_{S2}, and auxiliary inductor L_a. The converter also has two main switches S_1 and S_2, output diodes D_{O1} and D_{O2}, and output capacitor C_O. The main switches in this converter are turned on with 180 degrees of phase difference, and the frequency of the auxiliary switch is twice that of the main switches and it is turned on prior to the main switches being turned on. Fig. 2 demonstrates the main operating waveforms of the converter.

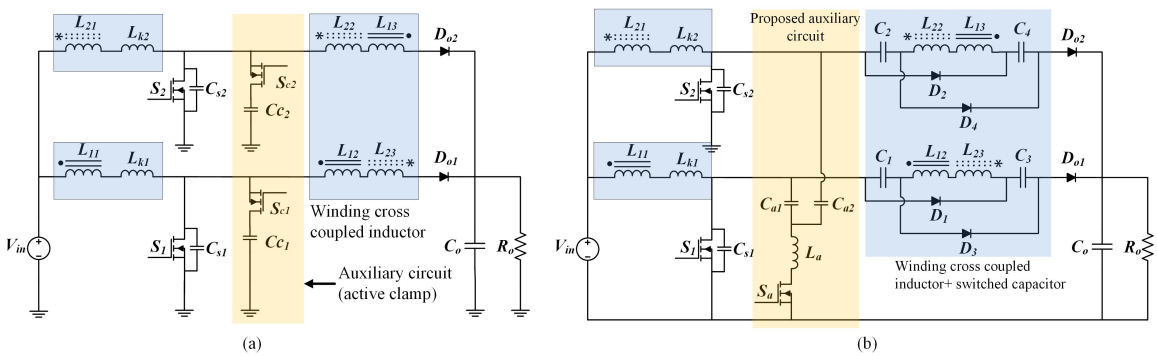

Figure 1. (a) The interleaved WCCI converter in [1] (b) The suggested WCCI converter.

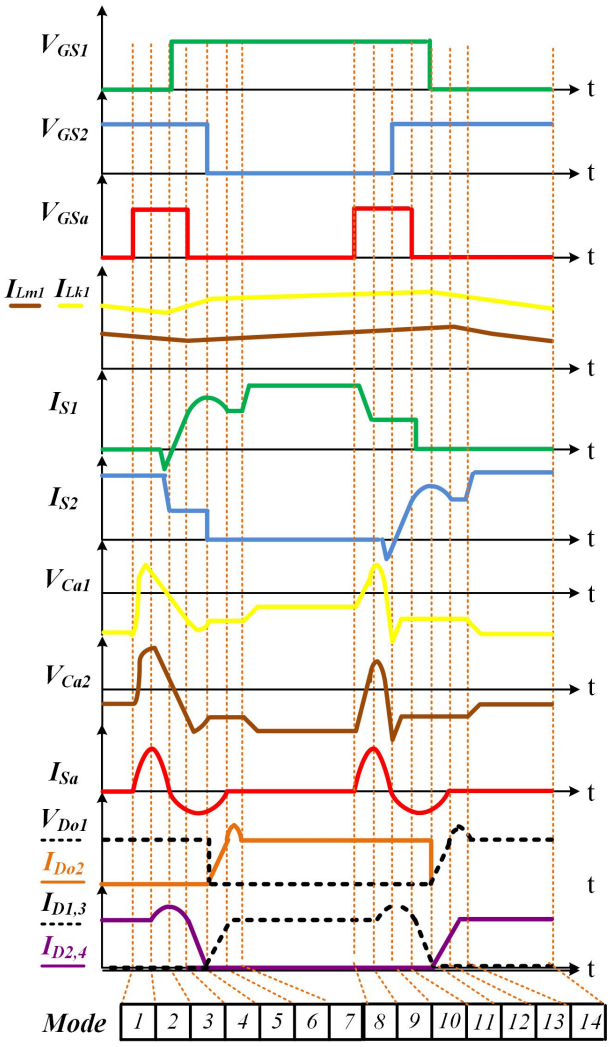

Figure 2. The theoretical operating curves.

2.1 The proposed converter operation

The proposed converter consists of 14 operating states in a cycle, whose 7 modes are explained due to symmetrical structure. Coupling inductors are modeled as a magnetizing inductor parallel to an ideal transformer (L_{m1}, L_{m2}) and leakage inductance is modeled by an inductor in series with an ideal transformer. Moreover, in order to eliminate input current ripple, N_{11}/N_{12} and N_{11}/N_{13} are equal to N_{12}/N_{22} and N_{21}/N_{23}, respectively. Hence, in this analysis, it is considered that $N_{11} = N_{21}$, $N_{22} = N_{12}$, and $N_{23} = N_{13}$. Furthermore, in a switching cycle the capacitors C_1 to C_4 and the output capacitor C_O are of sufficient value and their voltage remain constant, and the magnetizing currents I_{Lm1} and I_{Lm2} are also due to the large size of the magnetizing inductance during a cycle are considered as constant.

The 1st Mode: Resonance is stablished between the inductor L_a and capacitors C_{a1} and C_{a2}, respectively when the auxiliary switch S_a is activated. This resonance causes the current of L_a to increase resonantly from zero, and The auxiliary switch is triggered when the current is zero (ZC). This mode continues until the current through L_a reaches twice the value of I_{Lm}.

$$I_{La}(t) = I_{Sa}(t) = \frac{V_0}{Z_1(3n+1)}\sin(\omega_1(t-t_0)) \tag{1}$$

$$V_{Ca}(t) = \frac{V_0}{3n+1} - \frac{V_0}{3n+1}\cos(\omega_1(t-t_0)) \tag{2}$$

$$Z_1 = \sqrt{\frac{L_a}{C_a}} \tag{3}$$

$$C_{a1} = C_{a2} = C_a \tag{4}$$

$$\omega_1 = \frac{1}{\sqrt{L_a C_a}} \tag{5}$$

$$\Delta t_1 = \frac{1}{\omega_1}\sin^{-1}\frac{2I_{in}Z_1(3n+1)}{V_0} \tag{6}$$

The 2nd Mode: When the current of switch S_a reaches $2I_{Lm}$, diode D_{o2} is off and D_2 and D_4 are conducting. In this state, a new resonance between L_a and C_{a1}, C_{a2}, and C_{S1}, respectively, starts and continues until capacitor C_{S1} is completely discharged.

$$\begin{aligned} I_{La}(t) = {} & \frac{\frac{V_0}{1+3n} - V_{Cr}(t_1)}{Z_2}\sin(\omega_2(t-t_1)) \\ & + \frac{C_{eq}}{C_a}2I_{in}\cos(\omega_2(t-t_1)) + \frac{C_{eq}}{C_{S1}}2I_{in} \end{aligned} \tag{7}$$

$$\begin{aligned} V_{CS} = {} & \frac{C_{eq}}{C_{S1}}\left(\frac{V_0}{1+3n} - V_{Cr}(t_1)\right)\cos(\omega_2(t-t_1)) \\ & - \frac{C_{eq}}{C_a}I_{in}Z_2\sin\left(\omega_2(t-t_1) - \frac{V_0}{1+3n} + V_{Cr}(t_1)\right) \\ & + \frac{2I_{in}C_{eq}}{C_{S1}^2}(t-t_1) + \frac{V_0}{1+3n} \end{aligned} \tag{8}$$

$$C_{eq} = \frac{C_a C_{S1}}{C_a + C_{S1}} \tag{9}$$

$$Z_2 = \sqrt{\frac{L_a}{C_{eq}}} \tag{10}$$

$$\omega_2 = \frac{1}{\sqrt{L_a C_{eq}}} \tag{11}$$

The 3rd Mode: When C_{S1} is fully discharged, as the internal diode of S_1 starts conducting, it allows the switch to be turned on even under zero-voltage (ZV) conditions. In this mode, due to the short circuit of capacitor C_{S1}, a new resonance occurs and the current L_a and voltage C_a vary as follows:

$$I_2 = I_{La}[t_2]\ ,\ V_2 = V_{Cr}(t_2) \tag{12}$$

$$I_{La}(t) = I_2\cos(\omega_1(t-t_Z)) - \frac{V_2}{Z_1}\sin(\omega_1(t-t_Z)) \tag{13}$$

$$V_{Ca}(t) = V_2\cos(\omega_1(t-t_Z)) + I_2 Z_1\sin(\omega_1(t-t_Z)) \tag{14}$$

The 4th Mode: In this state, the current through S_2 becomes constant and equals the magnetizing current, while the currents through diodes D_2 and D_4 gradually decrease until they turn off under Zero Current (ZC) conditions at the conclusion of this state.

The 5th Mode: The mode is initiated when S_2 is turned off and snubber capacitor C_{s2} is charged. Thus, the auxiliary

switch shutdown occurs under ZVZC conditions. In this state, the current in inductor La becomes zero and the resonance between L_a and C_a continues via switches S_1, S_2, and D_{Sa}.

The 6th Mode: This mode starts after the L_a current reaches zero and the D_{Sa} turns off during zero-current (ZC) conditions. In this state, there is a resonant increase in D_{O2} current and diodes D_1 and D_3 are activated, resulting in the charging of capacitors C_1 and C_3. Switch S_1 is on, and leading to a linear charging of inductor L_{m1}.

The 7th Mode: Upon turning off the switch S_2, the output diode D_{o1} current remains fixed at the output current level. Consequently, the current through S_1 rises to match the input current value, and L_{m1} is still charged while inductor L_{m2} is discharged to the output. This interval persists until S_a is activated once more.

3. Examination of the proposed converter's performance

This section outlines the design process of the suggested interleaved converter.

3.1 Auxiliary circuit elements

According to the formula presented in reference [5], the snubber capacitors, C_{S1} and C_{S2}, are dimensioned as follows:

$$C_{S1}\ ,\ C_{S2} = \frac{I_{in} t_f}{4V_0} \tag{15}$$

C_{a1} and C_{a2} capacitors should be chosen much larger than the snubber capacitors so that the snubber capacitors can be thoroughly discharged. Hence, auxiliary capacitors C_{a1} and C_{a2}, when being designed, are considered 15 times bigger than snubber capacitors.

$$C_{a1} = C_{a2} = 15C_S \tag{16}$$

According to the performance of the converter in the first mode, to ensure zero-voltage conditions, the current of the L_a must reach I_{in} (Fig 3). Thus, the inductor L_a is achieved via the following equation:

$$I_{La} > I_{in} \rightarrow \frac{V_0}{Z_1(1+3n)} > I_{in} \tag{17}$$

$$Z_1 < \frac{V_0}{(1+3n)I_{in}} \tag{18}$$

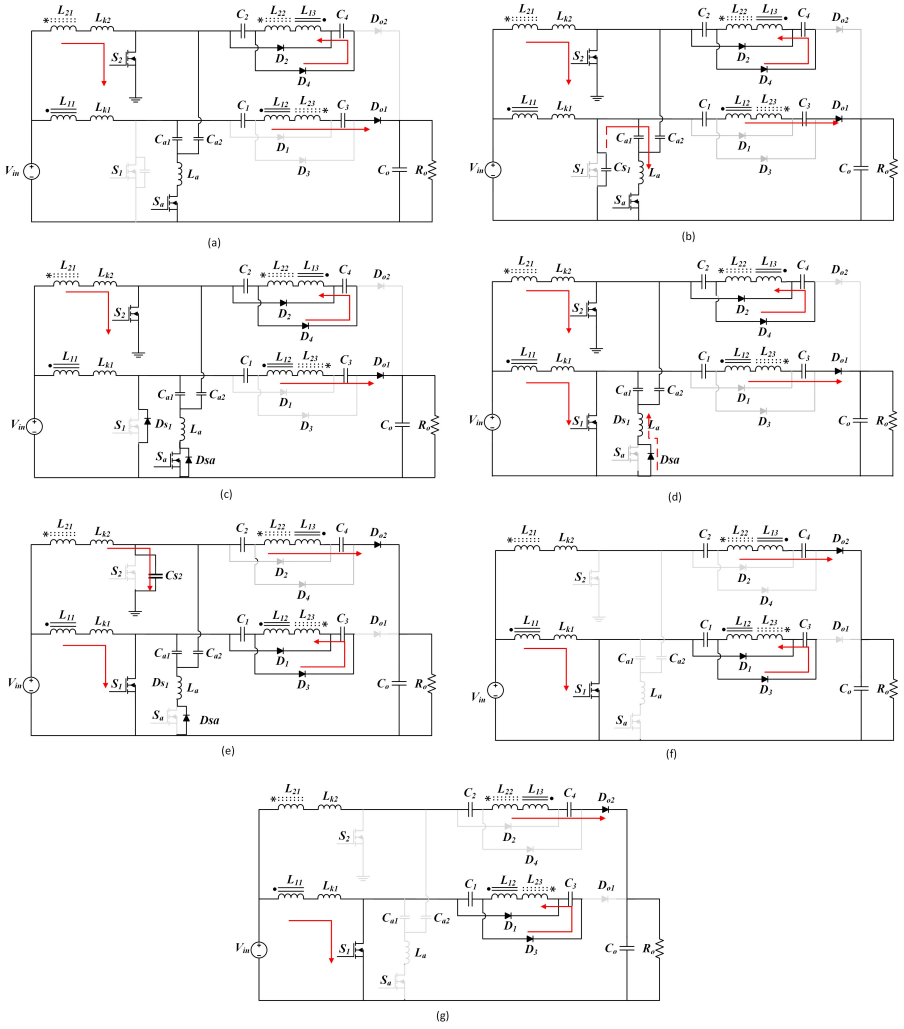

Figure 3. The corresponding circuit configurations for each operational stage are: (a) Stage 1, (b) Stage 2, (c) Stage 3, (d) Stage 4, (e) Stage 5, (f) Stage 6, (g) Stage 7.

Moreover, in the second and third modes, the snubber capacitor should be entirely discharged.
By choosing the right value for Z_1, inductor L_a is simply calculated as follows:

$$L_a = Z_1^2 C_a \tag{19}$$

3.2 Voltage gain of the proposed converter

The gain of the converter is derived by analyzing the volt-second equivalence across the input magnetizing inductor. This involves setting the product of the input voltage and its duty ratio equal to the product of the output voltage and its corresponding duty ratio.
The analysis assumes a turns ratio of n between the secondary and primary, as well as between the tertiary and primary windings of both inductors. This assumption simplifies the calculations and enables a more straightforward gain analysis.

$$\frac{nL_{22}}{nL_{21}} = \frac{nL_{23}}{nL_{21}} = n \tag{20}$$

$$\frac{nL_{12}}{nL_{11}} = \frac{nL_{13}}{nL_{11}} = n \tag{21}$$

$$V_{in}DT + V_{cc}(1-D)T = 0 \tag{22}$$

$$V_{CC} = V_{CS} = \frac{V_{in}}{1-D} \tag{23}$$

By writing a KVL when switch S_1 is off and diode D_{O1} is on.

$$\frac{V_{in}}{1-D} + 2V_C + V_{L12} + V_{L23} - V_0 = 0 \tag{24}$$

$$V_{L12} = \frac{nDV_{in}}{1-D} \tag{25}$$

$$V_{L23} = nV_{in} \tag{26}$$

Also, when diodes D_4 and D_2 are on, the voltages of C_2 and C_4 are equal. With the voltage transferred from the pair of inductors, therefore:

$$V_C = nV_{in} + \frac{nDV_{in}}{1-D} = \frac{nV_{in}}{1-D} \tag{27}$$

$$V_0 = \frac{V_{in}}{1-D} + 2V_C + nV_{Lm} + nV_{in} = \frac{(1+3n)V_{in}}{1-D} \tag{28}$$

$$\frac{V_0}{V_{in}} = \frac{1+3n}{1-D} \tag{29}$$

Figure 4 demonstrates how the gain of the introduced converter changes with variations in the duty ratio. It highlights a significant enhancement in voltage gain relative to a simple boost converter, which can enhance performance and increase efficiency in power conversion applications. When accounting for the effect of the leakage inductance, the coupling coefficient must be incorporated into the gain calculation, as shown in the following equations.

$$\frac{V_0}{V_{in}} = \frac{1+3nK}{1-D} \tag{30}$$

$$K = \frac{L_m}{L_m + L_k} \tag{31}$$

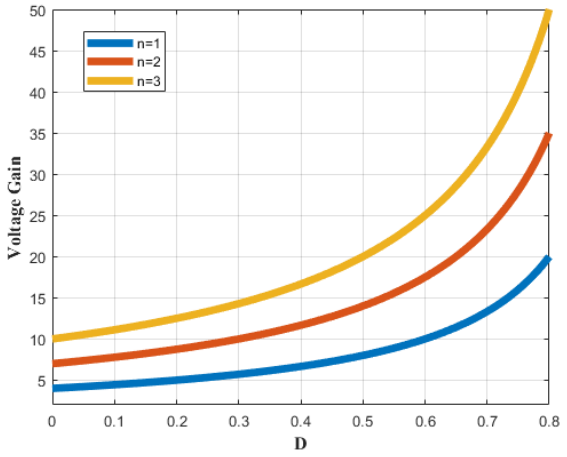

Figure 4. The converter voltage gain as a function of duty ratio variations.

3.3 The voltage stress experienced by the semiconductor devices in the converter

To obtain the voltage stress of the switches, a KVL should be written in the input loop when the switch is off.

$$V_{S1} = V_{S2} = \frac{V_0}{1+3n} \tag{32}$$

$$V_{Sa} = \frac{V_0}{1+3n} + V_C r(\max) \tag{33}$$

$$V_{Cr\,\max} = \sqrt{\frac{L_a}{C_a} I_{in}^2 + \left(\frac{C_S}{C_a}\right)^2 \frac{V_0^2}{(1+3n)^2}} \tag{34}$$

Additionally, by using KVL to the loop when the output diode is off and other diodes conducting, the voltage across the output diode can be easily determined.

$$V_{D_O} = V_C - V_0 = \frac{V_{in}}{1-D} + \frac{nV_{in}}{1-D} - \frac{V_{in}(1+3n)}{1-D} \tag{35}$$

$$V_{D_O} = \frac{2nV_{in}}{1-D} = \frac{2nV_0}{1+3n} \tag{36}$$

To calculate the voltage of diodes D_1 to D_4, It is sufficient to write the KVL for the current path through these diodes, Which has a value corresponding to the output diodes voltage.

$$V_{D_{1-4}} = V_{D_{O1-2}} = \frac{2nV_0}{1+3n} \tag{37}$$

Figure 5 illustrates the normalized voltage stress on the main switches and circuit diodes as a function of the inductors' turns ratio. As shown, growing the turns ratio n reduces the switches voltage stress, while simultaneously increasing the stress on the diodes. This introduces a design trade-off, making it crucial to select an optimal value for n that minimizes excessive the diodes voltage, enabling the application of diodes with a low forward voltage.

4. The simulation and experimental results

This section details the implementation and evaluation of the converter's performance. The proposed converter was initially simulated in the PSPICE software based on the specifications outlined in Table 1. Figure 6(a) presents the

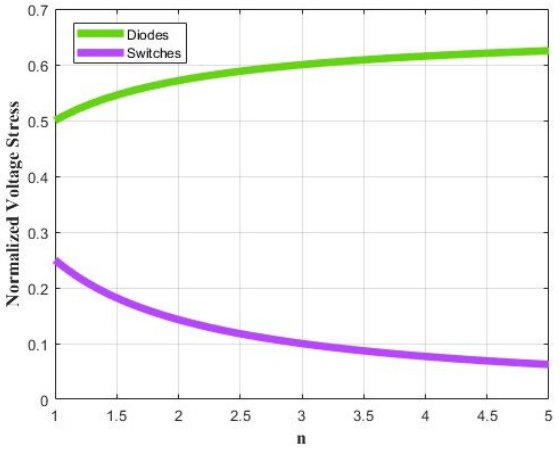

Figure 5. The normalized voltage stress of the main switches and diodes versus turn ratio.

simulation results for the voltage and current of switch S_1, demonstrating the achievement of soft-switching conditions. Figure 6(b) illustrates the simulated current of the auxiliary switch, where ZCS conditions for both turn-on and turn-off transitions are confirmed. Figures 6(c) and 6(d) display the current waveforms of diodes D_o and D_1, respectively. As evident from these figures, ZCS conditions are achieved for these diodes as well. Also, the suggested converter was tested under the conditions of a 400V output voltage, a 30 V input voltage, and a nominal power of 270 W. The prototype is presented in figure 7, with the specifications of the designed components recorded in Table 1. Figures 8(a) and 8(b) display the recorded current and voltage waveforms of the S_1 and S_2. These figures demonstrate that the switch current is negative when turned on, allowing for zero voltage switching conditions and minimizing capacitive turn-on losses. Additionally, the switch voltage increases gradually during turn-off as a result of the snubber capacitor's presence, indicating zero voltage conditions for turn-off instances. Figure 8(c) presents the current and voltage waveforms of S_a. As shown, the current initially increases with a positive slope and then decreases with a

Table 1. Important design specifications.

symbol	component	specification
V_{in}	input voltage	30 V
V_{out}	output voltage	400 V
P_{out}	output power	270 W
f_{sw}	switching frequency	100 kHz
C_{cp}	charge-pump capacitor	10 μF
C_a	auxiliary capacitor	22 nF
C_{out}	output capacitor	47 μF
S_m, S_a	switches	IRFP4668 pbf
D_1, D_2, D_a	diodes	MUR820
D_o	output diodes	MUR880

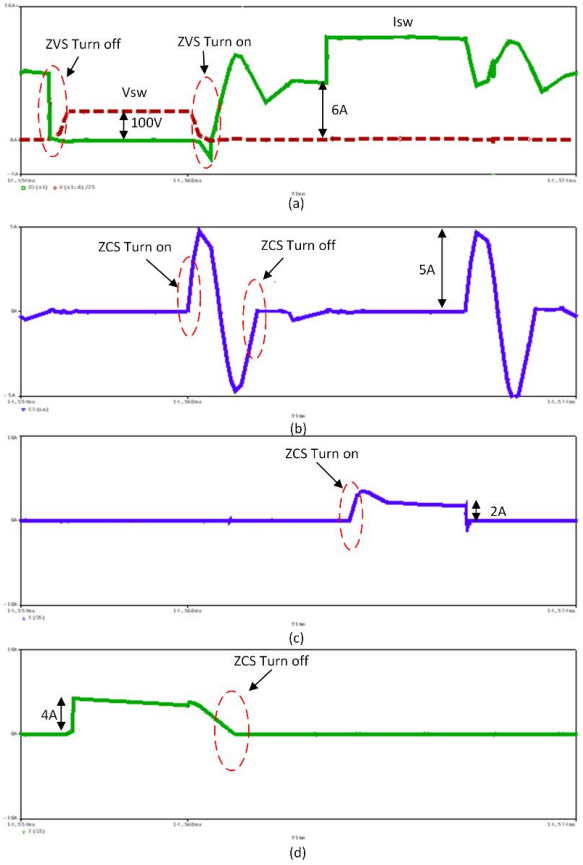

Figure 6. The simulated results (a) Voltage and current waveforms of main switch (b) Current waveform of auxiliary switch (c) Current waveform of D_{o1} (d) Current waveform of D_1.

negative slope, so the ZC conditions are available for turn on instance and ZVZC condition for turn off instance of S_a. Figure 8(d) illustrates the current waveform of the output diode D_{o1}, demonstrating the Zero Current (ZC) condition during the diode's operation. Additionally, the diode's voltage increases at turn-off instances, confirming the Zero Voltage (ZV) condition. As a result, the output diode does not experience reverse recovery issues. Therefore, the converter diodes do not impose significant conduction losses on it.

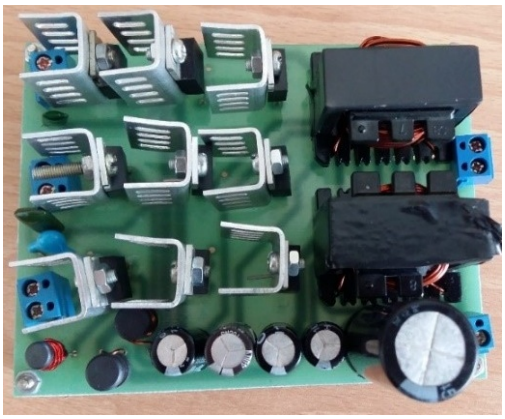

Figure 7. The implemented prototype of the proposed converter.

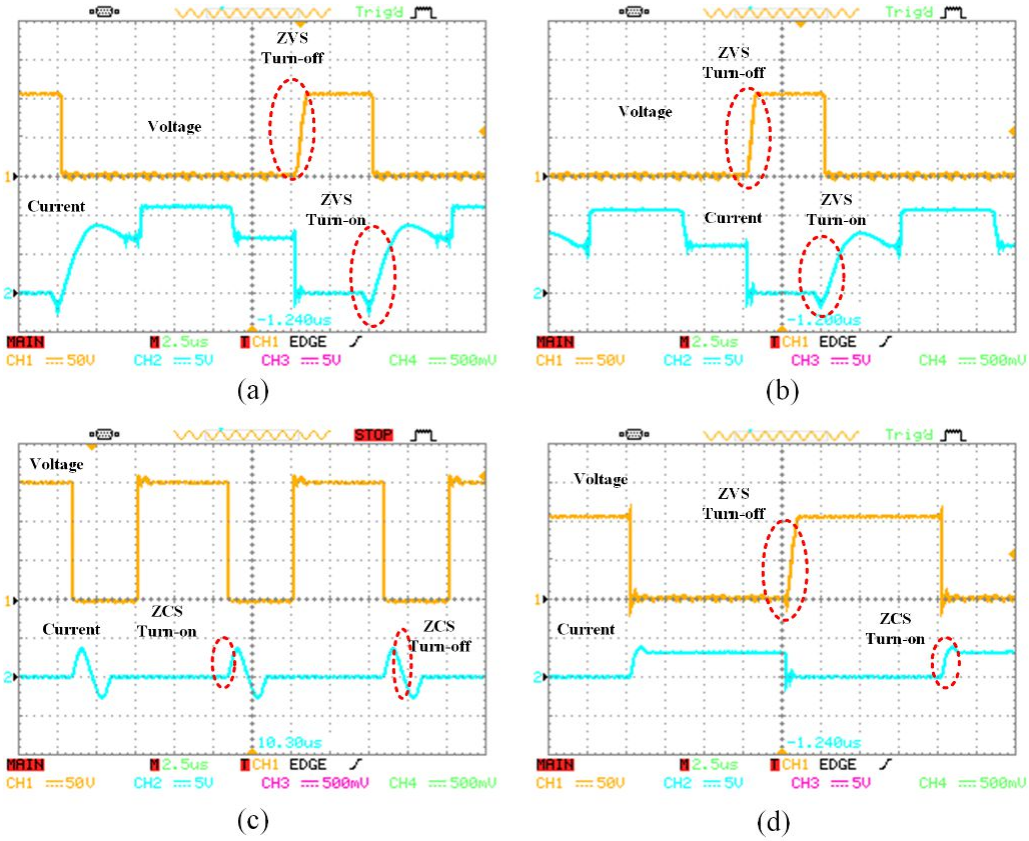

Figure 8. The measured voltage and current waveforms of semiconductor elements (a) S_1 (50 V/div, 5 A/div) (b) S_2 (50 V/div, 5 A/div) (c) S_a (50 V/div, 5 A/div) (d) D_{o1} (50 V/div, 1 A/div).

4.1 The measured conducted electromagnetic interference (EMI)

The presented converter and its hard-switched alternative with passive clamp (RCD) are measured for conducted EMI. For better comparison, the results of the spectrum analyzer (GW Instek) are shown in Fig. 9. According to these figures, based on the CISPR22 standard, the vertical axes are ranged between 20 dBμV and 100 dBμV, and the horizontal axes are ranged between 150 kHz and 30 MHz. Based on figures 9(a) and 9(b), the Electromagnetic Interference (EMI) common mode of the presented high voltage gain converter is reduced by approximately 14 dBμV compared to the conventional converter. This reduction is attributed to the soft-switching condition applied to all semiconductors, which helps minimize EMI.

4.2 Efficiency

Figure 10 compares the converter efficiency to that of a hard-switched counterpart, demonstrating a 6% improvement at full load. However, the efficiency decreases as the output power is reduced. This decline is due to nearly the auxiliary circuit current constant in during light load conditions.

4.3 Loss breakdown theoretical analysis of the proposed converter

In the evaluation of the suggested converter's loss breakdown, the switching losses and capacitive turn-on losses are

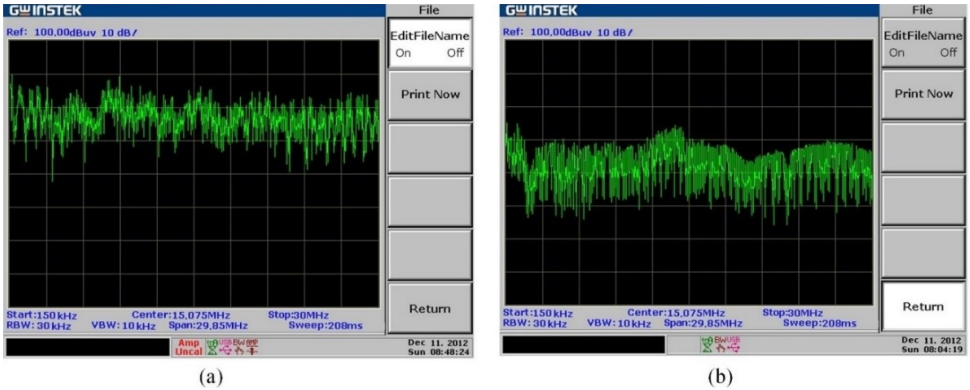

Figure 9. The measured conducted electromagnetic interference of (a) The hard-switched one (b) The proposed high step-up converter.

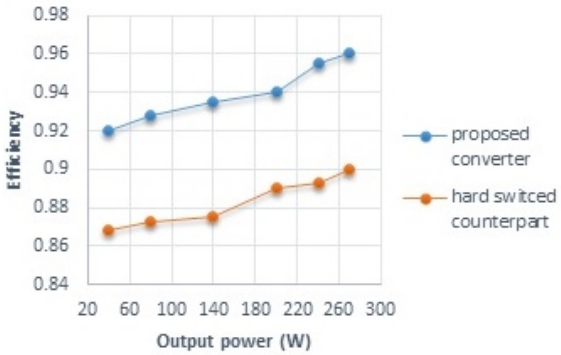

Figure 10. The recorded efficiency of the proposed converter in comparison with its hard-switched one.

considered nearly negligible thanks to the ZVS functioning of the switches. The conduction losses for switches and diodes are estimated using the formulas $R_{DS}(on)I_{S^2}$ (rms) and $V_F I_D$ (av), respectively. Here, R_{DS} (on) represents the switch resistance of the switches when they are on, IS (rms) is the current through the switches. The windings use Litz wires, and their conduction loss is calculated by the expression $R_W I_{W^2}$ (rms), where R_W stands for the winding's electrical resistance and I_W (rms) is the rms current in the windings. The ESR loss in capacitors is determined by $ESRI_{C^2}$ (rms). The distribution of power losses in the suggested converter is shown in Fig. 11.

5. Dynamic response of the proposed converter

Figure 12 illustrates the transient response of the converter to load variations. In Fig. 12(a), the load transitions from full to half, leading to a regulated output voltage overshoot of approximately 30 V and a settling time of 30 ms and additionally, in Fig. 12(b), the load changes from half load to full load change, resulting in a 30 V undershoot at a settling time of 40 ms. These observations confirm the effective functioning of the control circuit.

6. Comparison of the proposed converter with former similar converters

In Table 2, the proposed converter is compared with similar interleaved converters. Among the 10 converters examined, only the converter in [17] features automatic current balancing, making it simpler to control compared to the proposed converter and the other nine converters. In the

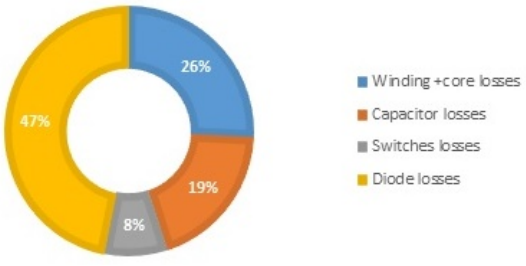

Figure 11. The converter power loss breakdown.

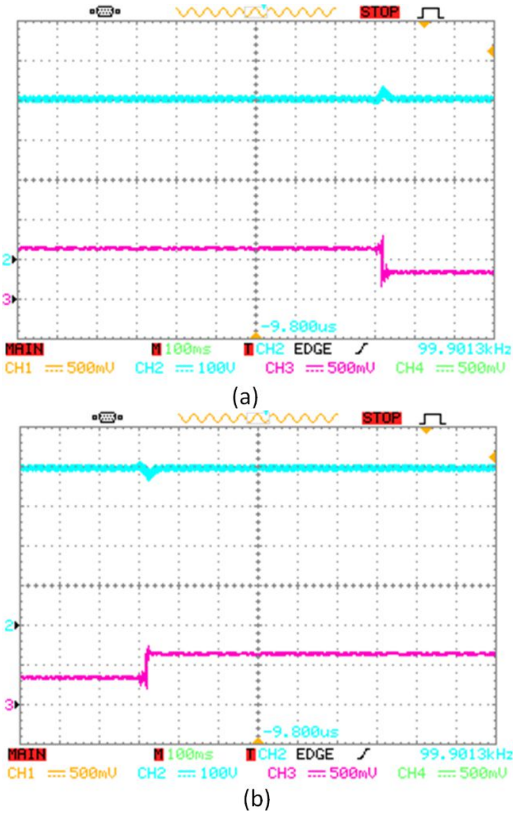

Figure 12. Dynamic response of the proposed converter under load step change (a) Full load to half load (b) Half load to full load.

proposed converter, due to the circuit's symmetry, current sharing between both phases can be achieved using a single, simple current control loop in the control circuit. Table 2 reveals that converters [11, 14] exhibit Increased voltage gain and minimized voltage stress compared to the proposed converter; however, they do not share a common ground between the input and output. Converter [15] features fewer components but requires a higher number of switches. Additionally, converters [1, 9, 13, 15] demonstrate high voltage gain and minimal input current ripple, yet they incorporate four switches in their design, which complicates the control and drive circuit implementation. Converter [10] has similar elements to the proposed converter but functions without soft switching conditions resulting in higher losses. Converter [12] exhibits a higher input current ripple than the suggested converter. In summary, although various converters present trade-offs regarding parameters like efficiency, voltage gain, switch stress, and component count, the proposed converter shows improved efficiency at full load relative to its hard-switched one, while still delivering satisfactory performance in other areas. Converter [16], on the other hand, achieves a greater voltage gain than the introduced converter.; however, it necessitates a larger number of passive components. Additionally, the output diode in [16] experiences higher voltage stress relative to the proposed converter. The switching range is limited, and switching loss occur during the turn-off instances. Furthermore, capacitive turn-on loss is present in the switches due to zero-current switching. The converter in [17] exhibits a higher voltage gain compared to the proposed converter.

Table 2. An evaluation of the performance of the proposed converter versus other similar interleaved converters.

converter	voltage gain	maximum voltage stress across switch	maximum voltage stress across diode	no. of elements M.C	S	D	C	T	switching condition	input current ripple	efficiency
[1]	$\frac{2n}{1-D}$	$\frac{V_0}{2n}$	V_0	2	4	2	5	13	ZVS	low	91% at 1kW
[10]	$\frac{2+2n}{1-D}$	$\frac{V_0}{2+2n}$	$\frac{2V_0}{2+2n}$	2	2	7	7	18	hard	low	92% at 800 W
[11]	$\frac{4+2n}{1-D}$	$\frac{V_0}{4+2n}$	$\frac{nV_0}{2+n}$	2	2	6	6	16	ZCS	high	95.7% at 500 W
[12]	$\frac{2+2n}{1-D}$	$\frac{V_0}{2+2n}$	$\frac{(1+2n)V_0}{2+2n}$	2	3	7	6	18	ZVS	low	94% at 580 W
[13]	$\frac{1+6n}{1-D}$	$\frac{V_0}{1+6n}$	$\frac{2nV_0}{1+6n}$	2	4	6	7	19	ZVS	low	95.4% at 415 W
[14]	$\frac{2n+4}{1-D}$	$\frac{V_0}{2n+4}$	$\frac{(n+1)V_0}{n+2}$	2	3	6	6	17	ZVS	low	96% at 200 W
[15]	$\frac{1+n+D}{1-D}$	$\frac{V_0}{1+n+D}$	$\frac{2V_0}{1+n+D}$	1	4	2	8	15	ZVS	low	94.7% at 200 W
[16]	$\frac{2+3n}{1-D}$	$\frac{V_0}{2+3n}$	$\frac{(2n+1)V_0}{2+3n}$	2	2	8	8	20	ZCS	low	97.2% at 200 W
[17]	$\frac{A^*}{1-D}$	$\frac{V_0}{A^*}$	$\frac{2V_0}{A^*}$	2	4	6	8	20	ZVS	high	95% at 760 W
[18]	$\frac{2+2n}{1-D}$	$\frac{V_0}{2+2n}$	$\frac{(1+2n)V_0}{2+2n}$	2	2	6	7	17	ZCS	low	93% at 1000 W
proposed converter	$\frac{1+3n}{1-D}$	$\frac{V_0}{1+3n}$	$\frac{2nV_0}{1+3n}$	2	3	6	7	18	ZVS	low	96% at 270 W

$^* A = \frac{4n+3-(1-2n)D}{1-D}$

However, its higher number of components and switches leads to increased conduction losses and operational complexity. On the other hand, the converter in [18] benefits from a lower component count and automatic current balancing control. Nevertheless, it suffers from lower voltage gain, higher switch voltage stress than the proposed converter, and capacitive turn-on losses, which adversely affect the efficiency of the converter.

Figure 13 compares the gain of the proposed converter with similar converters for turns ratios of 2 and 3. The results indicate that the proposed converter achieves a higher gain compared to all other converters at a turns ratio of 2. At a turns ratio of 3, it has a lower gain only compared to converter [16]. According to figure 13(b), the voltage stress on

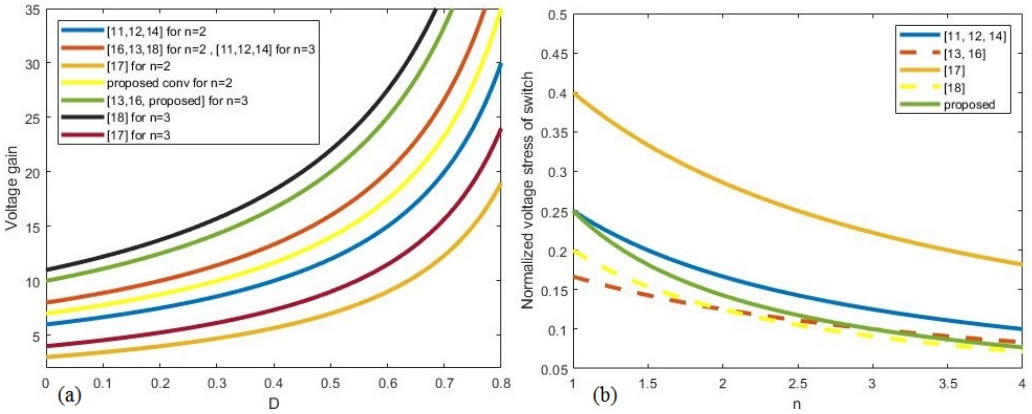

Figure 13. Comparative graphs (a) Voltage gain comparison graph (b) Maximum voltage stress on switches comparison graph.

the switch at high turns ratios is the lowest among all the converters.

7. Conclusion

This paper introduces a voltage-boosting converter designed to minimize input current ripple and minimize voltage stress on the switches. The converter incorporates a new auxiliary circuit that facilitates ZVT for the main switches and ZCT for the auxiliary switch. The auxiliary circuit is designed to have minimal impact on converter losses due to its low component count, short conducting time, and soft-switching operation of the auxiliary switch. Additionally, the proposed auxiliary circuit is modular and allows for expansion to more parallel branches without requiring an additional switch. To effectively reduce input current ripple, the converter utilizes winding-cross-coupled inductors. Overall, this converter offers higher efficiency and lower electromagnetic interference compared to hard switching methods.

Authors contributions
Authors have contributed equally in preparing and writing the manuscript.

Availability of data and materials
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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