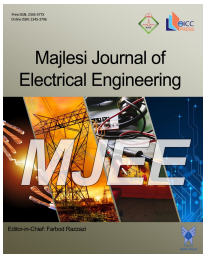

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Design of 65 nm 6T SRAM using improved sense amplifiers and write driver circuits

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Original Research

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Abstract:

Designing high-speed 6T SRAM for efficient read and write operations poses a significant challenge for circuit designers. In this paper, we propose a 65 nm 6T SRAM architecture using sense amplifiers and write driver circuits to enhance the read and write performance. The sense amplifier helps the reading process go faster and the reading data be more stable. The write driver is designed with a symmetrical structure to reduce the write delay. In addition, the control circuit performs the checking process to synchronize read operations, optimize latency without interruption. The simulation result shows that the read delay and write delay are 58.66 ps and 79.67 ps, respectively. These delays outperform most of the other study.

Keywords: Static random-access memory; Sense amplifier; Write driver circuit; Complementary metal oxide semiconductor; 65 nm

1. Introduction

SRAM (Static Random Access Memory) represents a crucial component in modern memory architectures, offering rapid access time and low power consumption [1]. The approach of pipelined hierarchical SRAM designs has shown significant improvements in both speed and power efficiency compared to traditional non-hierarchical SRAM architectures [2]. However, with the continuous increase in transistor density and the growing demand for high-speed data processing, SRAM design faces significant challenges related to power consumption and operational stability. Therefore, developing more optimized SRAM architecture has become essential to balance fast read/write performance with energy efficiency in modern systems.

Numerous prior studies have presented different SRAM designs. Some works have shown comparative analysis of SRAM Cells in different technologies [3–6]. S. Bagali et al. [7] proposed a 6T SRAM design in 45 nm and 180 nm technology using Cadence Virtuoso tool. The design consists of cross-coupled CMOS inverters P1-N1 and P2-N2 and two access transistors for reading and writing data to and from the memory, it was optimized to consume less power, space, and time to read and write data. M. Abhiram et al. [8] proposed 6T and 9T SRAM cells using 7 nm technology which not only consumes less power but also offers faster read/write operations. A. Siddik et al. [9] presented CMOS SRAM 6T, 7T, and 9T Cells using Cadence at 180 nm Technology. This work has shown the performance analysis comparison among 6T, 7T, and 9T SRAM cells [10] proposed an optimization of a 6T SRAM cell design in 90 nm and 45 nm technology using Low-Voltage Transistors instead of conventional transistors.

The designs in [7–9], and [10] focus on a single SRAM cell and use pulse sources to control read and write operations. Consequently, the SRAM cells of these designs do not accurately capture the read and write processes of an SRAM cell, i.e., the discharge and recharge of the bit-lines (BL) and bit-line bars (BLB). In addition, these studies do not present control circuits for SRAM cells. Designing a full SRAM circuit poses numerous challenges, including managing address lines, read/write signals, and implementing

auxiliary circuits to enable faster and more stable read/write operations. In our research, we propose a comprehensive 6T SRAM circuit design that incorporates clock signals, address buses, read/write signals, data in, and data out. This approach allows for a more accurate simulation of the operations of a complete SRAM circuit in practice. Furthermore, our design integrates sense amplifiers and write drivers to enhance the speed and stability of the read/write operations. Our design uses 65 nm process technology because this process is popular for university research and has reasonable manufacturing costs. This research's primary contribution is optimizing these circuits, resulting in significantly improved stability during read and write processes. The improved sense amplifier allows it to cut off from BL/BLB during read operation, guaranteeing steady and unaffected data output. Simultaneously, a symmetrical structure of the write driver is added to ensure that the input data of the SRAM is steady and not floating. In addition, our design includes a checking operation to turn the sense amplifier enable signal on and off at the right time to optimize latency for the read process.

2. Method

The overall architecture of the proposed SRAM is shown in Fig. 1. The architecture comprises of four main blocks: The Control Block, XDEC Block, Cell Array, and DIDO (Data In Data Out). Each block plays a vital role in the efficient operation of SRAM, ensuring seamless data retrieval and storage processes.

A. Cell SRAM structure

Cell SRAM 6T (6-Transistor Static Random-Access Memory) represents a fundamental and vital type of Static Random-Access Memory (SRAM) in the semiconductor industry and system design. The decision to select a 6T SRAM architecture over alternatives such as 8T or 9T is motivated by its inherent symmetric design [3]. This symmetry enables effective voltage balancing, and when combined with a sense amplifier, it creates an optimal ΔV for the sensing operation. Consequently, the read process is significantly accelerated, enhancing overall performance.
The structure of the 6T SRAM cell, as shown in Fig. 2, is a critical component in SRAM memory design.
Four NMOS transistors are structured as follows. Two of

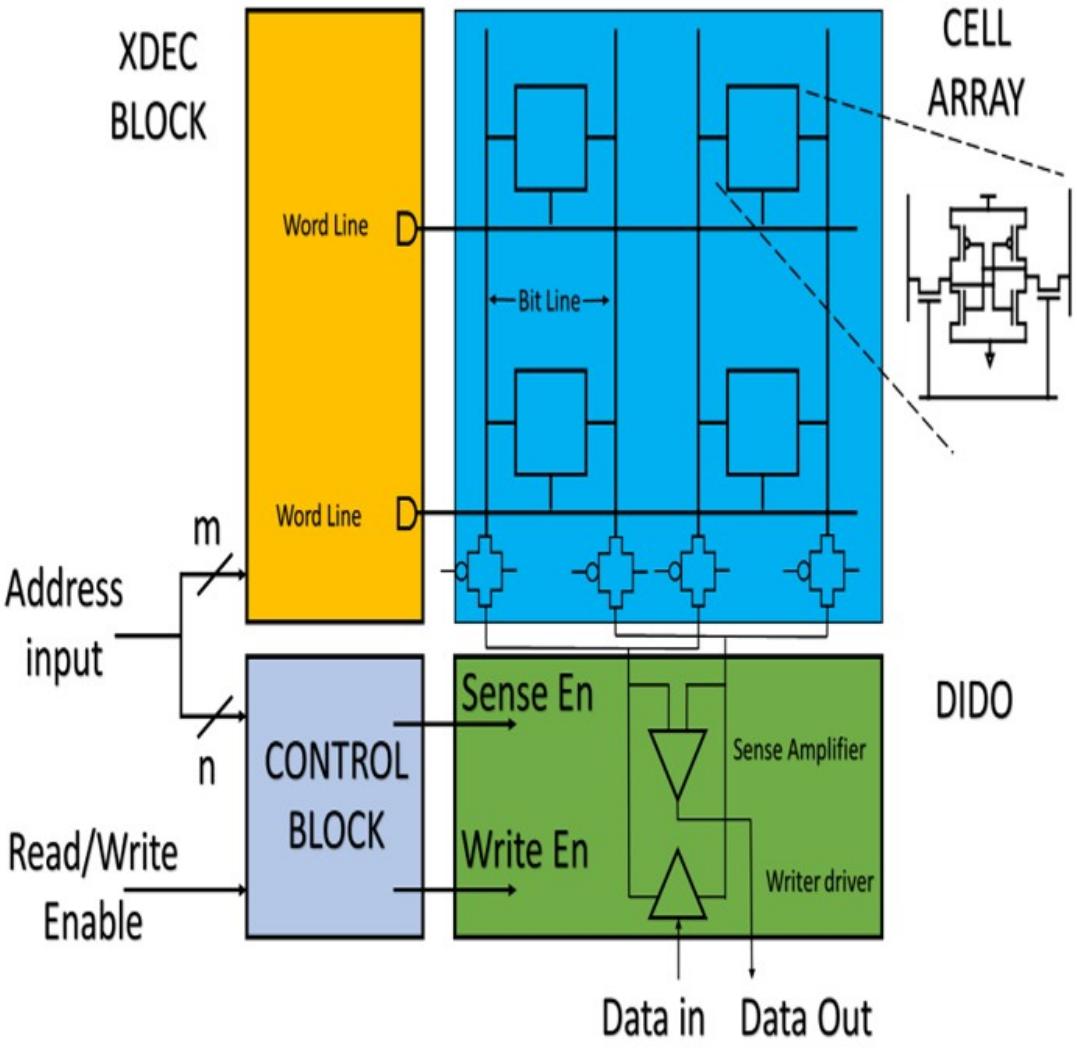

Figure 1. The functional block diagram for SRAM.

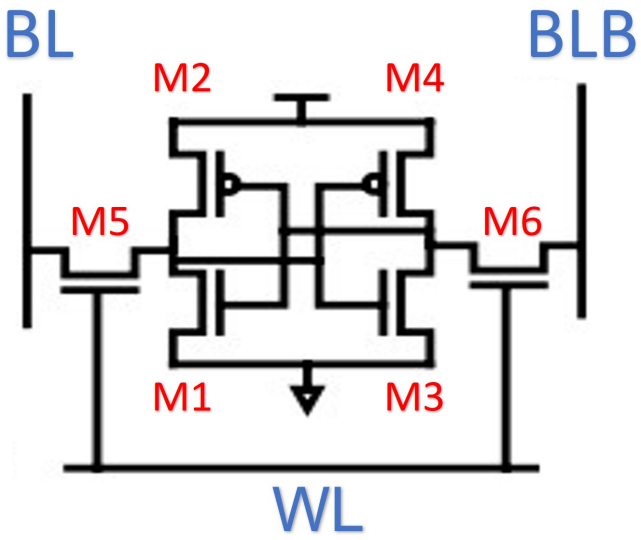

Figure 2. SRAM 6T structure.

them (M5 and M6) are connected between the data bit and a BL/BLB. The remaining two transistors (M1 and M3) operate as an Inverter pair, determining the storage state of the cell. Two PMOS transistors (M2 and M4) also operate as an Inverter pair and are connected inversely to M1 and M3, controlling the storage state of the SRAM cell.
Operation of the SRAM 6T is described as follows.
When writing data into the SRAM cell, the value to be stored is loaded into the BL, and its inverse value is loaded into BLB. Then, 2 NMOS pass-gates (M5 & M6) are opened to modify the data stored in the Cell.

When reading data from the Cell, BL & BLB are pre-charged to a high logic level, and then, 2 NMOS pass gates (M5 & M6) are opened. If the data in the Cell is 0, the BL is pulled low. At this point, the value in the Cell is read out.

B. Cell array structure

The Cell Array, shown in Fig. 3, is an array of SRAM cells composed of individual cells. In this research, a Cell Array is designed by 8 SRAM memory cells, organized in a 4×2 structure, which is a fundamental architecture block of Static Random-Access Memory (SRAM). The

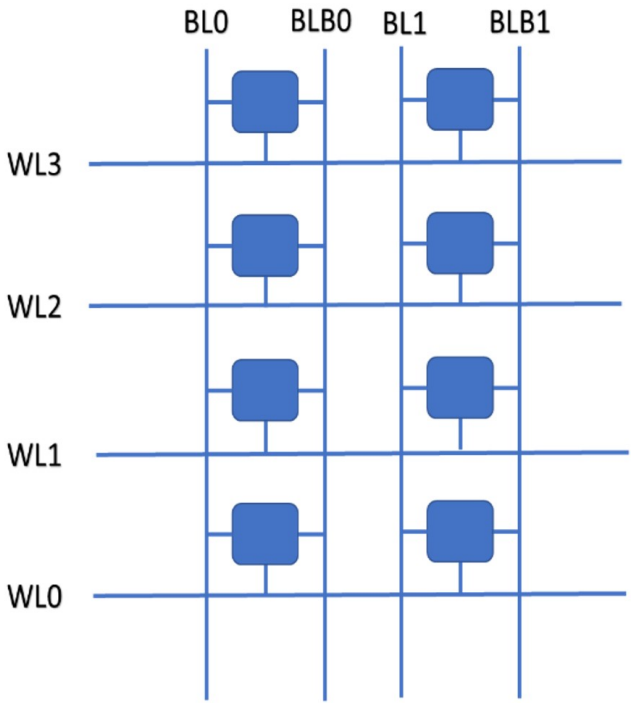

Figure 3. Cell array structure.

4×2 structure comprises four rows and two columns of SRAM memory cells, enabling efficient parallel access and storage of data.
When arranging the cells together, cells in the same column share the same BL and BLB lines, resulting in a total of 2 BL and 2 BLB lines. Similarly, cells in the same row share the same WL line, resulting in 4 WL lines.

C. Control block structure

The Control Block, as shown in Fig. 4, includes an Address Decoder, a Checking unit, a Write Enable (WE) line, and a Sense Amplifier Enable (SAEN) line.
This block serves as the central hub, receiving input address signals to select the SRAM cells for access. Additionally, it manages Read/Write Enable signals to facilitate read and write operations within the SRAM array. Through the interpretation of these signals, the Control Block triggers Sense Amplifier Enable or Write Enable signals, crucial for the read and write processes, respectively.
The Control Block performs a checking process to ensure that the read/write operations of data in and data out are completed at the correct timing and prepared for the initiation of read/write processes for the next cycle. This process involves generating checking signals within the Control Block, which then passes through dummy 6T SRAM cells to create Dummy Word Line (DWL) and Dummy Bit Line (DBL) signals.

D. XDEC block structure

The XDEC (X-Decoder) block, as shown in Fig. 5, is a crucial component in memory circuit design, especially in SRAM memory architecture. XDEC is responsible for controlling the data read and write processes in SRAM by decoding and determining specific rows or columns of the memory array to access. It is often accompanied by a series of address decoding circuits and designed to optimize access performance by accurately selecting and activating the desired rows or columns. It plays a vital role in ensuring the accuracy and efficiency of the data access process in SRAM memory circuits.
The XDEC Block performs its function by receiving Predecode address lines (AC & AE) from the Control Block, which helps us select the desired XDEC. Once a particular XDEC is selected, the address lines AX (0:3) choose the WL line we desire. Consequently, we select the desired SRAM cell and read or write to the correct cell as intended.

E. DIDO block structure

The DIDO (Data-In/Data-Out) block is a critical component in SRAM memory architecture. It plays a vital role in trans-

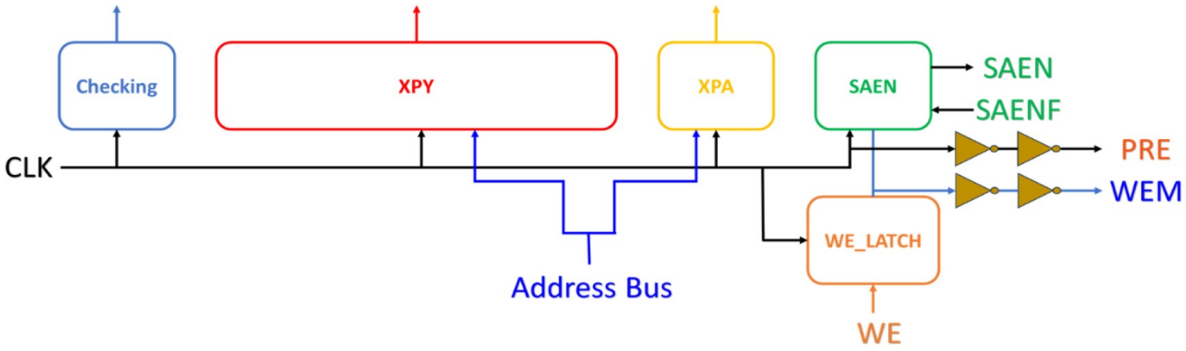

Figure 4. Control block in SRAM 6T structure.

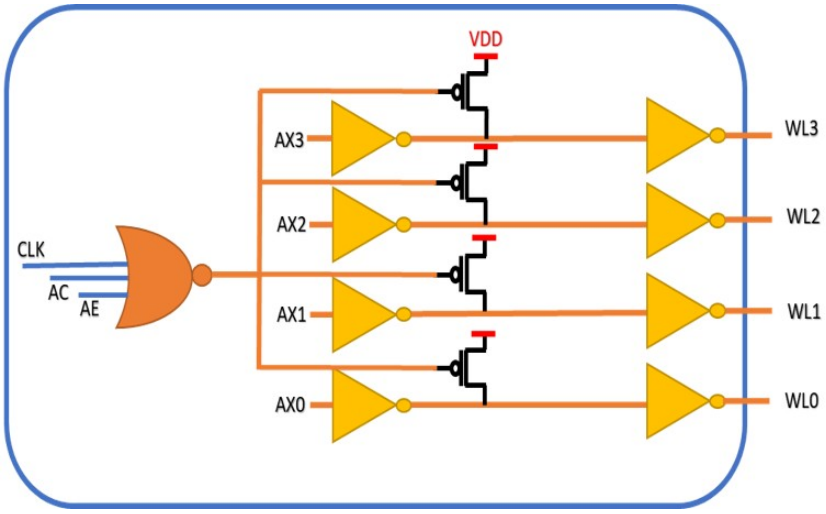

Figure 5. XDEC block structure.

ferring data into and out of the memory circuit, serving as a crucial element in the data read and write processes.
During the read process, DIDO receives data from the memory circuit and transfers it out of the memory for processing or forwarding. In the writing process, DIDO accepts data from peripheral sources or processing units and inputs it into the memory circuit for storage.
DIDO is typically designed to optimize data bandwidth and ensure efficient data transmission between the SRAM memory circuit and other parts of the system. Its efficiency is pivotal in enhancing the overall system performance, particularly in applications that demand fast and continuous data access.
The DIDO block consists of two smaller blocks: LDIDO (Local) and GDIDO (Global), which are described in the next section.

F. LDIDO structure

LDIDO, as shown in Fig. 6, assists in selecting one of the two columns of cells in the array. This block receives address decoding signals from the Control Block and selects one of the two pairs of BL/BLB in the Array.

G. GDIDO structure

GDIDO, as shown in Fig. 7, includes three components: Pre-Charge, Sense Amplifier and Write Driver. The Pre-Charge circuit supports read and write processes by charging BL and BLB to VDD at the beginning of each operating cycle. Then, depending on the read and write data, it will change the logic level of BL or BLB. Additionally, the Data Out signal has a latch circuit for stabilizing the output value.

H. Sense amplifier

We proposed a design of the sense amplifier, which is shown in Fig. 8. This block is a crucial circuit that supports the data reading from SRAM cells by comparing the voltage difference (Delta V) between bit lines BL and BLB. This comparison accelerates the reading process and significantly reduces power consumption during read operations.
The operation of the sense amplifier is described as follows. During the initial phase of the read operation, when EN = 0, the two top PMOS transistors are activated, connecting BL to RBL and BLB to RBLB. At this moment, SAEN = 0, which enables the two PMOS transistors within the Sense Amplifier, connecting RBL to DLL and RBLB to DLLB internally. The four MOS transistors (including two PMOS and two NMOS in the center) operate as a SRAM cell, establishing a balanced potential to determine which bit line is being pulled down more significantly. This mechanism enhances the differential sensing process, allowing the Sense Amplifier to accurately detect and amplify the stored data. Once the Checking process is completed, SAEN is asserted (SAEN = 1), disconnecting RBL from DLL and RBLB from DLLB. This separation allows the read operation to execute faster, as it eliminates the need to discharge the full charge stored within the Cell Array onto BL and BLB. The DO is directly connected to the power supply through DLL and DLLB, ensuring optimal output signal quality. Furthermore, after the DO signal is generated, it is latched and sent to the output stage, enhancing the stability of DO.

I. Write driver

The Write Driver is proposed as shown in Fig. 9. This is a circuit designed to facilitate the writing of data from the Data input into the SRAM cells. The writing process is performed by loading the data onto the two-bit lines, BL and BLB, and preparing it for entry into the SRAM cells.
The write operation is described as follows. When a Data In (DI) value is provided for the write process, it generates two corresponding signals, including WBL = DI and WBLB = NOT(DI).
For example, if DI = 1, then WBL = 1 and WBLB = 0. When the write operation is initiated (EN = 1), WBL is connected to BL, while WBLB = 0 activates the upper PMOS transistor, connecting BL to VDD. This ensures that BL is driven to a stable high voltage, improving signal integrity and speeding up the write process. The same principle applies to BLB, ensuring a fast and stable write operation.

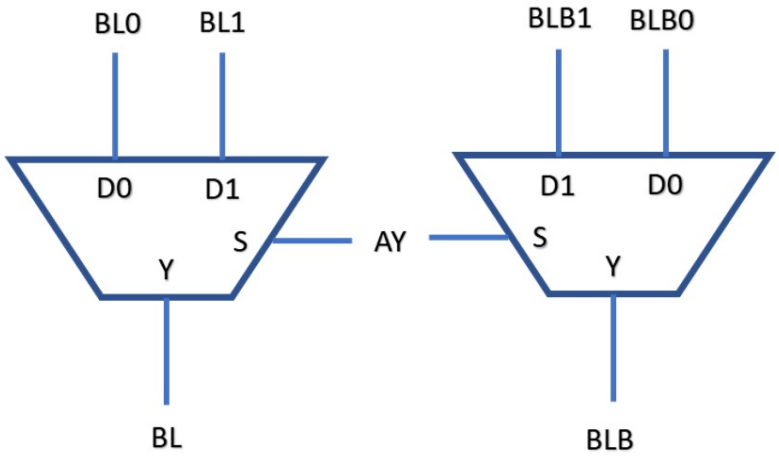

Figure 6. LDIDO block structure.

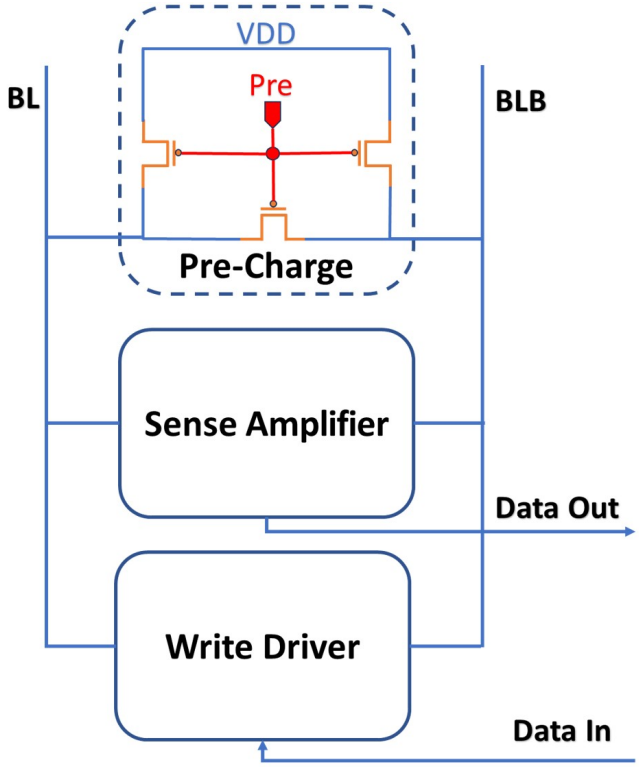

Figure 7. GDIDO block structure.

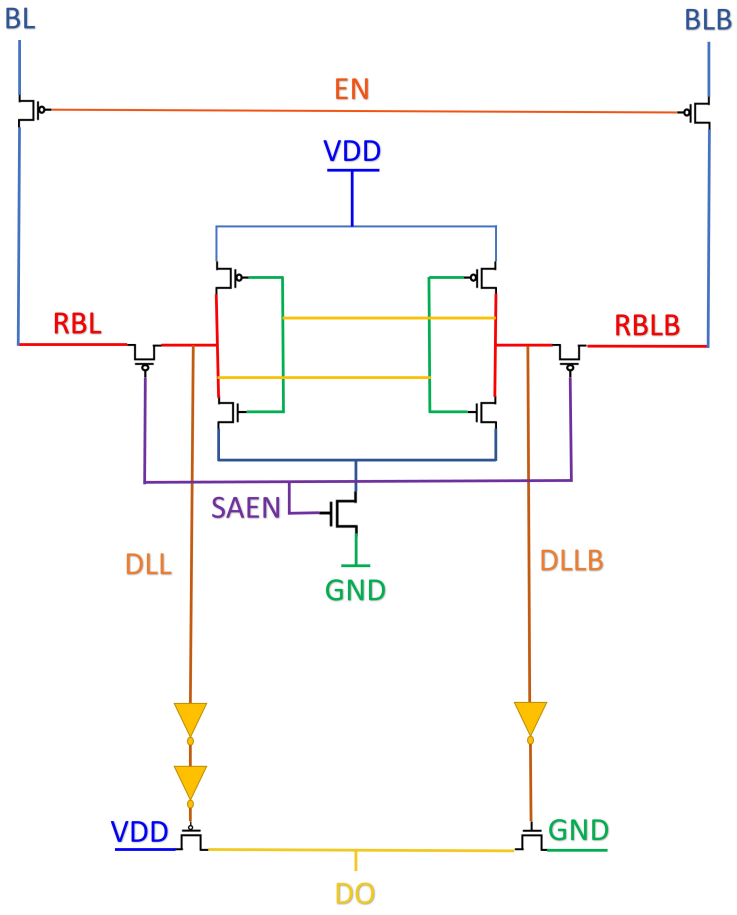

Figure 8. Sense amplifier structure.

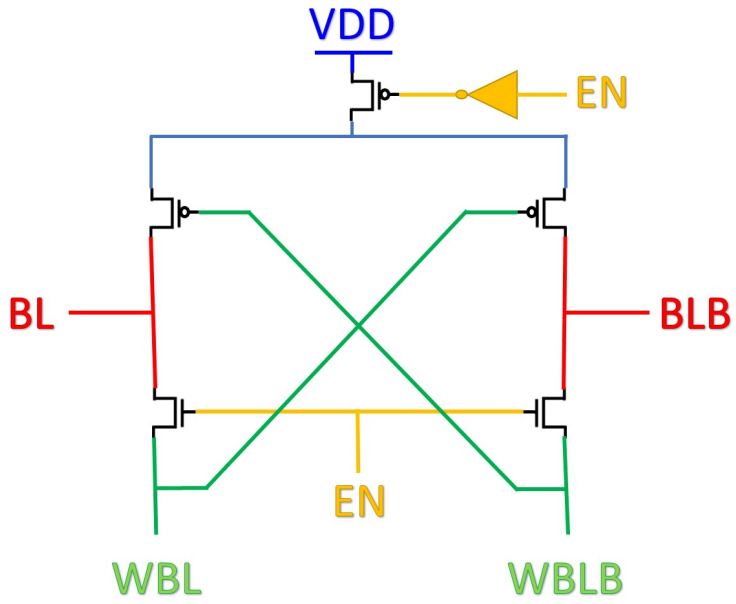

Figure 9. Write driver structure.

J. Checking operation

The Checking Operation structure is shown in Fig. 10. The Checking signal is generated within the Control Block and then propagates through dummy 6T SRAM cells to generate Dummy Word Line (DWL) and Dummy Bit Line (DBL) signals for the Checking process. This process closely mimics a real read operation of an actual SRAM cell, thereby activating the SAEN signal at the precise required timing. As a result, it ensures that Read/Write operations for Data In and Data Out are completed at the correct time while preparing for the next Read/Write cycle.

3. Results and discussion

In our experiment, the design and simulation have been performed by using Cadence Virtuoso tool, employing ADE XL to set up the simulation conditions. The schematic of the 6T SRAM cell is shown in Fig. 11. The primary simulations were conducted on the TTNN corner (Typical-Typical, 1 V,

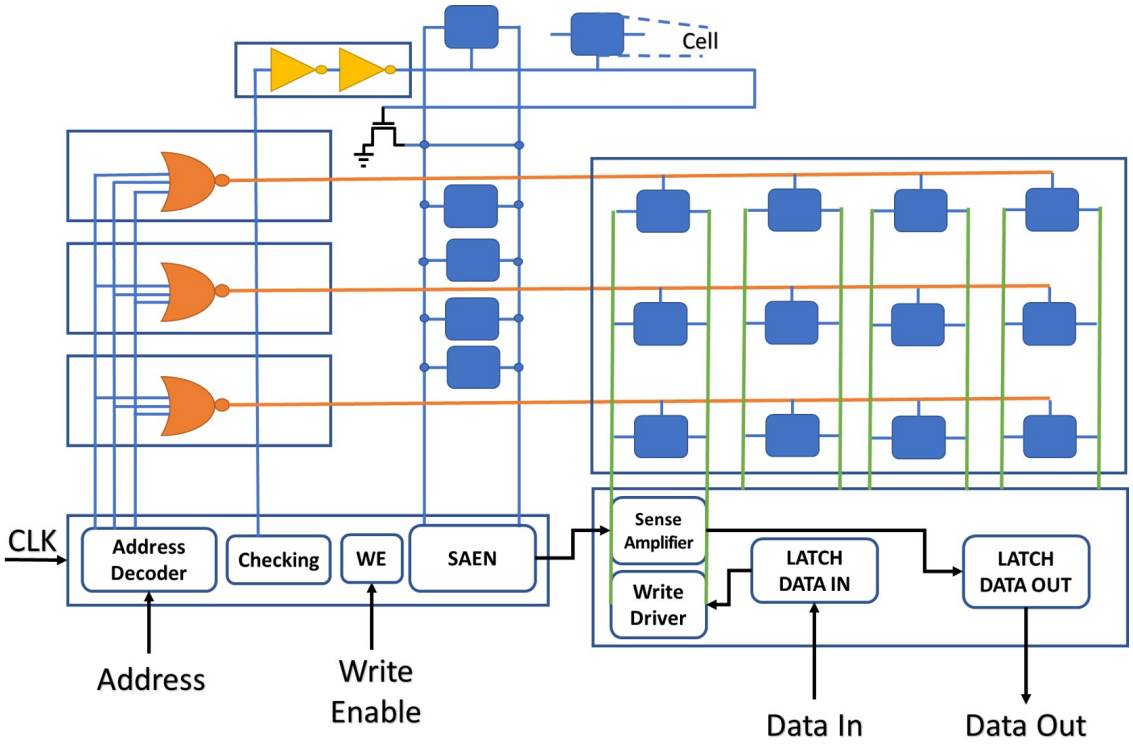

Figure 10. Checking operation structure.

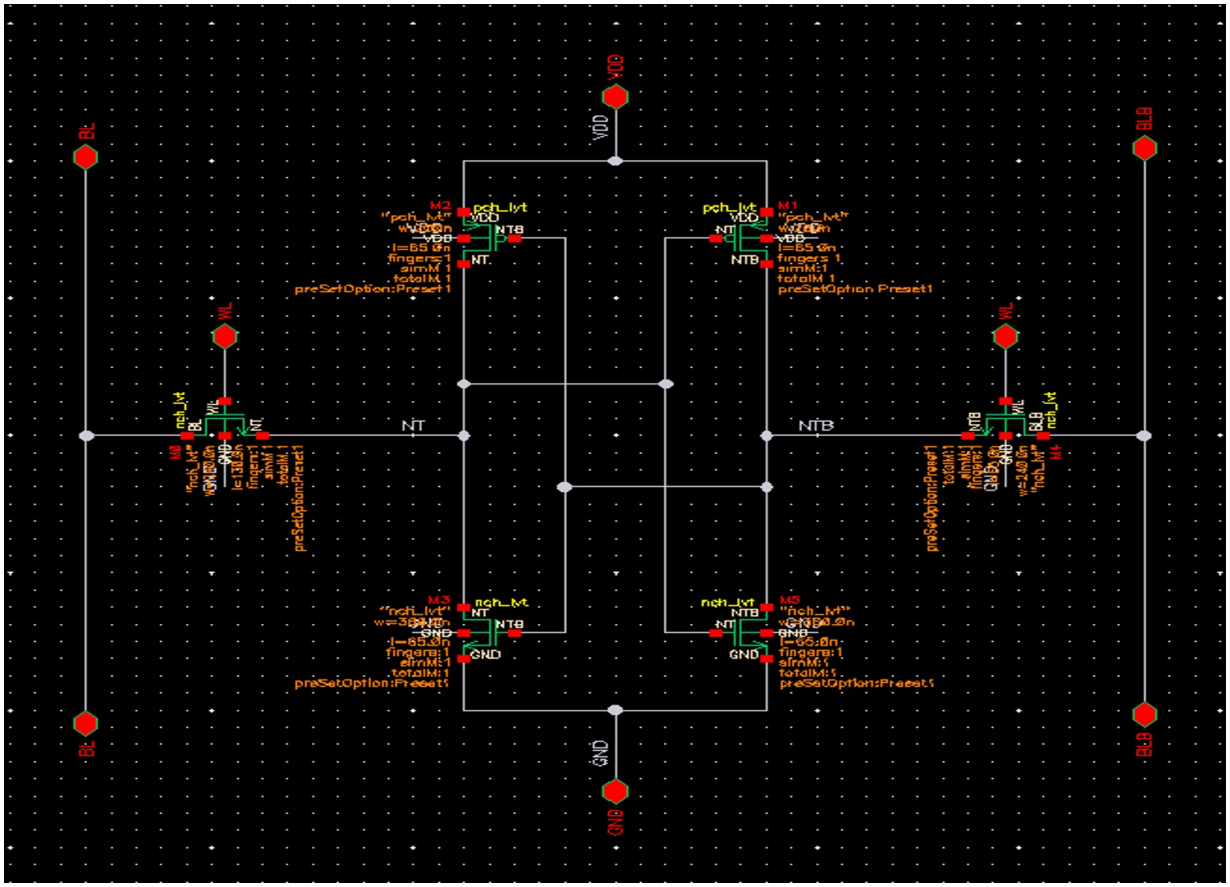

Figure 11. Schematic of 6T SRAM cell.

25 °C). In order to verify the operations of the proposed SRAM, we design a test circuit as shown in Fig. 12.

A 65 nm 1 V standard CMOS process is applied to verify the performance of our proposed circuit. In this study, the complete SRAM circuit with an 8-bit size (Cell Array 4×2) and 1 DIDO were simulated, focusing on verifying the Read/Write processes of the circuit. Power was supplied to generate square wave clock signals and provide value for Address and Data during the simulation process. In the circuit, a capacitor of 5 fF was added to both the BL and BLB lines to simulate the effect of delay on the circuit due to multiple cells connecting to BL and BLB. This addition allows for a more accurate representation of the potential impact of charging and discharging delays when multiple cells are connected to these lines.

A. Simulation results

In this scenario, the number of cells is small, and the operating clock frequency is 1 GHz. Fig. 13 and Fig. 14 present the Read/Write processes of the SRAM circuit. The read and write operations are stable at a frequency of 1 GHz and 1 V VDD.

During the first half cycle of the clock pulse, the Data In and Address values are prepared. As the clock pulse rises, these values are then inputted to execute the processes of the circuit. Upon completion, and as the clock pulse falls, the signals within the circuit are turned off, awaiting new values for the next operating cycle.

B. Parameter evaluation

After simulating the processes, timing parameters were measured to assess the performance of the SRAM circuit. Table 1 presents the obtained timing values.

Access Time represents the duration from when the clock pulse rises until the Read process completes (after this time, Data Out stabilizes, and access to retrieve Data Out is feasible). Write Time indicates the delay in executing the Write process (the time taken for the SRAM cell to change its state). Read Time denotes the delay for executing the Read process (the duration from when SAEN is activated until DO changes).

Regarding power consumption, each operational process of the circuit corresponds to a specific power consumption. Table 2 illustrates the power consumption of the proposed SRAM circuit.

C. Performance comparison

Table 3 presents a performance comparison between the design study conducted in this paper and several other research articles.

According to the simulation results, the performance of the proposed SRAM design outperformed most of the other designs. The SRAM designs in [7] and [10] have a much average delay because the transient period is high. In addition, the power consumption of these designs is high, because bit-lines of the SRAM cell are connected directly to the power source instead of using the Pre-Charge circuit. The

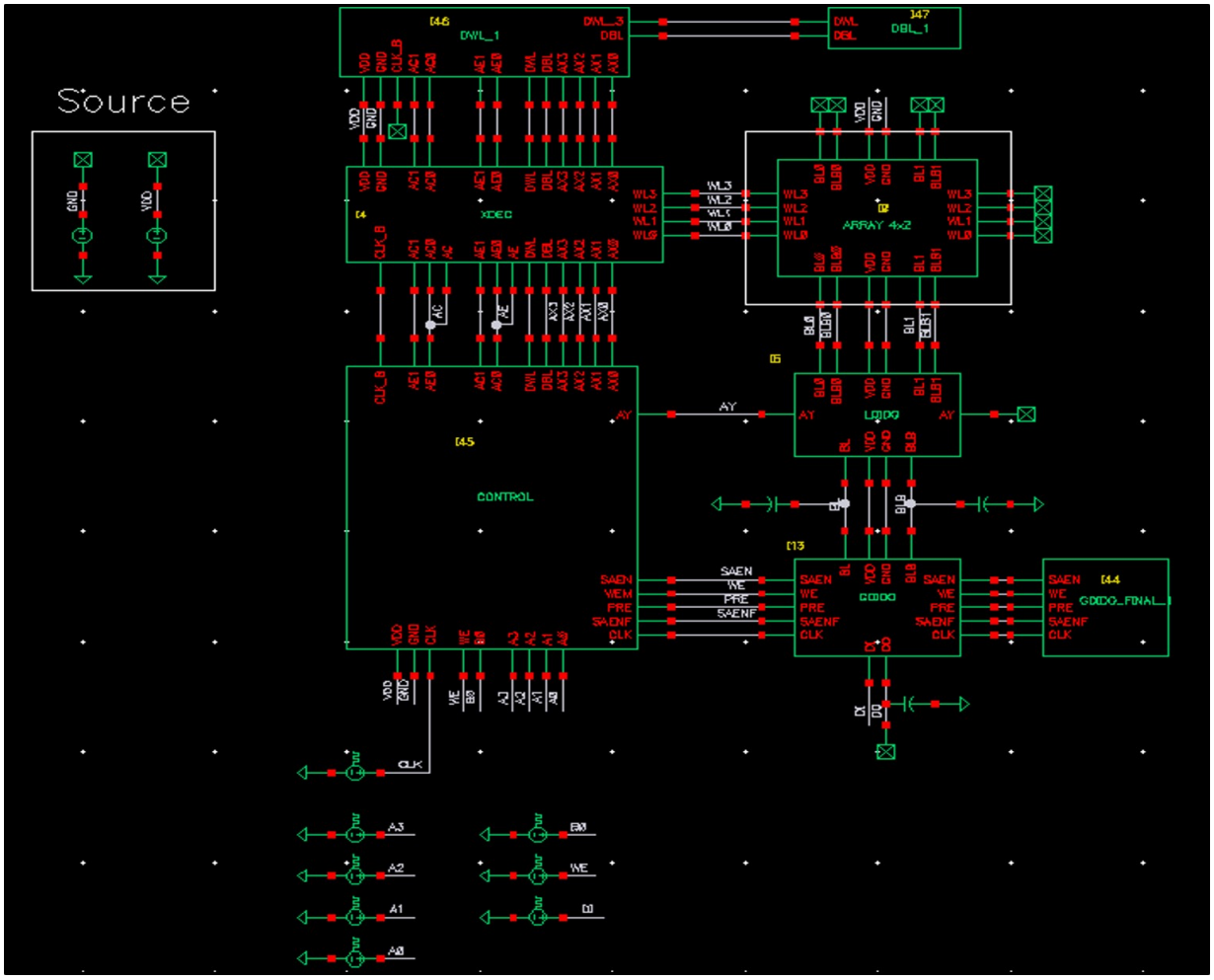

Figure 12. Testbench circuit of the proposed SRAM.

design in [8] showed the best performance since it has only one cell, which is implemented by the 7 nm technology. The proposed design focuses on the improvement of Read/Write processes by using Pre-Charge, Sense Amplifier, and Write Driver circuits. Therefore, the average delay and power consumption are much improved. This result provides insights into the advantages of the approaches of proposed design.

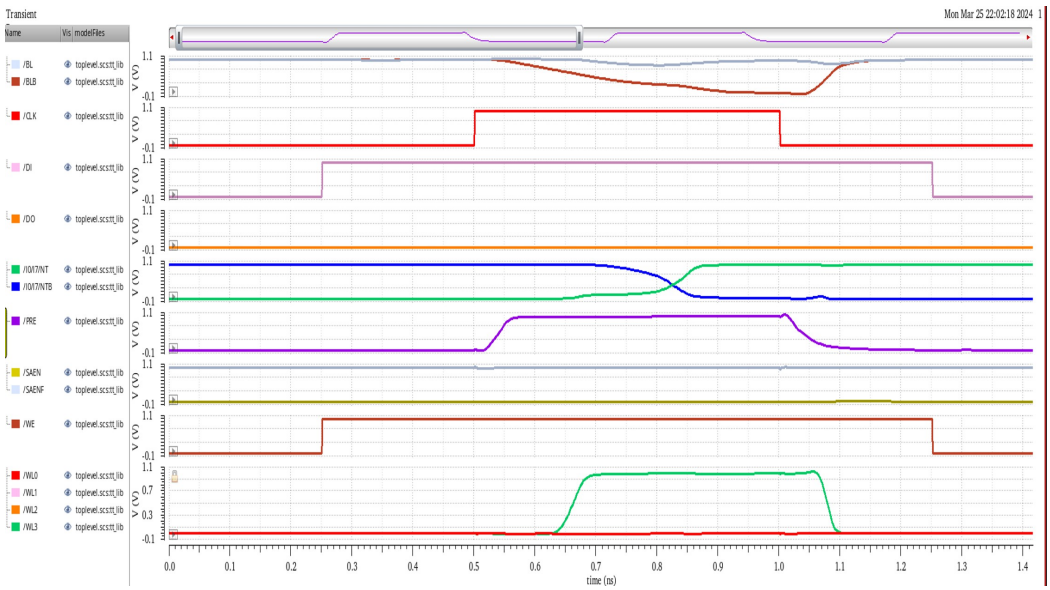

Figure 13. Writing operation.

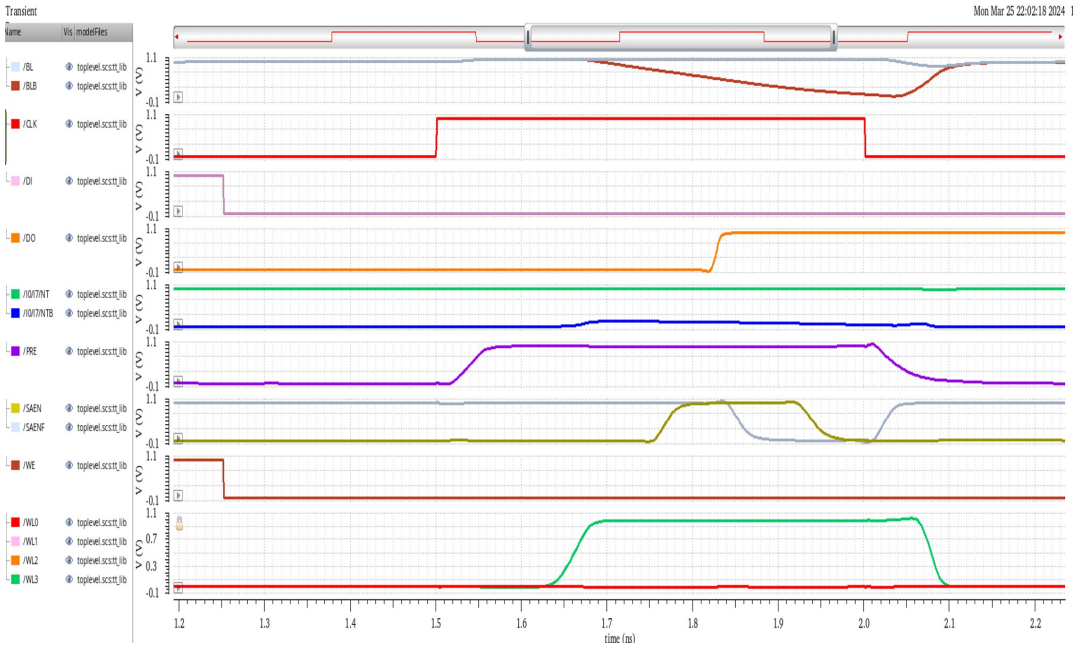

Figure 14. Reading operation.

Table 1. Timing parameter of the proposed SRAM circuit.

Parameter	Value
Access time	332.11 ps
Write time	79.67 ps
Read time	58.66 ps

Table 2. Power consumption of the proposed SRAM circuit.

Parameter	Value
Read power	185.4 µW
Write power	183.3 µW
Power consumption	368.7 µW

Table 3. Performance comparison.

Design	Cells	Supply voltage (V)	Technology (nm)	Power (µW)	Average delay (ps)
Proposed	6T	1	65	368.7	332.11
S. Bagali [7]	6T	1	180	898.3×10^3	25.30×10^3
	6T	1	45	502.0×10^3	23.76×10^3
M. Abhiram [8]	6T	0.7	7	4.0305	46.2061
T. Kalpana [10]	6T	1	90	558×10^3	22.1×10^3
	6T	1	45	294×10^3	20.7×10^3

4. Conclusion

This paper has presented a complete design of 6T SRAM, including detailed schematic diagrams of the Control Block, XDEC, Array Cell, and DIDO modules. The simulation of Read/Write operations has been conducted to verify the correct functionality of the design. The performance of the proposed SRAM is noteworthy, with a power supply voltage of 1 V and an operating frequency of 1 GHz. The power consumption of the SRAM under these conditions is measured to be 368.7 µW, indicating efficient power utilization. In addition, our complete 6T SRAM design incorporates a sense amplifier circuit that disconnects the BL/BLB lines during the read process, thereby reducing power consumption and accelerating read operations. Moreover, the integration of a write driver contributes to faster and more stable write processes. Overall, the results demonstrate the viability and effectiveness of the designed 6T SRAM for various applications in high-performance computing and integrated circuits.

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Authors contributions
Authors have contributed equally in preparing and writing the manuscript.

Availability of data and materials
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of interests
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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